Regulations & Syllabi for DipIETE Examination (Electronic & Telecommunication)

सह वीर्यं करवावहै

Prof. V N R Pillai VC, IGNOU Chief Guest lighting the ceremonial lamp with Prof. B S Sonde, Past President IETE and Shri S Narayana, President, IETE at the 1st Convocation Day - 02 Nov. 2007

Dr. Anil Kakodkar, Shri G Madhvan Nair and Shri S Narayana at the Inauguration of Exhibition during 50th Annual Technical Convention at Hyderabad -29-30 Sept. 2007.

Students after attending 1st Convocation on 02 Nov. 2007.

Installation of New President Lt Gen Ashok Agarwal, PVSM (Retd) for the year 2008-09 by the Chief Guest Shri N R Narayana Murthy, Chairman of the Board and Chief Mentor, Infosys Technologies Ltd, Bangalore during the inaugural session of the 51st Annual Technical Convention of 29 Sep 2008

Release of Special Issue of IETE Technical Review during the inaugural session at the 51st Annual Technical Convention on 29 Sep 2008. Seen in the picture are - Shri P N Chopra, Shri S Narayana, Shri N R Narayana Murthy (Chief Guest), Lt Gen Agarwal, PVSM (Retd), Shri A Bhaskaranarayana and Brig V K Panday.

Prospectus
Containing
Regulations & Syllabi
For
DipIETE Examination
(Electronics & Telecommunication)

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Website : http://www.iete.org
Phone : (011) 43538800-99
Fax : (011) 24649429
Email : sec.gen@iete.org,
        membership@iete.org.

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CONTENTS

THE INSTITUTION

INTRODUCTION

The Institution of Electronics and Telecommunication Engineers (IETE), formerly the Institution of Telecommunication Engineers (ITE) was founded in 1953 by a small group of professionals for the advancement of Telecommunication and Electronics in India. Today the Institution has grown in its status to international levels with its manifold activities for furthering the cause of development in the key sectors of Electronics, Telecommunications, Computer Science Engineering, Information Technology and allied disciplines. The emphasis of the current activities is on creation of a concrete base of trained manpower in these fields at various levels of competence and also to contribute gainfully towards the continued professional development needs of existing technical personnel. The IETE also provides a platform for meaningful interaction among professionals from the Industry, R&D Organisations, Educational Institutions and Government Departments.

MEMBERSHIP

1.   The IETE is a professional society devoted to the advancement of Electronics and Telecommunication, Computers and Information Technology. The Institution is headed by a Council, elected from its large base of corporate members in India and abroad. It confers professional status by way of admitting such persons, as may be qualified to various classes of membership such as Honorary Fellow, Distinguished Fellow, Fellow, Member, Associate Member, Diploma Member Student Member and Associate. Organizational Membership is also open to Public/Private Sector Companies, Institutions, R&D Laboratories and Government Organisations.

OBJECTIVES

2.   The IETE focuses on advancing the science and technology of electronics, telecommunications, computers, information technology and related areas. The objectives of the Institution include;

   •   Organise conferences, symposia, workshops and brainstorming sessions involving all concerned professionals students and industry associations for the advancement of the Disciplines.

   •   Provide a forum for discussion on national policies and to provide suitable inputs to policy makers.

   •   Promote and conduct basic engineering and continuing technical education programmes for human resource development.

   •   Bring out quality publications for all levels of readership.
       Honour outstanding professionals.

EXAMINATIONS

3.   The IETE conducts Diploma Level (DipIETE) Examination, in order that a student qualifies and become a Diploma Member. At the time of enrolment, a student is enrolled as Student Diploma (SD) scheme On successful completion of the curriculum and clearance of requisite membership fee, he is made a Diploma member of IETE (DipIETE). Such members are then eligible to pursue AMIETE course without paying any enrolment fee. The DipIETE Examination is recognized by the Ministry of Human Resource Development (MHRD). A similar recognition has also been given by several State Governments – **(Appendix 'F' (Annexure I, II, III, IV, V, VI. VII. VIII, IX and X) and the list of recognitions of DipIETE is given at Appendix 'G'.**

FACILITIES FOR STUDENTS

6   The IETE helps the students by extending library facilities, laboratory assistance, and coordination of IETE Students Forum and by providing necessary guidance at its IETE Centres. To spread its many fold technical activities in all the regions of the country, IETE has established so far 58 Centres spread all over the country including a centre at Kathmandu and examination centre at Abu Dhabi. IETE also has mutual arrangements with similar professional bodies like the Institution of Engineers (India), CSI, IEEE (USA), IEEE Com Soc and IET (UK) for availing each other's facilities for the benefit of its members.

LECTURES THROUGH EDUSAT SATELLITE

7   IETE has embarked on an ambitious project of " Reaching The Unreached "through its Satellite Education Programme In this programme, live, interactive lectures are broadcast from its Teaching End Studio at IETE, Noida centre and is received at classrooms terminals (SITs) at Ahmedabad, Bangalore, Bhopal , Chandigarh ,Delhi, Pune ,Hyderabad, Palakkad, Mankapur and Imphal

SOLUTIONS TO QUESTION PAPERS

8   To help the students , IETE has printed solutions to Questions papers for both AMIETE and DipIETE streams. List of subjects for which solutions are printed is available on the website www.iete.org

LABORATORY   MANUAL

9   All students of AMIETE and DipIETE pursuing new scheme implemented from Jun 09 exams are required to procure lab-manuals and conduct their experiments and record the same in the concerned lab-manuals   The manuals of all the lab examination have been printed. Students can obtain these manuals as under:

    (a)   From Reception counter at IETE HQ on payment of Rs.225/- per manual without CD and Rs 300/- for manual with CD.

    (b)   Through post by sending a DD in favour of Secretary General, IETE payable at New Delhi towards cost of Manuals plus postal charges   The postal charge is Rs 50/- per manual

    (c)   These manuals are also available at all IETE Centres. Students are advised to approach the nearby Centre for the same

ASSISTANCE IN PLACEMENT

10.   IETE makes effort to assist in the placement of students with the help of a Placement Cell established at IETE HQ, 2 Institutional Area, Lodi Road, New Delhi-110003..

RECOGNITION

11   The IETE is recognised by the Government of India as an EDUCATIONAL INSTITUTION OF NATIONAL EMINENCE.   The IETE has also been recognised by the Government of India, Ministry of Science and Technology, Dept of Scientific and Industrial Research as a SCIENTIFIC AND INDUSTRIAL RESEARCH ORGANISATION (SIRO). Copy of recognition letter is appended at **(Annexure !)**.

STUDENT INTERACTION CELL

12.   With a view to quickly resolve student queries, a single window to address all types of queries, problems and to help students, a Student Interaction Cell has been established at IETE HQ, New Delhi. This Cell is at the ground floor of the IETE HQ building. Student can approach SIC by -

- Tel No 011-43538853
- Fax   : 011-24649429
- SMS   : 53131 (By typing **IETEFB** followed by < **query** >)
- Email: sic@iete.org

13   If the students queries are not answered or resolved within a reasonable time, students may contact Secretary General, IETE through personal meeting or phone (011-43538821/22) or email (sec gen@iete org). **Students are not to approach any other section of the HQ as their queries/problems shall not be entertained by them.**

IMPORTANT INFORMATION

> **Students are advised to give their Mobile No. & Email ID for better and faster communication**

DipIETE EXAMINATION
REGULATIONS & SYLLABI

INTRODUCTION

.12.   IETE conducts DipIETE Examination in the following two streams.

    (a)   **Electronics and Telecommunication Engineering (ET)**
    (b)   **Computer Science and Engineering (CS)**

13.   The block and outline syllabi of these streams are given in this booklet. In addition, a detailed syllabus of Electronics & Telecommunication stream is given. **(please see Appendix 'A','B','C','D', and 'E').**

TRANSITION FROM OLD SYLLABUS TO REVISED SYLLABUS

14.   Existing students who are pursuing DipETE(ET) to be shifted to new syllabus if they do not complete the course by Dec 2010 examination. General Guidelines for Transition from Old Syllabus to New Syllabus is placed at **Appendix 'H '**. Details can also be obtained from the web site www.iete.org.

ELIGIBILITY

15.   A candidate desirous of taking up the DipIETE Examination should first be enrolled as Student (D) member as per Byelaw 17 of the Institution, which is reproduced below: -

Bye law 17 – Student (D) Member

Every candidate for election to the class of Student (D) shall satisfy the Council that he/she is not less than 14 years of age and has minimum pass in Class X conducted by a Recognised Board of Education with General Science (Physics) and Mathematics or its equivalent as prescribed by the Council from time to time; and

(a)   is sponsored by a Corporate Member of the Institution, and either

(b)   that he/she is or has been a student of Electronics Engineering/ Telecommunication Engineering/ Electrical Engineering/ Physics/ Computer Engineering as applicable, from a University/ College/ School approved by the Council

<div align="center">OR</div>

(c)   that he/she is or has been an engineering pupil/apprentice/assistant in a recognized firm, society or organization engaged in engineering or allied activities.

ENROLMENT

16   A candidate is required to apply for enrolment on the prescribed form **(Form IETE-2)**, which is appended in the last. The form also includes the conditions for eligibility Every application form for student member must be attached with the copies of certificates (age, educational/experience) duly attested by a Corporate member/Gazetted Officer, failing which the application shall not be entertained. For this purpose, the candidate may contact the office of the IETE centre/sub-centres of IETE. In case of any difficulty in getting the form proposed, the form may be submitted directly to the IETE HQ for further action.

ENROLMENT FEE

17. Fees to be paid for enrolment are as given in Form IETE-2 contained in this syllabus. The enrolment fees payable by student members are as under: -

		Member in India (Rs)	Member Abroad (US $)
(a)	Application Fee	200.00	40.00
(b)	Admission Fee	200.00	40.00
(c)	Building-cum-Lib. Fund	1300-00	260-00
(d)	Composite Subscription	1800-00	360-00
(e)	Lab Infrastructure Fee	500-00	100-00
(f)	Development Fee	500.00	100-00
(g)	Establishment Fee	500.00	100-00
		5000-00	**1000-00**

18. Enrolment fee is to be paid in one instalment at the time of enrolment. The student membership will be valid for 10 consecutive examinations from the date of enrolment. Thereafter, the student members not completing their DiplETE Examination are to seek re-enrolment for further 10 examinations by remitting applicable amount before or immediately after the expiry of the membership period to continue their membership to enable them to appear in the remaining papers and complete DiplETE. Any examination chance not availed by a student due to whatsoever reason will be counted within 10 examinations.

MINIMUM PERIOD OF MEMBERSHIP

19. A Student member shall be allowed to appear in the DiplETE Examination only after he has been enrolled as Student (D) member with the Institution. Only those Students (D) members enrolled on or before 28/ 29th February and 31st August, will be allowed to appear in the next DiplETE Examination of the Institution, held in June and December respectively. Membership should be alive at the time of submitting the examination application form.

DUPLICATE IDENTITY CARD

20. In case duplicate I-Card is required due to loss of original Card, application must be submitted along with a fee of Rs.500/-.

TIME LIMIT TO COMPLETE DiplETE

21. A student is required to complete DiplETE Examination within two enrolment periods of 10 consecutive examinations each from the date of initial enrolment. The student will, therefore, be permitted to seek only one renewal of membership. Renewal is to be applied for before or immediately after the expiry of initial enrolment with continuity of enrolment maintained by the student. Any delayed re-enrolment entailing missed chances will be counted towards total number of examinations and no relaxation in this regard will be permissible. If the request for renewal is made after the stipulated period of two enrolments, admission will be treated as a fresh enrolment and no benefit in terms of exemptions in respect of subject(s) passed or exempted during the earlier enrolment will be granted. Students must renew their membership in time. Otherwise they will not be allowed to appear in the DiplETE examination. No notice will be sent to the students for renewal of membership.

22. **The course curriculum and outline Syllabi for both the streams are given as follows: -**
    (a) **Course Curriculum (ET)** (Appendix-,A')
    (b) **Outline Syllabus (ET)** (Appendix-'B')
    (c) **Course Curriculum (CS)** (Appendix-'C')
    (d) **Outline Syllabus (CS)** (Appendix-'D')

    The detailed syllabus of Electronics & Telecommunication stream is appended at **Appendix 'E'.**

DiplETE EXAMINATION

23. DiplETE examination is divided in two Sections viz. Section A & B with a total 15 theory papers (8 in Section A and 7 in Section B) and 4 labs (2 labs in Section A and 2 labs in Section B). Each Section is divided in two parts viz. Part-I and Part-II. In addition a student has to undergo a project work and a Course in Communication Skills & Technical Writing. The course on Communication Skills & Technical Writing is mandatory but would not count towards overall CGPA.

24. Distribution of subjects is as under.

    (a) SECTION A

    PART-I   Four subjects & 1 Lab
    PART-II   Four subjects & 1 Lab

    (b) SECTION B

    PART-I   Four subjects & 1 Lab
    PART-II   Three subjects & 1 Lab
                          (One compulsory & two from
                          Elective subjects)

    (c) PROJECT WORK

    (d) COURSE IN COMMUNICATION SKILLS & TECHNICAL WRITING (Any time during the course)

25. Not withstanding above, a student will not be allowed to complete the curriculum in less than three years unless he has been exempted in some subjects.

27 **Eligibility for Project**

A student can apply for registration of Project (DE 64) after eligible for Lab III. The student can appear for mid term examination of project (viva) after three months from the date of registration of project. The student can appear for project examination after one year from the date of registration of project.

COMMUNICATION SKILLS & TECHNICAL WRITING

28 **The course on Communication Skills & Technical Writing** is compulsory for all students. However, the course does not contribute to the overall CGPA. A minimum of 50% marks individually in theory and oral test has to be obtained by the student at any time before the completion of his/her DiplETE. This course consists of theory and oral test. Accordingly, "PASS" or "FAIL" will be reflected in the Grade Sheet.

(a) **Theory :** This consists of written examination for 70 marks.

(b) **Oral Test :** consists of an Oral Test to test the Communication Skills which includes an oral presentation on any subject of the choice of students (e.g. About IETE, General knowledge topics etc). This presentation need not be on technical subjects. This test carries 30 marks.

EXEMPTIONS

29. Exemption may be granted in various papers (s) to the students who have passed similar subjects from elsewhere or other courses. Such exemptions are granted to a candidate passing the subject and successfully completing the course/curriculum from a recognized Institution/ Colleges/Universities and approved by the IETE Council.

30 Candidates seeking exemption are required to submit the following documents along with the requisite fee:

(a) Application form for exemption.

(b) Certificate of the course/curriculum completed by the student duly attested.

(c) Mark sheet duly attested.

(d) Certified copy of syllabus from which the candidate has passed the course.

(e) Fee @ Rs. 400/- per subject for which exemption is sought.

31 Candidates are advised to apply for exemption, if required, at the earliest opportunity. All cases of exemptions are considered by the Academic Committee of the Institution. For all subjects where exemption are granted will be communicated to the students in the Mark sheet of the first examination after the exemption is sought as it generally takes three months to process an application for exemption. Exemption will generally be granted if the major portion of the syllabi matches with IETE syllabus. **THE DECISION OF THE ACADEMIC COMMITTEE WILL BE FINAL AND BINDING TO ALL CONCERNED. NO REPRESENTATION IN THIS RESPECT WILL BE ENTERTAINED. (For accepted list of exemptions refer to the website www.iete.org/www.iete.info.)**

AWARD OF DiplETE

32 Every Student member (SD) successfully completing Sections A&B subjects including lab examinations with project work and a course in Communication Skills & Technical Writing of DiplETE Examination as per regulations prescribed by the Council from time to time shall be eligible to become a member (DiplETE). On payment of requisite fee for membership, he/she will be awarded a certificate of having passed the DiplETE examination of the Institution and shall then be eligible for transfer to the class of DiplETE To

pass DipIETE Examination, a student is required to score a minimum grade of 'D' having a grade point of 4 for each subject and having an aggregate of 5 CGPA. However for Project and lab examination, he/she should get a minimum grade of C having a grade point of 5.

CGPA SYSTEM

33. CGPA System which is followed in IETE is given below :

(a) Subject wise conversion of % marks into grade and grade point are as under:-

Grade	Grade Point
A+	10
A	9
B+	8
B	7
C+	6
C	5
D	4
F, F+	Fail

(b) CGPA will be calculated as under only for the subjects where a student has passed:-

$$CGPA = \frac{C_1 G_1 + C_2 G_2 \text{------} + C_n G_n}{C_1 + C_2 + C_3 \text{------} C_n}$$

Where $G_1 G_2$ ------denote the grade point scored.

   $C_1 C_2$ ------denote the credits of subjects.

All theory Subjects & Labs Carry 4 Credits.
Project work Carries 8 Credits.

(c) The award of division/classification will be as under :-

(i)   CGPA of 9 or more   -   Distinction
(ii) CGPA 6.5 or more but less than 9   -   First Division
(iii) CGPA 5 or more but less than 6.5   -   Second Division
(iv) Less than 5   -   FAIL (No award will be given) .

(d) CGPA is converted into percentage with a multiplier of 9.5

EXAMINATION APPLICATION

34. Applications for appearing in any of the subjects of the DipIETE Examination must be made on the prescribed OMR Examination Form (enclosed) and accompanied by the requisite examination fee. The prescribed application form is given initially free of cost along with the prospectus and later on with the Admit card where a student has appeared for an examination. OMR Examination application form can also be obtained by the students by payment of Rs. 20/- from any IETE Centre or HQ IETE. No action will be taken on an incomplete application. Students are advised to ensure that they have filled all the columns and have enclosed relevant documents. Separate form is to be used for exemption. Generally, after the acceptance of examination form of the students, change of examination centre is not encouraged. However in exceptional cases, change of exam Centre will be allowed with an additional charge of Rs. 200/-. For any correction in the examination form after processing and additional amount of Rs 200/- will be charged as reprocessing fee.

Note : Change of streams will be allowed with an additional charge of Rs. 600/-.

EXAMINATION FEE

35. Students are to submit their Examination Application form along with the fee as given below. The fee may get revised from time to time and the students are required to submit their application form along with the latest fee structure in force. The present fee structure is given below:

		In India (Rs)	Abroad (US $)	Remarks
(a)	Theory papers/per subject	400.00	80.00	To be deposited along with
(b)	Exemption/per subject	400.00	80.00	exam application form.
(c)	Written Test on Communication Skills & Technical Writing	400.00	80.00	
(d)	Project work	1100.00	200.00	To be deposited at
(e)	Each Lab Examination	400.00	80.00	respective IETE Centre
(f)	Oral Test on Communication Skills & Technical Writing	400.00	80.00	

Note: **(a) Fees will be charged per subject irrespective of whether it is for improvement OR re-appearance OR remaining paper OR additional paper OR exemption.**

(b) Examination fees once paid are neither refundable nor transferable to a subsequent examination.

(c) Enrolment Form, Examination Form and Exemption Form are to be sent separately with requisite fee along with each form.

LAST DATE FOR RECEIPT OF EXAMINATION APPLICATION

36 The last date for receipt of examination form duly filled in at the IETE HQ office for June/Dec examination respectively are as under:-

- Without late fee   25 Apr/25 Oct

- With late fee (of Rs.500/-)   5 May/5 Nov.

- With late fee (of Rs.750/-)   10 May/10 Nov.

Note: Application received after these dates will not be considered

DATE SHEET

37. The examinations are held twice a year from 15th June and 15th December and are conducted on all days including holidays and Sundays. The sequence of the papers of ET stream is given at **Appendix 'I'**. These dates are fixed and changes if any, will be notified to students along with admit cards and through our website **www.iete.org/www.iete.info** and at the IETE centre.

ADMIT CARD

38. Admit Cards will be sent to all the students to reach them by about 05th of June/December. Admit Cards of eligible students will also be available on our Websites www.iete.org/www.iete.info and can be

www.iete.org/www.iete.info and can be downloaded. Students will be allowed to appear for examination with these downloaded admit card along with their identity card. In the case of non-receipt of Admit-Card by above dates or the admit card not available on the website, the student must approach the concerned Examination Centre or IETE HQ and obtain permission to appear in the examination No complaint in respect of non-receipt of Admit Card will be entertained once the Examination is over **A student is required to carry his IETE Identity Card and Admit Card issued by IETE for appearing in examination.**

EXAMINATION CENTRES

41   At present the Examination are conducted at the following Centres . -

  (a)   In India:

Centre	Code	Centre	Code	Centre	Code
AHMEDABAD	01	HYDERABAD	08	NOIDA	38
ALIGARH	24	IMPHAL	31	PALAKKAD	41
ALLAHABAD	25	JABALPUR	23	PATNA	46
AMRAVATI	53	JAIPUR	09	PILANI	30
AURANGABAD	43	JAMMU	35	PUNE	14
BANGALORE	02	KANPUR	10	RAIPUR	51
BHOPAL	36	KOCHI	32	RAJKOT	44
BHUBANESWAR	27	KOLKATA	04	RANCHI	48
CHANDIGARH	05	KOZIKODE	52	SHIMLA	45
CHENNAI	12	LUCKNOW	11	TRIVANDRUM	16
COIMBATORE	47	MANKAPUR	28	VADODARA	42
DEHRADUN	26	MHOW	40	VARANASI	13
DELHI	06	MUMBAI	03	VIJAYAWADA	15
DHARWAD	49	MYSORE	33	VISAKHAPATNAM	34
GUWAHATI	07	NAGPUR	37		
GWALIOR	50	NASHIK	39		

  (b)   Abroad:

Centre	Code
ABU DHABI	17
KATHMANDU	19

USE OF UNFAIR MEANS

42.   If a student is found to have resorted to or made attempt to use **Unfair Means**, the Examination Superintendent/Invigilator has absolute powers to expel the candidate from the examination hall, if in his/her opinion the student has adopted unfair means. The Council/Board of Examination may take necessary disciplinary action against the

disciplinary action against the candidate which may consist of punishment(s) extending from cancellation of the paper(s) to debarring from future examinations as well as expulsion from IETE

RESULTS

41 Results of the examinations will be announced on or before 25th March and 25th September for December & June examinations respectively and communicated to the candidates through Result Sheets separately. Results will be available on IETE Websites (www.iete.org/www.iete.info/www.iete-elan.ac.in).

RECOUNTING

42. It may be noted that there is **no provision of re-evaluation** of answer books. Therefore request for re-evaluation are out rightly rejected

43 Recounting of scores, if requested, can be done by paying Rs 200/- (US$40) for students from abroad per subject. Requests for recounting of scores must be received at IETE HQ within 30 days from the date of announcement of results on **a separate application**.

IMPROVEMENT OF GRADES

44 A student who has passed in a subject may appear for improvement. He may take any number of chances irrespective of Grades previously obtained. If the student secures lower Grade than already secured, the original grade will hold good. Fee for improvement is Rs 400/- per paper. However, **no improvement is permitted in DipIETE Lab examination and project work**. Improvement is also allowed after completion of the examinations. After completion, students are required to give an Undertaking that they want/do not want to appear in any subject for improvement. Provisional Certificate/Certificate/Final Grade Sheet will be issued only after receipt of undertaking that no improvements are required and the payment of membership fee.

IETE MEANS-CUM-MERIT SCHOLARSHIP SCHEME FOR DipIETE STUDENTS

45 IETE has instituted IETE Means-Cum-Merit Scholarship scheme for DipIETE students from the year 2010. The scheme envisages award of 50 annual scholarships for DipIETE economical weaker and meritorious students. The amount of scholarship will be Rs.5000/- per student in a year. The details of the scheme are available on IETE website http://www.iete.org freely accessible and application form freely downloadable.

AWARDS FOR ACADEMIC EXCELLENCE

46 Six awards have been instituted to give incentive to student members for high level of performance in the DipIETE Examinations. Details of awards are listed at **Appendix 'J'**

LEGAL MATTERS

47 Adjudication in respect of legal cases concerning IETE HQ will be as per Bye-law 95 of the Institution which is reproduced below. -

"All Legal cases concerning IETE HQ shall lie within the jurisdiction of Delhi courts only"

AFFILIATION/ACCREDITATION

50   The Institution of Electronics & Telecommunication Engineers (IETE) neither recognises nor accepts affiliations of any private coaching Institute. Students in the past have reported that some private institution claim that they run classes/coaching on behalf of IETE. It is reiterated that IETE does not authorise any private institution to run classes on behalf of IETE. Therefore IETE is not responsible for such Private Coaching Institutes.

CORRESPONDENCE WITH IETE HQ

51   Important announcements concerning students and examinations will be available on the website www.iete.org and are also published in IETE Journal of Education which is issued six monthly (January – June and July - December) to the AMIETE Student members who have paid their subscriptions to date. For other facilities like participation in technical lectures, symposia etc. nearest IETE Centre/Sub-Centre (Address given in **Appendix-'J'**) may be contacted. All correspondence must be addressed to the Secretary General of the Institution (by designation and not by name). Remittances shall be made by way of crossed Bank Draft only. Bank drafts should be drawn in favour of Secretary General , IETE, New Delhi payable at New Delhi. Cash is accepted by hand at Accounts Section at IETE HQ only. Whenever depositing fee by cash, students must obtain receipt and attach photocopy of the same alongwith application. MONEY ORDER WILL NOT BE ACCEPTED All payment of fees can also be made on-line. For details refer our website www.iete.org.

CHANGE OF ADDRESS

52   **Students are advised to intimate their change of address to IETE HQ immediately, quoting their Membership Number, complete address with Pin Code.**

53.   Students are advised to provide their e-mail ID, telephone no and mobile no with their latest address in all correspondence.

MISCELLANEOUS INFORMATION

54   More miscellaneous information is given in **Appendix-'K'**.

- Acknowledgement for receipt of enrollment forms and declaration of exam results are given through SMS and Web.

- All student related information is displayed on web site **www.iete.org** and http://iete-elan.ac.in

- Students are advised to visit our web site regularly.

- **All payment of fees can also be made on-line. For details refer our website www.iete.org.**

Course Curriculum for the Programme of DIPIETE in Electronics & Telecommunication

SECTION A

		Part - I						Part - II		
SI No	Sub Code	Title	Theory	Practicals		SI No	Sub Code	Title	Theory	Practicals
			Examination Credits						**Examination Credits**	
1	DE51	Engineering Mathematics - I *	4	-		1	DE55	Engineering Mathematics – II *	4	-
2	DE52	Fundamentals of Electrical & Electronics *	4	-		2	DE56	Analog Electronics	4	-
3	DE53	Computer Fundamentals & C Programming *	4	-		3	DE57	Networks & Transmission Lines	4	-
4	DE54	Engineering Materials	4	-		4	DE58	Logic Design *	4	-
5	DE91	C Programming Lab	-	4		5	DE92	Analog Electronics Lab	-	4
		Total Credits	16	4				**Total Credits**	16	4

All the students have to pass a course in "Communication Skills & Technical Writing" which will not be counted for the overall percentage

SECTION B

		Part - I						Part - II		
SI No	Sub Code	Title	Theory	Practicals		SI No	Sub Code	Title	Theory	Practicals
			Examination Credits						**Examination Credits**	
1	DE59	Electronic Instrumentation & Measurements	4	-		1	DE63	Digital Communications	4	-
2	DE60	Microprocessors & Microcontrollers	4	-		2		Elective – I	4	-
3	DE61	Analog Communications	4	-		3		Elective – II	4	-
4	DE62	Telecommunication Switching Systems	4	-		4	DE94	Analog & Digital Communications Lab	-	4
5	DE93	Logic Design Lab	-	4		5	DE64	Project Work	-	8
		Total Credits	16	4				**Total Credits**	12	12

1	DE99	Communication Skill & Technical Writing

For Electives I & II, students can chose any two of the following elective subjects

SI No	Sub Code	Title
1	DE65	Control Engineering
2	DE66	Wireless & Mobile Communications
3	DE67	Embedded Systems *
4	DE68	Television Engineering
5	DE69	Data Communication & Networks **
6	DE70	Object Oriented Programming with C++ **
7	DE71	Power Electronics

NOTE: * Subjects common to ET / CS Streams
    ** Syllabus is same as that of the core subject for DIPIETE (CS)

OUTLINE SYLLABUS
DIPIETE (ELECTRONICS & TELECOMMUNICATION)

DE51   ENGINEERING MATHEMATICS – I
- Differential Calculus
- Integral Calculus
- Linear Algebra
- Differential Equations
- Algebra
- Trigonometry
- Coordinate Geometry

DE52   FUNDAMENTALS OF ELECTRICAL AND ELECTRONICS
- Electromagnetism
- DC Circuits and AC Circuits
- DC Motor
- Transformer and Induction Motor
- Basic Semiconductor and PN Junctions
- Semiconductor Diodes
- Diode Applications
- Bipolar Junction Transistor
- BJT Biasing
- Amplifiers and Oscillators

DE53   COMPUTER FUNDAMENTALS & C PROGRAMMING
- Computer Basics
- Data Representation
- Input / Output Units
- Computer Languages
- Operating Systems
- Microcomputers
- Computer Networks
- Constants, Variables And Data Types
- Operators And Expressions
- Managing Input And Output Operations
- Decision Making And Branching
- Decision Making And Looping
- Arrays
- User – Defined Functions
- Pointers
- File Management

DE54   ENGINEERING MATERIALS
- Conducting Materials
- Dielectric Materials in Static Fields
- Dielectric Materials in Alternating Fields
- Magnetic Materials
- Semi conducting Materials
- Semi conducting Devices
- Electronic Component Materials
- Fabrication of Semi conductors

DE91   C PROGRAMMING LAB

DE55   ENGINEERING MATHEMATICS – II
- Differential calculus
- Integral calculus
- Complex numbers
- Vector algebra
- Linear differential equation of higher order
- Laplace transform
- Fourier series

DE56   ANALOG ELECTRONICS
- Integrated Circuit Fabrication
- AC Analysis of BJT Circuits
- Field Effect Transistors
- Audio Power Amplifiers
- Optoelectronic Devices
- Operational Amplifier
- Operational Amplifier Characteristics
- Operational Amplifier Applications
- Comparators and Waveform Generators
- Voltage Regulators; DAC and ADC

DE57   NETWORKS AND TRANSMISSION LINES
- Basic Concepts
- Laplace Transforms and Signal Functions
- Network Theorems
- Network Functions and Parameters
- Resonance Circuits and Selectivity
- Transmission Lines
- Transmission Lines at Radio Frequencies
- Filters and Attenuators

DE58   LOGIC DESIGN
- Introductory Concepts
- Number Systems and Codes
- Describing Logic Circuits
- Combinational Logic Circuits
- Flip-Flops and Applications
- Digital Arithmetic Operations and Circuits
- Counters and Registers
- MSI Logic Circuits
- Synchronous Counter Design
- Memory Devices

DE92   ANALOG ELECTRONICS LAB

DE59   ELECTRONIC INSTRUMENTATION AND MEASUREMENTS
- Measurement Fundamentals
- Measurement of Resistance, Inductance and capacitance
- Instruments to measure Current and Voltages
- Digital measuring Instruments
- Signal Generators and Oscilloscope
- Signal Analysis Instruments and R.F Power measurement Techniques
- Recorders
- Transducers and Data Acquisition System

DE60   MICORPROCESSORS & MICROCONTROLLERS
- Evolution of Microprocessors
- Fundamentals of a Computer
- Number Representation
- Fundamentals of Microprocessor
- First Assembly Language Program
- Instruction set of 8085
- Chip select logic
- Addressing of I/O ports
- Architecture of 8085
- Assembly language programs
- Use of PC in writing and executing 8085 programs
- Interrupts in 8085
- 8255 Programmable peripheral interface chip
- Programs using interface modules
- Interfacing of I/O devices
- Intel 8259A, 8257, 8253, 8251A
- Intel 8051 microcontroller

DE61   ANALOG COMMUNICATIONS
- Introduction to Communication Systems
- Noise
- Amplitude Modulation
- Single-Sideband Techniques
- Frequency Modulation
- Radio Receivers
- Antennas
- Radiation and Propagation of Waves
- Waveguides, Resonators and Components
- Pulse Communications
- Broadband Communications Systems

DE62   TELECOMMUNICATION SWITCHING SYSTEMS
- Switching Systems
- Telecommunications Traffic
- Switching Networks

- Time Division Switching
- Control of Switching Systems
- Signaling
- Packet Switching
- Networks

DE93   LOGIC DESIGN LAB

DE63   DIGITAL COMMUNICATIONS
- Introduction
- Fundamental Limits On Performance
- Sampling Process
- Waveform Coding Techniques
- Base-Band Shaping For Data Transmission
- Digital Modulation Techniques
- Detection And Estimation
- Spread Spectrum Modulation
- Applications

DE65   CONTROL ENGINEERING
- Introduction
- Control Systems Terminology
- Differential Equations and Linear Systems
- Laplace Transform Applications
- Stability
- Transfer Functions
- Block-Diagram Algebra
- Signal Flow Graphs
- System Sensitivity & Classification
- Analysis and Design: Objectives and Methods
- Nyquist Analysis
- Root-Locus Analysis
- Bode Analysis

DE66   WIRELESS & MOBILE COMMUNICATIONS
- Introduction
- Mobile Radio Propagation
- Channel Coding and Error Control
- Cellular Concept
- Multiple Radio Access
- Multiple Division Techniques
- Channel Allocation
- Satellite Systems
- Mobile Communication Systems
- Existing Wireless Systems
- Ad Hoc and Sensor Networks
- Wireless MANs, LANs and PANs
- Recent Advances

DE67   EMBEDDED SYSTEMS
- Introduction to embedded systems
- Custom single purpose processors: Hardware
- General purpose processors: Software

- Standard single-purpose processors: Peripherals
- Memory
- Interfacing
- Introduction to Real Time Operating Systems
- Case studies of programming with RTOS

DE68   TELEVISION ENGINEERING
- Applications of Television
- Television Picture
- Video Cameras and Camcorders
- Picture Tubes
- Scanning & Synchronizing
- Colour TV circuits and signals
- Video test signals
- TV Receiver Signal Circuits
- Television and Video servicing

DE69   DATA COMMUNICATION & NETWORKS
- Data Communications, Data Networking, and the Internet
- Protocol Architecture, TCP/IP, and Internet-Based Applications
- Data Transmission
- Transmission Media
- Signal Encoding Techniques
- Digital Data Communication Techniques
- Data Link Control Protocols
- Multiplexing
- Circuit Switching and Packet Switching
- Routing in Switched Networks
- Congestion Control in Data Networks
- Local Area Network Overview
- High-Speed LANs
- Wireless LANs
- Inter network Protocols
- Inter network Operation
- Transport Protocols

DE70   OBJECT ORIENTED PROGRAMMING WITH C++
- Object-oriented Programming Concepts
- Language Constructs
- Advanced Constructs
- Classes in C++
- Member Functions
- Operator Overloading
- Constructors and Destructors
- Inheritance
- Multiple Inheritance
- Polymorphism
- Handling Exceptions
- Templates
- C++ I/O

DE71   POWER ELECTRONICS
- Power Electronics
- Power Diodes
- Power Transistors
- Thyristor Devices
- Single-Phase Controlled Rectifiers
- Three-Phase Controlled Rectifiers
- DC Choppers
- Inverters
- AC Voltage Controller
- Static Switches

DE94   ANALOG & DIGITAL COMMUNICATIONS LAB

DE64   PROJECT WORK

DE99   COMMUNICATION SKILLS AND TECHNICAL WRITING
- Communication: Its Types and Significance
- Grammar
- Syntax
- Reading Skills
- Writing Skills
- Listening Skills
- Technical Report
- Speaking Skills
- Self Development

DIPIETE (ET)
STREAMWISE DETAILED SYLLABUS

Introduction

Most of the Student Members of the IETE are working engineers/ technicians/science graduates or under graduates. Thus, due to occupational reasons and other factors these students are deprived of a formal education and therefore have to learn the subjects through self-study only.

Review of Syllabus

2.   IETE periodically reviews the syllabi of DIPIETE and the aim of these reviews is not only to renovate and modernize the contents but also to make them contemporary. The syllabi for both Electronics & Telecommunications (ET) and Computer Science & Engineering (CS) streams have been reviewed recently.

3.   Keeping the above aspects in view and based on feed backs/suggestions received from the students, this syllabus has been formulated to meet the following criteria:-
- The Syllabus should cater to the technological advancements.
- The textbooks should be available and affordable to the students.
- In the absence of a formal coaching to the students, there should be a reasonable correlation between the topics in a subject and the textbooks.

Salient Features

4.   Some salient features of the syllabus are:-
- Each subject has a code preceding it (viz DE51 and DC51 are codes for Mathematics-I in ET & CS streams respectively).
- In order to guide the student and to enable him/her to prepare well for an examination, each subject is divided into 8 units and each unit has the course contents to be covered in 7 or 8 hours.
- The textbooks have been numbered in Roman Numerical (viz I, II, III)
- The chapters and sections are mentioned inside the bracket e.g. I (2.1) would indicates chapter 2 and section 1 of textbook-I.

Scheme of the Examination

5.   For all theory subjects the Question Paper contains
- 10 objective questions for 20 marks covering the complete syllabus
- 8 questions are from each unit and each question carries 16 marks.

6.   Regular feed back from the students, academicians, corporate members and professionals is requested to keep this syllabus updated, so that our students keep abreast of latest technological changes. Though every effort has been made to identify standard and best textbooks for each subject, we welcome suggestions on availability of better and cheaper textbooks.

DE51   **ENGINEERING MATHEMATICS – I**

UNIT I
DIFFERENTIAL CALCULUS   **08 hrs**

Limits; Left hand and Right hand Limits; Continuity of functions; Evaluation of simple limits; Differentiability of a Function; Geometrical Meaning of derivative; Standard Results; Logarithmic Differentiation; Differentiation of Implicit function; Parametric Equations; Successive differentiation; Calculation of nth derivative of standard functions; Leibnitz theorem for the nth derivative of the product of two functions; Applications of differentiation – Tangents and Normals; Increasing and Decreasing functions; Maxima and Minima.
III (1.6, 1.8, 1.9, 1.10, 2.3, 2.25, 2.26, 2.27, 2.30, 2.31, 2.37, 3.1, 4.1, 4.2)

UNIT II
INTEGRAL CALCULUS   **07 hrs**

Introduction; Definitions; Hyperbolic functions; Standard results – Indefinite Integrals; Integration by the Method of Substitution; Standard formula; Integration by parts; Integration by Partial Fraction Method; Integration of Irrational Functions; Integration of Trignometric functions; Definite Integrals - Introduction; Theorems on Definite Integrals.
III (21.1, 21.2, 21.4, 21.5, 22.1, 22.2, 23.1, 24.1, to 24.7, 25. 1 to 25.6, 26.1 to 26.3, 28.1, 28.2)

UNIT III
LINEAR ALGEBRA   **08 hrs**

Introduction; Determinants; Minors and Cofactors; Properties of Determinants; Laplace's Expansion of a Determinant; Solutions of Simultaneous Linear Equations by Determinants (Cramer's Rule); Rule for Multiplication of two Determinants; Matrices – Types of Matrices; Matrix Multiplication; Properties of Matrix Multiplication; Adjoint of a Square Matrix; Inverse of a Matrix by using Adjoint of a Matrix; Solutions of Simultaneous Equations; Elementary transformation; Elementary Matrices; Rank of a Matrix; Types, Consistency and Solutions of system of Linear equations.
I (2.1, 2.2, 2.4, 2.5, 2.7, 2.12, 2.13, 2.14, 3.1, 3.2, 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, 3.12, 3.13, 3.16to 3.19)

UNIT IV
DIFFERENTIAL EQUATIONS   **07 hrs**

Definition of Differential Equation; Order and Degree of a Differential Equation; Formation of Differential Equation; Solution of First order and First Degree Differential Equation; Solution by the Method of Variable Separable;   Homogeneous Differential Equation; Reducible to Homogeneous Differential Equation; Linear Differential Equation of 1st Order; Equations Reducible to Linear Form; Linear Differential Equation in x; Exact Differential Equation; Equations Reducible to Exact Equations; Simple Electric Circuits.
I (7.1 to 7.14)

UNIT V
ALGEBRA   **07 hrs**

Principles of Mathematical Induction; Permutation and Combinations; Binomial Theorem (for positive integral index); Arithmetic Progressions; Geometric Progressions.
II (Unit II Chapters 14, 18, 19, 20, 21, 22)

UNIT VI
TRIGONOMETRY   **07 hrs**

Introduction; Measurement of Angles; Trigonometric ratios; Trigonometric functions; Trigonometric functions of Sum and Difference of two angles; Transformation Formulae; Trigonometric functions of Multiple and sub-multiple angles; Conditional Identities and Equations; Graphs of Trignometric Functions; Trignometric Equations; Relations between the Sides and the Trignometric Ratios of the Angles of a Triangle.
II (Unit I Chapters 4, 5, 6, 7, 8, 9, 10, 11, 12)

UNIT VII

CO-ORDINATE GEOMETRY   **08 hrs**

Co-ordinates; Conversion of Cartesian Co-ordinates into Polar Co-ordinates and vice versa; Distance between Two Points; Ratio formula for internal and external division (No proof); Concurrency of the Medians of a Triangle; Concurrency of the bisectors of the angles of a triangle; Area of a triangle; Straight lines; Slope of a line; Intercepts; Different forms of equation to a straight line; Line through two points; intersection of straight lines; Line through intersection of two given lines; Angle between two lines; Condition for Parallelism and Perpendicularity; Length of perpendicular.

I (4.1, 4.2, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10, 4.11, 4.12, 4.13, 4.14, 4.15, 4.16, 4.17, 4.18, 4.19, 4.20, 4.21, 4.23)

UNIT VIII

CO-ORDINATE GEOMETRY (CONTINUED)   **08 hrs**

Circle - Definition; Standard Form; Central Form; General equation of a circle; General Form; Conditions for the equation of a Circle; Circle through three given points; Diameter form; Conic; Geometrical definition of a conic; Parabola; Ellipse; Hyperbola; Finding equations of conic when its focus, directrix and vertex are given.

I (4.25, 4.26, 4.27, 4.28, 4.29, 4.30, 4.31, 4.32, 4.33, 4.34, 4.36, 4.38)

Text Books:

I. Applied Mathematics for Polytechnics, H. K. Dass, 8th Edition, CBS Publishers & Distributors.
II. A Text book of Comprehensive Mathematics Class XI, Parmanand Gupta, Laxmi Publications (P) Ltd, New Delhi.
III. Engineering Mathematics, H. K. Dass, S, Chand and Company Ltd, 13th Edition, New Delhi.

Reference Book:

1. Higher Engineering Mathematics, B. S. Grewal, 40th Edition, Khanna Publishers, Delhi.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE52 **FUNDAMENTALS OF ELECTRICAL AND ELECTRONICS**

PART A: FUNDAMETALS OF ELECTRICAL ENGINEERING
UNIT I
ELECTROMAGNETISM **07 hrs**

Coulomb's Law of Electrostatics; Capacitor Charging and Discharging; Magnetic Field; Force on Current Carrying Conductor in a Magnetic Field; MMF; Magnetic Field Strength; Reluctance; Laws of Magnetic Circuits; Calculation of Ampere-Turns; Magnetization Curve; Comparison of Electric and Magnetic Circuits; Faraday's Law; Statically Induced EMF.
I (2.3, 2.8, 2.9, 3.2, 3.9, 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 5.2, 5.6)

UNIT II
DC CIRCUITS AND AC CIRCUITS **08 hrs**

Ohm's Law; Kirchoff's Laws; Superposition Theorem; Thevenin's Theorem; Norton's Theorem; Production of AC Voltage; RMS Value; Phasor Representation; Steady State Analysis of R, L, C, RL, RC, RLC circuits; Power in AC Circuits; Generation of Three Phase EMF; Phase Sequence; Star and Delta Connection; Relationship Between Line and Phase Quantities; Power in Three Phase System.
I (1.5, 1.6, 1.8, 1.9, 1.10, 6.2, 6.4, 6.9, 6.12, 6.13, 6.14, 7.2, 7.3, 7.4, 7.5, 9.2, 9.3, 9.5, 9.6, 9.7, 9.8, 9.9)

UNIT III
DC MOTOR **08 hrs**

Principle of Operation; Construction; EMF Equation; Types of DC Motor (Shunt and Series Motor); Torque Equation; Motor Characteristic Curves; Necessity of Starter; Speed Control of Shunt Motor-Armature Control and Field Control.
I (17.3, 17.4, 17.6, 17.9, 19.2, 19.4, 19.5, 19.6)

UNIT IV
TRANSFORMER AND INDUCTION MOTOR **07 hrs**

Transformer: Principle of Operation; EMF Equation of Transformer; Three Phase Induction Motor: Construction; Rotating Magnetic Field; Principle of Operation; Slip.
I (14.3, 14.6, 23.2, 23.3, 23.4, 23.8)

PART B: FUNDAMETALS OF ELECTRONICS

UNIT V
BASIC SEMICONDUCTOR AND PN JUNCTION THEORY **04 hrs**

Introduction; Atomic Theory; Conduction in Solids; Conductors, Semiconductors and Insulators; n-type and p-type Semiconductors; The p-n Junction; Biased Junctions.
II (1.1, 1.2, 1.3, 1.4, 1.5, 1.6)

SEMICONDUCTOR DIODES **04 hrs**

Introduction; p-n Junction Diode; Characteristics and Parameters; Diode Approximations; DC Load Line Analysis; Temperature Effects; AC Equivalent Circuits; Zener Diodes.
II (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.9)

UNIT VI
DIODE APPLICATIONS **07 hrs**

Introduction; Half Wave Rectification; Full Wave Rectification; Half Wave Rectifier DC Power Supply; Full Wave Rectifier DC Power Supply; Power Supply Performance; Zener Diode Voltage Regulators; Series Clipping Circuits; Shunt Clipping Circuits; Clamping Circuits; DC Voltage Multiplexers.
II (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10)

UNIT VII

BIPOLAR JUNCTION TRANSISTORS   **04 hrs**

Transistor Operation; Transistor Voltages and Currents; Amplification; Common Base Characteristics; Common Emitter and Common Collector Characteristics.
II   (4.1, 4.2, 4.3, 4.4, 4.5, 4.6)

BJT BIASING   **04 hrs**

DC Load Line and Bias Point Base Bias; Collector to Base Bias; Voltage Divider Bias; Comparison of Basic Bias Circuits; Bias Circuit Design; Thermal Stability of Bias Circuits (Qualitative Discussions Only).
II   (5.1, 5.2, 5.3, 5.4, 5.5, 5.7, 5.9)

UNIT VIII

AMPLIFIERS AND OSCILLATORS   **07 hrs**

Decibels and Half Power Points; Single Stage CE Amplifier; Capacitor Coupled Two Stage CE Amplifier (Qualitative Discussions Only); Series Voltage Negative Feedback (Qualitative Discussions); Additional Effects of Negative Feedback (Qualitative); The BJT Phase Shift Oscillators; BJT Colpitts and Hartley Oscillator (Qualitative).
II   (8.2, 12.1, 12.3, 13.1, 13.7, 16.1, 16.2, 16.3)

Text Books:
 I. V.N. Mittle and Arvind Mittal, 'Basic Electrical Engineering', Tata McGraw-Hill Publishing Company Limited, 2nd edition, 2006.
II. Electronic Devices and Circuits, David A Bell, Fourth Edition, PHI (2006).

Reference Books:
1. D.P. Kothari and I.J. Nagrath, 'Basic Electrical Engineering', Tata McGraw-Hill Publishing Company Limited, 2nd edition, 2002.
2. I.J. Nagrath and D.P. Kothari, 'Electric Machines', Tata McGraw-Hill Publishing Company Limited.
3. Electronic Devices and Circuits, I.J. Nagrath, PHI, 2007.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks, selecting atleast **TWO** questions from each part.

DE53 **COMPUTER FUNDAMENTALS & C PROGRAMMING**

PART A: COMPUTER FUNDAMENTALS
UNIT I
COMPUTER BASICS

07 hrs

Algorithms, A Simple Model of a Computer, Characteristics of Computers, Problem Solving Using Computers

DATA REPRESENTATION
Representation of Characters in Computers, Representation of Integers, Representation of Fractions, Hexadecimal Representation of Numbers, Decimal to Binary Conversion, Error Detecting Codes.
I (1, 2)

UNIT II
INPUT / OUTPUT UNITS **08 hrs**
Description of Computer Input Units, Other Input Methods, Computer Output Units

COMPUTER LANGUAGES
Why Programming Language? Assembly Language, Higher Level Programming Languages, Compiling High Level Language Program, Some High Level Languages

OPERATING SYSTEMS
Why Do We Need an Operating System? Personal Computer Operating System, The Unix Operating System
I (3, 9, 10.1, 10.5, 10.6)

UNIT III

MICROCOMPUTERS **07 hrs**
An Ideal Microcomputer, An Actual Microcomputer, Memory Systems for Microcomputers, A Minimum Microcomputer Configuration, Evolution of Microcomputers

COMPUTER NETWORKS
Need for Computer Communication Networks, Internet and the World Wide Web, Local Area Networks
I (11.1to 11.4, 14.1, 14.2, 14.4)

PART B: C PROGRAMMING

UNIT IV
CONSTANTS, VARIABLES AND DATA TYPES

08 hrs

Introduction, Characters set, C tokens, Keywords and Identifiers, Constants, Variables, Data types, Declaration of variables

OPERATORS AND EXPRESSIONS
Arithmetic operators, Relational operators, Logical operators, Assignment operators, Increment and Decrement operators, Conditional operator, Bit wise operators, Special operators, Arithmetic expressions, Evaluation of expressions, Precedence of Arithmetic operators, Type conversions in expressions, Operator precedence and associativity

MANAGING INPUT AND OUTPUT OPERATIONS
Introduction, Reading a character, Writing a character, Formatted Input, Formatted Output
II (2.1 to 2.8, 3.2 to 3.12, 3.14, 3.15, 4)

UNIT V

DECISION MAKING AND BRANCHING   **07 hrs**

Introduction, Decision making with *if* statement, Simple *if* statement, The *if… else* statement, Nesting of *if…. else* statements, The *else….if* ladder, The *switch* statement, The?: operator, The *Goto* statement

DECISION MAKING AND LOOPING

Introduction, The *while* statement, The *do* statement, The *for* statement, Jumps in Loops.
II (5, 6)

UNIT VI

ARRAYS   **08 hrs**

Introduction, One – dimensional Arrays, Declaration of one – dimensional Arrays, Initialization of one – dimensional Arrays, Two – dimensional Arrays, Initializing two – dimensional Arrays.

CHARACTER ARRAYS AND STRINGS

Introduction, Declaring and Initializing String Variables, Reading Strings from Terminal, Writing Strings to Screen, Putting Strings together, Comparison of Two Strings, String-handling Functions
II (7.1 to 7.6, 8.1 to 8.4, 8.6, 8.7, 8.8)

UNIT VII

USER – DEFINED FUNCTIONS   **07 hrs**

Introduction, Need for User – defined Functions, A multi – function program, Elements of User defined Functions, Definition of Functions, Return Values and their Types, Function Calls, Function Declaration, Category of Functions, No Arguments and no Return Values, Arguments but no Return Values, Arguments with Return Values, No Argument but Returns a Value, Functions that Return Multiple Values.
II (9.1 to 9.14)

UNIT VIII

POINTERS   **08 hrs**

Introduction, Understanding Pointers, Accessing the Address of a Variable, Declaring Pointer Variables, Initialization of Pointer Variables, Accessing a Variable through its Pointer, Chain of Pointers, Pointer Expressions, Pointer Increments and Scale Factor, Pointer and Arrays, Pointers and Character Strings, Array of Pointers.

FILE MANAGEMENT

Introduction, Defining and Opening a File, Closing a File, Input/Output Operations on Files
II (11.1 to 11.12, 12.1 to 12.4)

Text Books:
I.   Fundamentals of Computers, V. Rajaraman, Fourth Edition, PHI, 2007
II. Programming in ANSI C, E. Balagurusamy, Third Edition, Tata McGraw Hill

Reference Book:
1. Computer Science – A Structured Programming Approach Using C, Behrouz A. Forouzan, Richard F. Gilberg, Second Edition, Thomson Learning.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks, selecting **TWO** questions from Part A and **THREE** from Part B.

DE54   **ENGINEERING MATERIALS**

UNIT I
CONDUCTING MATERIALS   **08 hrs**
Introduction; Factors Affecting the Resistivity of Electrical Materials; The Electron Gas Model of Metal; Motion of Electron in Electric Field; Equation of Motion of an Electron; Current Carried by Electrons; Mobility; Energy Levels of a Molecule; Fermi Energy; Fermi-Dirac Distribution; Emission of Electrons from Metals-Thermionic, Photoelectric, Field and Secondary Emissions; Contact Potential, Effect of Temperature on Electrical Conductivity of Metals; Superconductivity; Electrical Conducting Materials; Thermo-Electric Effects; Operation of Thermocouple.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, .9, 3.14, 3.15)

UNIT II
DIELECTRIC MATERIALS IN STATIC FIELDS   **07 hrs**
Introduction, Effect of a Dielectric on the Behavior of a Capacitor; Polarization; Dielectric Constant of Monatomic Gases; Polarization Mechanisms-Electronic, Ionic and Dipolar polarization; Internal Fields in Solids and Liquids-Lorentz field; Clausius-Mosotti Relation; Polarisability Catastrophe.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III
DIELECTRIC MATERIALS IN ALTERNATING FIELDS   **08 hrs**
Introduction; Frequency Dependence of Electronic Polarizability; Frequency Dependence of Permittivity; Ionic Polarizability; Dielectric Losses and Loss Tangent; Dipolar Relaxation; Frequency and Temperature Dependence of Dielectric Constant of Polar Dieletrics; Dielectric Properties of Polymeric Systems; Ionic Conductivity in Insulators; Insulating Materials; Breakdown in Gaseous, Liquid and Solid Dielectric Materials; Important Requirements of Good Insulating Materials; Ferroelectricity; Piezoelectricity.
I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11, 5.12, 5.13)

UNIT IV
MAGNETIC MATERIALS   **08 hrs**
Introduction; Classification of Magnetic Materials; Origin of Permanent Magnetic Dipoles-Diamagnetism and Paramagnetism; Ferromagnetism-Origin and Ferromagnetic Domains; Magnetization and Hysteresis Loop; Magnetostriction; Factors Affecting Permeability and Hysteresis Loss; Common Magnetic Materials-Iron and Silicon Iron Alloys; Nickel-Iron Alloys and Permanent Magnet Materials and Design of Permanent Magnets; Anti-Ferromagnetism and Ferrimagnetism; Magnetic Resonance.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11, 6.12, 6.13, 6.14, 6.15, 6.16)

UNIT V
SEMICONDUCTING MATERIALS   **08 hrs**
Introduction; Energy Bands in Solids-Energy Bands in Conductors, Semiconductors   and Insulators; Types of Semiconductors-Energy Bands for n-type and p-type Semiconductor; Intrinsic Semiconductors; Impurity Type Semiconductor and Interaction of Semiconductor with Time-Dependent Fields.; Diffusion and Einstein Relation; Hall-effect-Hall Voltage; Hall Coefficient; Thermal Conductivity of Semiconductors; Electrical Conductivity of Doped Materials; Materials for Fabrication of Semiconductor Devices; Passive Materials Integral to Device-Metals; Capacitance Materials; Junction Coatings.
Device Potting; Packaging; Process Aids; Susceptor Materials; Reactor Envelopes; Plastics and Pump fluids; Solvents and Etchants.
I (7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.7, 7.8, 7.9, 7.10, 7.11, 7.12, 7.13)

UNIT VI

SEMICONDUCTING DEVICES   **07 hrs**

Metal-Semiconductor Contacts; P-N Junction; Barrier Capacitance; Breakdown Phenomena in Barrier Layer-Zener and Avalanche Breakdown; Junction Diodes-Zener, Varactor and Tunnel Diodes; Junction Transistor; Thermistors and Varistors; Semiconductor Materials-Silicon and Germanium; Silicon-Germanium Mixed Crystals; Silicon Carbide and Intermetallic Compounds; Silicon Controlled Rectifier-Two Transistor and Electromechanical Analogue.

I (8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8, 8.9)

UNIT VII

MATERIALS FOR ELECTRONIC COMPONENTS   **07 hrs**

Resistors-Carbon Composition; Insulated-Moulded; Film type; Cracked Carbon and Alloy Resistors; Metal-Oxide Film; Wire-Wound; High-Value; Non-Linear Resistors; Voltage-Sensitive; Non-Symmetrical and Variable Resistors; Capacitors-Paper, Mica, Ceramic, Glass-Dielectric, Vitreous-Enamel, Plastic, Electrolytic, Air-Dielectric and Variable Capacitors; Inductors-Air-Cored Coils; Laminated-Core; Powdered-Core and Ferrite-Core Inductors; Relays-Reed; Moving Coil; Induction; Thermal Type Relays; Electronic Valves; Function of Relays; Dry-Reed; Mercury-Wetted and Ferreed Relays.

I (12.1, 12.2, 12.3, 12.4, 12.5)

UNIT VIII

FABRICATION OF SEMICONDUCTORS   **07 hrs**

Fabrication Technology-Czochralski Method of Growing Single Crystal Semiconductor; Zone-Refining; Grown Junction and Alloyed Junction Processes-Alloyed Junction Diode and Gold-Bonded Diode; Diffused Junction Technique and Epitaxial Diffused Junction Diode; Fabrication of Junction Transistors-Grown Junction; Alloyed Junction Surface Barrier Alloyed Junction; Diffused Mesa; Planar Diffused and Epitaxial Planar Diffused Transistors; Field-Effect Devices-General Properties and Types; Drain and Transfer Characteristics of JFET.

I (14.1, 14.2, 14.3, 14.4, 14.5, 14.6, 14.7, 14.8, 14.9)

Text Book:

 I. Introduction to Electrical Engineering Materials by C.S. Indulkar and S. Thiruvengadam, 4th Edition, Reprint 2006 Edition, S. Chand and Company, New Delhi.

Reference Books:

1. Materials Science and Engineering, V. Raghavan, Prentice-Hall of India, New Delhi, 5th Edition, (Reprint April 2007)
2. Electronic Engineering Materials and Devices, John Allison, Tata McGraw Hill, New Delhi (1998)
3. Elements of Materials Science and Engineering, Lawrence H. Van Vlack, Pearson Education (6th Edition)

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE91   **C PROGRAMMING LAB**
List of Experiments
1. Write a C program to find and output the roots of a given quadratic equation with non-zero coefficients.
2. Write a C program to simulate a simple calculator that performs addition, subtraction, multiplication, and division of integers. Error should be reported, if any attempt is made to divide by zero.
3. Write a C program to generate and print the first N Fibonacci numbers.

4. Write a C program to find the GCD and LCM of two given integers, and output the results.

5. Write a C program to reverse a given four-digit number and check whether the number is a palindrome or not.

6. Write a C program to find whether a given integer is prime or not.

7. Write a C program to input N real numbers in ascending order into a single dimension array, conduct binary search for a given key number, and report success or failure.

8. Write a C program to sort a given set of N student names in alphabetical order.

9. Write a C program to evaluate the polynomial $f(x) = a_4x^4 + a_3x^3 + a_2x^2 + a_1x + a_0$ for a given value of x, and the coefficients using Horner's method.

10. Write a C program to read two matrices A (M x N) and B (P x Q), and compute the product of A.B after checking compatibility for multiplication.

11. Write C user defined functions
    a. to input N integer numbers into a single dimension array
    b. to conduct linear search
Using these functions write a C program to accept N integer numbers and a given key integer and conduct linear search.

12. Write C user defined functions
    a. to input N integer numbers into single dimension array
    b. to sort the integer numbers in ascending order using bubble sort technique
    c. to print the single dimension array elements
Using these functions, write a C program to input N integers numbers into a single-dimension array, sort them in ascending order, and print both the given array and the sorted array.

13. Write C user defined functions
    a. To input N real numbers into single dimension array
    b. to compute their mean
    c. to compute their variance
    d. to compute their standard deviation
Using these functions write a C program to input N real numbers into a single dimension array, compute their mean, variance, and standard deviation.

14. Write a C program to read a matrix A(M x N) and compute the following using user defined functions:
    a. Sum of the elements of the specified row
    b. Sum of the elements of the specified column
    c. Sum of all the elements of the matrix
15. Write a C program using pointers to read in an array of integers and print its elements in reverse order.
Note: Minimum of 13 experiments to be conducted.
• All the C programs to be executed using Turbo C or similar environment.

DE55   **ENGINEERING MATHEMATICS – II**

UNIT I
DIFFERENTIAL CALCULUS   **07 hrs**
Introduction to Limit continuity and differentiability of function; fundamental theorems of differential calculus; Rolle's theorem; Geometrical interpretation; Lagrange's Mean value theorem; Cauchy's Mean value theorem; Taylor's theorem for one variable (without proof); Maclaurin's series expansion; Indeterminate forms.
I (3.3, 3.3(1), 3.3(2), 3.3(3), 3.3(4), 3.4, 3.5)

UNIT II
INTEGRAL CALCULUS   **07 hrs**

Reduction formulae; Reduction formulae for $\int_{0}^{\pi/2} \sin^{n}(x)dx$, $\int_{0}^{\pi/2} \cos^{n}(x)dx$, $\int_{0}^{\pi/2} \sin^{m}(x)\cos^{n}(x)dx$;

Problems-Application of Integration ; Areas of Cartesian curves; Length of curves, Volumes of revolution; Surface area of revolution.
I (5.1, 5.2, 5.3, 5.9, 5.10, 5.11(1), 5.12)

UNIT III
COMPLEX NUMBERS   **08 hrs**
Introduction; Geometric representation of complex number (Argand diagram); Modulus and Argument of Complex number; conjugate of a Complex number; Addition; Subtraction of Complex numbers; Multiplication and Division of Complex numbers; Exponential and Circular functions of Complex variables; DeMovire's Theorem; Phasor; R and A.C Circuits; L and A.C Circuits; C and A.C. Circuits; Impedance; R-L in Parallel Circuit.
Reference 1 Chapter 10

UNIT IV
VECTOR ALGEBRA   **07 hrs**
Introduction to Vectors; Addition and Subtraction of Vectors; Properties of Addition of vectors; Rectangular resolution of a Vector; Position Vector of a point; Ratio formula; Product of two Vectors; Scalar or Dot product of two Vectors; Geometrical interpretation; Work done as a scalar product; Vector product or cross product; Geometrical interpretation; Moment of a force; Angular velocity; Scalar triple product; Geometrical interpretation; Condition for coplanarity; Vector triple product.
II (20.1 to 20.10 except 20.5, 20.10(2), 20.13, 20.14, 20.14 (2), 20.17 to 20.22)

UNIT V
LINEAR DIFFERENTIAL EQUATION OF HIGHER ORDER   **07 hrs**
Definition; General form; complete solution as C.F+P.I; Method of finding complimentary function; Method of finding particular integral for the functions
e^{ax} ; $\sin(ax+b)$; $\cos(ax+b)$; x^{m} ; $e^{ax}V$ $where$ $V = \sin(ax+b) or \cos(ax+b) or x^{m}$
Application of Linear Differential equation; Simple Harmonic motion; Simple pendulum; Oscillation of a spring; Oscillatory Electrical Circuits; Deflection of beams.
I (9.1, 9.2, 9.3, 9.4, 9.8, 9.9, 9.10, 9.11, 9.12)

UNIT VI
FOURIER SERIES   **08 hrs**
Introduction; Periodic functions; Dirchlet conditions; Euler's coefficients; Fourier Series expansion of Periodic functions of period 2π defined in (c, c $+2\pi$); Functions having points of discontinuity; change of interval; Even and odd functions; Half range series; Complex form of Fourier series; Practical Harmonic Analysis.
I (11.1 to 11.3, 11.4(1), 11.4(2), 11.5, 11.7, 11.8)

UNIT VII

LAPLACE TRANSFORMS   **08 hrs**

Introduction; Definition; Linearity property; Laplace transforms of standard functions; Shifting theorem of Laplace transform; change of scale property; Laplace transform of derivatives; Laplace transforms of integrals; Multiplication by t_n; Division by t; unit step function; Unit Impulse function; Laplace transforms of Periodic functions.

III (18.1 to 18.4, 18.5(a), 18.5(b), 18.7 to 18.10, 18.13(1), 18.13(2), 18.13(3))

UNIT VIII

INVERSE LAPLACE TRANSFORMS   **08 hrs**

Definition; Standard results; Theorems on Inverse Laplace transforms; Problems; Convolution Theorem (only statements and problems); Application of Laplace transform to solve Linear differential problems.

III (18.6, 18.11, 18.12)

Text Books:
 I. Engineering mathematics –Dr. B.S.Grewal, 12th edition 2007, Khanna publishers, Delhi.
 II. Engineering Mathematics – H.K.Dass, S. Chand and Company Ltd, 13th Revised Edition 2007, New Delhi.
 III. A Text book of engineering Mathematics – N.P. Bali and Manish Goyal , 7th Edition 2007, Laxmi Publication(P) Ltd.

Reference Book:
 1. Applied Mathematics for Polytechnic, H.K.Dass, 8th Edition, CBS Publishers
    & Distributors, New Delhi

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE56   **ANALOG ELECTRONICS**

UNIT I
INTEGRATED CIRCUIT FABRICATION   **07 hrs**
Introduction; Classification; IC Chip Size and Circuit Complexity; Fundamentals of Monolithic IC Technology; Basic Planar Processes; Fabrication of a Typical Circuit; Active and Passive Components of IC's; Fabrication of FET; Thin and Thick Film Technology; Technology Trends.
II (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 1.10)

UNIT II
AC ANALYSIS OF BJT CIRCUITS   **07 hrs**
Coupling and Bypassing Capacitors; AC Load Lines; Transistor Models and Parameters; Common Emitter Circuit Analysis; CE Circuit with un-bypassed Emitter Resistor; Common Collector Circuit Analysis; Common Base Circuit Analysis; Comparison of CE; CC and CB Circuits.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8)

UNIT III
FIELD EFFECT TRANSISTORS   **07 hrs**
Junction Field Effect Transistor; JFET Characteristics; JFET Data Sheet and Parameters; FET Amplification; MOSFETS.
I (9.1, 9.2, 9.3, 9.4, 9.5)

UNIT IV
AUDIO POWER AMPLIFIERS   **04 hrs**
Transformer Coupled Class-A Amplifier; Transformer Coupled Class-B Amplifier; and Class AB Amplifiers; Transformer Coupled Amplifier Design; Complementary Emitter Follower.
I (18.1, 18.2, 18.3, 18.4)

OPTOELECTRONIC DEVICES   **03 hrs**
Light Units; Light Emitting Diodes; Seven Segment Displays; Photo Transistors; Opto-couplers.
I (20.1, 20.2, 20.3, 20.6, 20.7)

UNIT V
OPERATIONAL AMPLIFIER   **04 hrs**
Basic Information of Operational Amplifier; The Ideal Operational Amplifier; Operational Amplifier Internal Circuit.
II (2.1, 2.2, 2.3, 2.4, 2.4.1, 2.4.2)

OPERATIONAL AMPLIFIER CHARACTERISTICS   **04 hrs**
Introduction; DC Characteristics; AC Characteristics; Frequency Response; Stability of Op-Amp (Qualitative Analysis); Slew Rate; Analysis of Data Sheet of an Op-Amp.
II (3.1, 3.2, 3.3, 3.3.1, 3.3.2, 3.3.4, 3.4)

UNIT VI
OPERATIONAL AMPLIFIER APPLICATIONS   **08 hrs**
Introduction; Basic Op-Amp Applications; Instrumentation Amplifier; AC Amplifier; V to I and I to V Converters; Op-Amp Circuits using Diodes; Sample and Hold Circuits; Differentiator; Integrator; Monolithic Power Amplifiers.
II (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.10, 4.11, 4.13)

UNIT VII
COMPARATORS AND WAVEFORM GENERATORS   **04 hrs**
Introduction; Comparator; Regenerative Comparator (Schmitt Trigger); Square Wave Generator (Astable Multivibrator); Monostable Multivibrator; Triangular Wave Generator; Sine Wave Generators.
 II (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7)

555 TIMER   **04 hrs**
Introduction; Description of Functional Diagram; Monostable Operation; Astable Operation.
II (8.1, 8.2, 8.3, 8.4)

UNIT VIII
VOLTAGE REGULATORS; DAC AND ADC   **08 hrs**
Introduction; Series Op-Amp regulator; IC Voltage Regulator; 723 General Purpose Regulator; Basic DAC Techniques; A-D Converters.
II   (6.1, 6.2, 6.3, 6.4, 10.1, 10.2, 10.2.1, 10.2.2, 10.3, 10.3.1, 10.3.2, 10.3.4, 10.3.6)

Text Books:

 I. Electronic Devices and Circuits, Fourth Edition, David A Bell, PHI (2006).
 II. Linear Integrated Circuits, Revised Second Edition, D. Roy Choudhury, Shail B. Jain, New Age International Publishers.

Reference Books:

1. Electronic Devices and Circuits, I.J. Nagrath, PHI, 2007.
2. Operational Amplifiers and Linear IC's, Second Edition, David A Bell, PHI.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE57   **NETWORKS AND TRANSMISSION LINES**

UNIT I
BASIC CONCEPTS   **07 hrs**
Introduction; Network Elements; R, L, C Parameters; The Resistance Parameter; The Inductance Parameter; The Capacitance Parameter; Energy Sources; Transformation of Energy Sources; Two Mutually Coupled Inductors and Dot Convention.
I (1.1, 1.2, 1.6 to 1.11, 1.13.1)

UNIT II
LAPLACE TRANSFORMS AND SIGNAL FUNCTIONS   **08 hrs**
Introduction; Laplace Transformation and Inverse Laplace Transformation; Advantages of Laplace Transforms in Solving Integro-Differential Equations; Important Theorems; Transforms of Standard Functions Namely a Constant (A) t, t^2 and t^n; e^{at} and e^{-at}, sin ωt, cos ωt, sin(ωt+α), cos (ωt+α), e^{-at} sin(ωt+α), e^{-at} cost (ωt+α), sinh ωt and cosh ωt (without proofs); Transforms of Derivatives and Integrals (Without proofs); Response to Shifted Unit Step Functions; Shifting Theorem; Ramp and Impulse Functions; Unit Ramp and Impulse Functions; Laplace Transformation of Impulse; Synthesis of a Few Typical Waveforms and their Laplace Transforms; Transform of any Function That Repeats Itself; Initial and Final Values Theorem; The Convolution Integral.
I (6.1 to 6.5; 7.1 to 7.3; 7.8 to 7.10, 7.14, 7.18, 7.19, 7.22, 7.23)

UNIT III
NETWORK THEOREMS   **07 hrs**
Superposition Theorem; Thevenin's and Norton's Theorem; Millman Theorem and its dual (All theorems without proofs); Thevenin's and Norton's Theorem in Frequency Domain; Reciprocity Theorem; Substitution theorem; Compensation Theorem; Maximum Power Transfer Theorem; Bisection Theorem; π-T Equivalent Theorem; Foster's Reactance Theorem; Principle of Duality.
I (9.1 to 9.8); II (13.7, 13.8, 13.9, 13.10, 13.11, 13.12, 13.14)

UNIT IV
NETWORK FUNCTIONS AND PARAMETERS   **08 hrs**
Introduction; Network Functions for One Port Network; Network Functions for a Two Port Network; Network Functions as a Quotient of Polynomials in s; Poles and Zeros of Network Functions; Significance of Poles and Zeros in Network Functions; Criterion for Stability in Terms of Denominator Polynomial of Transfer Function: Routh Criterion; Short Circuit Admittance Parameters; Open Circuit Impedance Parameters; Expressions for z-parameters in Terms of y-parameters and vice-versa; Transmission Parameters (A, B, C, D Parameters); Expressions for A B C D Parameters in Terms of z-parameters and y-parameters; Hybrid Parameters; Conversion of Parameter Sets; Conditions for Reciprocity of a Two-port Network; T-section and π-section Representation of a Two-port Network; Image Impedances; Image parameters in Terms of Short Circuit and Open Circuit Impedances; Symmetrical Networks; Ladder Network; Bridged-T, Parallel-T and Lattice Networks.
I (10.1 to 10.6, 10.11, 11.1 to 11.6; 11.8; 11.10; 11.11; 11.19; 11.20; 11.22 to 11.26)

UNIT V
RESONANCE CIRCUITS AND SELECTIVITY   **08 hrs**
Series Resonance; Phasor Diagram of Series R-L-C Circuit; Reactance and Impedance Curves of a Series R-L-C Circuit; Variation of Current and Voltages with Frequency in a series R-L-C Circuit; Selectivity and Bandwidth; Quality Factor; Parallel Resonance; Impedance, Selectivity and Bandwidth of Parallel Tuned Circuit; Use of Double Tuned Circuits in Radio Receivers.
I (22.1 to 22.7; 22.11 to 22.13; 22.20)

UNIT VI
TRANSMISSION LINES   **07 hrs**
Introduction; Distributed Parameters and Primary Constants; Loop Inductance; Shunt Capacitance; Loop Resistance; Equivalent Circuit; Secondary constants of a line; General Equation of a Transmission Line; Line Terminated in an Impedance other than Z_0; Distortions in Transmission Lines; Distortionless Line and Loading of Lines (Qualitative study only); Wave Propagation in Transmission Lines; Propagation of a link terminated in Z_R; Reflection in open circuited and short circuited lines; Reflection of a line terminated in Impedance other than Z_0; Reflection Coefficient; Reflection factor and Reflection loss; Insertion Loss;
I (17.1, 17.2, 17.3, 17.4, 17.5, 17.6, 17.7, 18.1 to 18.4; 18.7, 19.1 to 19.8)

UNIT VII
TRANSMISSION LINE AT RADIO FREQUENCIES   **08 hrs**
Parameters of Open wire and Coaxial Lines at Radio Frequencies; Secondary Constants of a Dissipationless Line; Voltages and Currents for a Lossless Line; Standing Wave Ratio (Without proofs); Input Impedance of the Lossless Line; Input Impedance of Open and Short Circuited Lossless Line; Impedance Matching Lines - ¼, ½ and $^1/_8$ Wavelength; Single and Double Stub Impedance Matching on Lines; Equations for Design of Single and Double Stubs (Without proofs); The Smith Chart and its Applications to Determine the Impedance; Admittance; VSWR, K and Design of Stubs.
I (20.1 to 20.11; 20.13; 20.15 to 20.17); II (6.13, 6.16)

UNIT VIII
FILTERS AND ATTENUATORS   **07 hrs**
Decibel and Neper; Classification of Filters; Constant k Low Pass and High Pass Filters; Design of Constant k Low Pass and High Pass Filters; Band Pass Filters; m-derived Filters; Symmetrical Attenuators – T, π, Bridged T and lattice Attenuators; Asymmetric Attenuators – T, L, π and L Attenuators Asymmetric L Attenuator Working Between Two Equal Impedances with a Given Loss.
I (23.1, 23.2, 23.5 to 23.9, 23.13, 24.1 to 24.11)

Text Books:
I.   Network Analysis; G. K. Mittal; 14th Edition (2007) Khanna Publications; New Delhi
II.   Transmission Lines and Networks; Umesh Sinha, 8th Edition (2003); Satya Prakashan, Incorporating Tech India Publications, New Delhi

Reference Book:
1.   Networks, Lines and Fields; John D Ryder; Prentice Hall of India.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE58   **LOGIC DESIGN**

UNIT I
INTRODUCTORY CONCEPTS   03 hrs
Numerical Representations; Digital and Analog Systems; Digital Number Systems; Representing Binary Quantities; Digital Circuits / Logic Circuits; Parallel and Serial Transmission; Memory, Digital Computers.
I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8)

NUMBER SYSTEMS AND CODES   04 hrs
Introduction; Binary to Decimal Conversions; Decimal to Binary Conversions; Octal Number System; Hexadecimal Number System; BCD Code; Putting it all together; The Byte; Nibble and Word; Alphanumeric Codes; Parity Method for Error Detection.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9)

UNIT II
DESCRIBING LOGIC CIRCUITS   04 hrs
Introduction; Boolean Constants and Variables; Truth Tables: OR, AND, NOT Operations; Describing Logic Circuits Algebraically; Evaluating Logic Circuit Outputs; Implementing Circuits from Boolean Expressions; NOR and NAND Gates; Boolean Theorems; De-Morgan's Theorems; Universality of NAND and NOR Gates.
I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, 3.12)

COMBINATIONAL LOGIC CIRCUITS   04 hrs
Sum of Product Form; Simplifying Logic Circuits; Algebraic Simplification; Designing Combinational Logic Circuits; Karnaugh Map Method (3 and 4 Variables); Exclusive OR and Exclusive NOR Circuits; Parity Generator and Checker; Enable and Disable Circuits.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8)

UNIT III
FLIP-FLOPS AND APPLICATIONS   08 hrs
Introduction; NAND Gate Latch; NOR Gate Latch; Clocked Signals and Clocked Flip-Flops; Clocked SR Flip-Flop; Clocked JK Flip-Flop; Clocked D Flip-Flop; D Latch; Asynchronous Inputs; IEEE / ANSI Symbols; Flip-Flop Timing Considerations; Potential Timing Problem in Flip-Flop Circuits; Master Slave Flip-Flops; Flip-Flop Applications; Flip-Flop Synchronization; Data Storage and Transfer; Serial Data Transfer: Shift Registers; Frequency Division and Counting; Schmitt Trigger Devices; Analyzing Sequential Circuits.
I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11, 5.12, 5.13, 5.14, 5.16, 5.17, 5.18, 5.19, 5.20)

UNIT IV
DIGITAL ARITHMETIC: OPERATIONS AND CIRCUITS   08 hrs
Introduction; Binary Addition; Representing Signed Numbers; Addition in 2's Complement System; Subtraction in 2's Complement System; Multiplication and Division of Binary Numbers; BCD Addition; Hexadecimal Arithmetic; Arithmetic Circuits; Parallel Binary Adder; Design of a Full Adder; Complete Parallel Adder with Registers; Carry Propagation; Integrated Circuit Parallel Adder; 2's Complement System; BCD Adder; ALU Integrated Circuits.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11, 6.12, 6.13, 6.14, 6.15, 6.16, 6.17)

UNIT V
COUNTERS AND REGISTERS   08 hrs
Introduction; Asynchronous (Ripple) Counters; Counters with Mod Numbers $< 2^N$; IC Asynchronous Counters; Asynchronous Down Counters; Propagation Delay in Ripple Counters; Synchronous (Parallel) Counters; Synchronous Down and Up / Down Counters; Presettable Counter; Decoding a Counter; Decoding Glitches; Cascading BCD Counters.
I (7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.7, 7.8, 7.11, 7.12, 7.13)

UNIT VI

MSI LOGIC CIRCUITS   **07 hrs**

Introduction; Decoders; BCD to 7-Segment Decoder / Drivers; Liquid Crystal Displays; Encoders; Multiplexers; Multiplexer Applications; De-Multiplexers; Magnitude Comparator; Code Converters.
I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7, 9.8, 9.9)

UNIT VII

SYNCHRONOUS COUNTER DESIGN   **07 hrs**

Synchronous Counter Design; Integrated Circuit Registers; Parallel In / Parallel Out Register; Serial In / Serial Out Register; Parallel In / Serial Out Register; Serial In / Parallel Out Register; Shift Register Counters.
I (7.14, 7.15, 7.16, 7.17, 7.18, 7.19, 7.21)

UNIT VIII

MEMORY DEVICES   **07 hrs**

Memory Terminology; General Memory Operation; CPU Memory Connections; Read Only Memories; ROM Architecture; ROM Timing; Types of ROM's; Flash Memory; ROM Applications; Semiconductor RAM; RAM Architecture; SRAM; DRAM; DRAM Structure and Operation.
I (11.1, 11.2, 11.3, 11.4, 11.5, 11.6, 11.7, 11.8, 11.9, 11.10, 11.11, 11.12, 11.13, 11.14)

Text Book:

I. Digital Systems – Principles and Applications, Ronald J Tocci, Neal S. Wildmer, Gregory L. Moss, Ninth Edition, Pearson Education, 2008.

Reference Books:

1. Digital Fundamentals, Thomas L. Floyd and R. P. Jain, Eighth Edition, Pearson Education Publisher, 2005
2. Digital Electronics and Microprocessors – Problems and Solutions, R. P. Jain, 2007, Tata-McGraw Hill

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE92   **ANALOG ELECTRONICS LAB**

List of Experiments

1. **Characteristics of Semiconductor Diode and Zener Diode:** Determination of forward and reverse resistance from VI characteristics.
2. **Static Characteristics of BJT under CE Mode:** Determination of h-parameters h_{ie} from input characteristics and h_{fe} and h_{oe} from output characteristics.
3. **Static Characteristics of JFET:** Determination of r_d from drain characteristics and g_m from mutual characteristics and hence obtain amplification factor.
4. **Characteristics of UJT:** Determination of intrinsic standoff ratio η from emitter characteristics.
5. **Resonant Circuits:** Characteristics of Series and Parallel Circuits, Determination of quality factor and bandwidth.
6. **Bridge Rectifier with and without C-Filter:** Display of output waveforms and Determination of ripple factor, efficiency and regulation for different values of load current.
7. **Diode Clipping Circuits:** Design and display the transfer characteristics of single ended and double ended shunt type clipping circuits.
8. **RC Coupled Single-stage BJT Amplifier:** Determination of lower and upper cutoff frequencies, mid band voltage gain, gain bandwidth product from the frequency response.
9. **Emitter Follower:** Determination of mid band voltage gain, input and output impedances at mid frequency range.
10. **Class-B Complementary Symmetry Power Amplifier:** Display of input and output waveforms and Determination of the conversion efficiency and optimum load.
11. **BJT Colpitt's Oscillator:** Design and test the performance for a given frequency.
12. **Study of Basic Op-Amp Circuits:** Design and verification of inverting amplifier, non-inverting amplifier, voltage follower, integrator, differentiator and inverting adder circuits.
13. **Schmitt Trigger:** Design, testing, and display of waveforms.
14. **Op-Amp Wein Bridge Oscillator:** Design and test the performance for the given frequency.
15. **Study of 555 Timer:** Design and test the performance of Astable multivibrator circuit for the given frequency.
16. **Study of Voltage Regulator:** Design and study of IC7805 voltage regulator, calculation of line and load regulation.

Note: Minimum of 14 experiments to be conducted.

DE59 **ELECTRONIC INSTRUMENTATION AND MEASUREMENTS**
UNIT I
MEASUREMENT FUNDAMENTALS **08 hrs**

Significance of Measurements; Methods of Measurements; Instruments and Measurement Systems; Mechanical, Electrical and Electronic Instruments; Classification of Instruments. Characteristics of Instruments; Static Calibration; Static Characteristics; Errors in Measurement; True value; Static Error; Static Correction; Scale Range and Scale Span; Error Calibration; Accuracy and Precision; Indication of Precision; Linearity; Hysteresis; Threshold; Dead Time and Dead Zone; Resolution.

Limiting Errors; Relative Limiting Error; Combination of Quantity with Limiting Errors; Known and Types of Errors; Gross Errors; Systematic Errors; Random Errors.

Units, Systems, Dimensions and Standards – Units; Absolute Units; Fundamental and Derived Units; Dimensions; Dimensions of Mechanical Quantities; Dimensional Equations; Relationship between Electrostatic and Electromagnetic System of Units; SI Units; Base Units of SI; Standards and their Classification.

I (1.1 to 1.6, 2.1 to 2.9, 2.13,2.14, 2.18 to 2.23, 3.1 to 3.8, 5.1 to 5.6, 5.9, 5.10, 5.13, 5.14, 5.20)

UNIT II
MEASUREMENT OF RESISTANCE, INDUCTANCE AND CAPACITANCE **08 hrs**

Measurement Resistance-Classification of resistances; Measurement of Medium Resistances-Wheatstone Bridge; Sensitivity of Wheatstone Bridge; Measurement of Low Resistance-Kelvin Double Bridge; Measurement of High resistance-Difficulties; Earth Resistance Measurement using Megger. Measurement of Inductance-General Form of an AC Bridge; Measurement of Self Inductance Using Anderson Bridge; Measurement of Capacitance Using Schering Bridge; High Voltage Schering Bridge.

I (14.1, 14.2, 14.2.3, 14.2.4, 14.3.2, 14.4, 14.4.1, 14.5, 16.4, 16.5.4, 16.6.2, 16.6.3)

UNIT III
INSTRUMENTS TO MEASURE CURRENT AND VOLTAGES **07 hrs**

Measurement of current by DC Ammeter; Multi range Ammeters; RF Ammeters; Limitations of Thermocouple; Effect of Frequency on Calibration; Measurement of Very Large Currents by Thermocouple.

Measurement of voltage by DC Voltmeter; DC Voltmeter; Multi range AC voltmeter; Solid State Voltmeter; AC Voltmeter using Rectifier, Half-Wave and Full Wave Rectifiers; Average and Peak Responding Voltmeter; True RMS Voltmeter; Multimeter; Digital Multimeters.

II (3.1, 3.2, 3.6, 3.7, 3.8, 3.9, 4.2, 4.3, 4.4, 4.9, 4.12 to 4.14, 4.16 to 4.18, 4.25, 6.2)

UNIT IV
DIGITAL MEASURING INSTRUMENTS **07 hrs**

Digital Voltmeter-Dual Slope Integrating Type DVM; Integrated Type DVM; Continuous Balanced DVM; 3½ Digit; Digital Meter for Measuring Frequency and Time; Counter-Universal, Decade, Electronic; Digital Tachometer; Digital pH Meter; Digital Phase Meter; Digital Capacitance Meter. Other Measuring Instruments-Output Power Meter; Field Strength Meter; Phase Meter; Q-Meter

II (5.3, 5.4, 5.7, 5.8, 6.3 to 6.10, 6.12, 6.13, 10.2, 10.3, 10.5, 10.7)

UNIT V
SIGNAL GENERATORS AND OSCILLOSCOPE **08 hrs**

Introduction; Basic Standard Signal Generator; Standard Signal Generator; Modern Laboratory Signal Generator; AF Sine and Square Wave Generator; Function Generator; Square and Pulse Generator; Standard Specifications of a Signal Generator. Oscilloscope-Basic Principle; CRT Features; Block diagram; Simple CRO; Vertical Amplifier; Deflecting system; Triggered CRO; Trigger Pulse Circuits; Storage and Sampling Oscilloscope.

II (8.1, 8.4 to 8.9, 8.20, 7.1 to 7.9, 7.17, 7.18)

UNIT VI
SIGNAL ANALYSIS INSTRUMENTS AND R.F POWER MEASUREMENT TECHNIQUES

08 hrs

Wave Analyzers-Basic; Frequency Selective; Heterodyne Wave Analyzers; Harmonic Distortion and Spectrum Analyzer.
Bolometer Method of Power Measurement; Bolometer Element and Mount; Measurement of Power by Means of Bolometer Bridge; Unbalanced and Self Balancing Bolometer Bridge; Measurement of Large Amount of RF Power.
II (9.2, 9.4, 9.5, 9.6, 20.3 to 20.10)

UNIT VII

RECORDERS **07 hrs**

Objective and Requirement of Recording Data; Recorder Selection for Particular Applications; Recorders-Strip Chart; Galvanometer Type; Null Type; Circular Chart Type; X-Y; Magnetic; Potentiometric Recorders; Recorder Specifications.
II (12.2 to 12.7, 12.10 to 12.13)

UNIT VIII

TRANSDUCERS AND DATA ACQUISITION SYSTEM **07 hrs**

Electrical transducer; Selecting a Transducer; Resistive transducer; Resistive Position Transducer; Strain Gauges; Resistance Thermometer; Thermistor; Inductive Transducer, Differential Output Transducers; LVDT; Pressure Inductive; Capacitive Transducers; Load Cell; Temperature Transducers, Flow Measurement Transducer. Data Acquisition System-Objective of Data Acquisition System; Signal Conditioning of the Inputs; Single and Multi Channel Data Acquisition System.
II (13.2 to 13.14, 13.20, 13.23, 17.1 to 17.5)

Text Books:
 I. A Course in Electrical and Electronic Measurements and Instrumentation, A.K Sawhney, Dhanpat Rai & Co., New Delhi, 18th Edition 2007.
II. Electronic Instrumentation, H.S Kalsi, Tata McGraw Hill, Second Edition 2004.

Reference Books:
1. Electronic Instrumentation and Measurement Techniques, W.D. Cooper and A. D. Helfrick, Prentice Hall of India Pvt. Ltd., New Delhi
2. Electronic Instrumentation and Measurements, David A. Bell, Second Edition, PHI, 2007.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE60   **MICROPROCESSORS & MICROCONTROLLERS**

UNIT I
INTRODUCTION TO MICROPROCESSORS   **08 hrs**

Evolution of Microprocessors, Fundamentals of a Computer, Number Representation – Unsigned binary integers, Signed binary integers; Fundamentals of Microprocessor – description of 8085 pins, Programmer's view of 8085, Registers A, B, C, D, E, H and L First Assembly Language Program; Instruction set of 8085 – Data transfer group, Arithmetic group, Logical group, NOP and Stack group of instructions .
I (1, 2, 3.1, 3.2, 4.2, 4.3, 4.4, 4.5, 5, 6, 7, 8, 9)

UNIT - II
INTRODUCTION TO MICROPROCESSORS (CONTD)   **08 hrs**

Instruction set of 8085 continued – Branch group, Chip select logic, Addressing of I/O ports, Architecture of 8085 – Details of 8085 architecture
I (10, 11, 12, 13.1)

UNIT III
ASSEMBLY LANGUAGE PROGRAMS   **07 hrs**

Exchange 10 bytes, Add 2 multibyte numbers, Add 2 multibyte BCD numbers, Block movement without overlap, Monitor routines, Multiply two numbers
Linear search, Find the smallest number
I (14.1 to 14.4, 14.6.1, 16.1, 16.2)

UNIT IV
INTERRUPTS IN 8085

                                                                      07 hrs

Data transfer schemes, 8085 interrupts, EI and DI instructions, INTR and INTA* pins, RST 5.5, RST 6.5, RST 7.5, and TRAP pins, SIM and RIM instructions
I (18.1 to 18.7, 18.9)

UNIT V
PROGRAMS USING INTERFACE MODULES
         07 hrs

8255 Programmable peripheral interface chip, Description of 8255, Operational modes, Control port of 8255, Logic controller interface, Evaluation of Boolean expression, Decimal counter, Intel 8279 Keyboard and display controller.
I (20.1, 20.2, 20.3, 21.1 – 21.1.1, 21.1.3, 22.6.1)

UNIT VI
INTEL 8259A- PROGRAMMABLE INTERRUPT CONTROLLER   **08 hrs**

Need for interrupt controller, Overview of 8259, Pins of 8259, Registers of 8259, Intel 8257 – Programmable DMA controller, Concept of DMA, Need for DMA, Description of 8257, Pins of 8257.
I (23.1 to 23.4, 24.1, 24.2, 24.3, 24.5)

UNIT VII
INTEL 8253 – PROGRAMMABLE INTERVAL TIMER

                                                                      08 hrs

Need for programmable interval timer, Description of 8253, Programming the 8253, Mode 0 operation, Intel 8251A – Universal synchronous asynchronous receiver transmitter, Need for USART, Asynchronous transmission, Asynchronous reception, Synchronous transmission, Synchronous reception, Pin description of 8251.
I (25.1 to 25.4, 26.1 to 26.6)

UNIT VIII
8051 MICROCONTROLLER

                                                                      07 hrs

Main features, Functional blocks, Program memory structure, Data memory structure, Programmer's view, Addressing modes, Instruction set, Programming examples.
I (29)

Text Book:
I. The 8085 Microprocessor; Architecture, Programming and Interfacing, K. Udaya Kumar and B. S. Umashankar, Pearson Education, 2008

Reference Books:
1. Microprocessor Architecture, Programming and Applications with the 8085, Fourth Edition, R. S. Gaonkar, Penram International Publishing (India), 2000
2. The 8051 Microcontroller and Embedded Systems, Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay, Second Edition, Pearson Education, 2008

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE61   **ANALOG COMMUNICATIONS**

UNIT I

INTRODUCTION TO COMMUNICATION SYSTEMS   **03 hrs**
Communications; Communication Systems; Modulation; Bandwidth Requirements.
I (1.1, 1.2, 1.3, 1.4)

NOISE   **04 hrs**
External Noise; Internal Noise; Noise Calculations; Noise Figure; Noise Temperature.
I (2.1, 2.2, 2.3, 2.4, 2.5)

UNIT II

AMPLITUDE MODULATION   **04 hrs**
Amplitude Modulation Theory; Generation of AM.
I (3.1, 3.2)

SINGLE-SIDEBAND TECHNIQUES   **04 hrs**
Evolution and Description of SSB; Suppression of Carrier; Suppression of Unwanted Sideband; Extensions of SSB.
I (4.1, 4.2, 4.3, 4.4)

UNIT III

FREQUENCY MODULATION   **07 hrs**
Theory of Frequency and Phase Modulation; Noise and Frequency Modulation; Generation of Frequency Modulation.
I (5.1, 5.2, 5.3)

UNIT IV

RADIO RECEIVERS   **08 hrs**
Receiver Types; AM Receivers; FM Receivers; Single and Independent Sideband Receivers.
I (6.1, 6.2, 6.4, 6.5)

UNIT V

ANTENNAS   **08 hrs**
Basic Considerations; Wire Radiators in Space; Terms and Definitions; Effects of Ground on Antennas; Antenna Coupling at Medium Frequencies; Directional High-Frequency Antennas; UHF and Microwave Antennas.
I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7)

UNIT VI

RADIATION AND PROPAGATION OF WAVES   **03 hrs**

Electromagnetic Radiation; Propagation of Waves.
I (8.1, 8.2)

WAVEGUIDES, RESONATORS AND COMPONENTS   **05hrs**
Rectangular Waveguides; Circular and Other Waveguides; Waveguide Coupling, Matching and Attenuation; Cavity resonators.
I (10.1, 10.2, 10.3, 10.4)

UNIT VII

PULSE COMMUNICATIONS   **07 hrs**
Information Theory; Pulse Modulation; Pulse Systems.
I (13.1, 13.2, 13.3)

UNIT VIII

BROADBAND AND COMMUNICATIONS SYSTEMS   **07hrs**
Multiplexing; Short and Medium-Haul Systems; Long-Haul Systems; Elements of Long-Distance Telephony.

I (15.1, 15.2, 15.3, 15.4)

Text Book
I. Electronic Communication Systems, George Kennedy and Bernard Davis, Fourth Edition (1999), Tata McGraw Hill Publishing Company Ltd.

Reference Books
1. Communication Systems, 3rd Edition, Simon Haykin, John Wiley & Sons.
2. Telecommunications Principles Circuits Systems and Experiments, S. Ramabhadran, Khanna Publishers, Sixth Edition, 1997.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE62   **TELECOMMUNICATION SWITCHING SYSTEMS**

UNIT I
SWITCHING SYSTEMS   **08 hrs**
Evolution of Telecommunications; Basics of a Switching System; Functions of a Switching System; Strowger Switching Components; Step by Step Switching; Design Parameters; 100 Line Switching System; 1000 Line Blocking Exchange; 10,000 Line Exchange; Crossbar Switching-Principle of Crossbar Switching; Crossbar Switch Configurations; Crosspoint Technology; Crossbar Exchange Organization; A General Trunking; Electronic Switching; Reed Electronic Systems; Digital Switching Systems.
I (3.5, 3.10, 3.11, 3.12, 3.13); II (1.1, 1.3, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 3.3, 3.4, 3.5, 3.6)

UNIT II
TELECOMMUNICATIONS TRAFFIC   **08 hrs**
Introduction; The Unit of Traffic; Congestion; Traffic Measurement; A Mathematical Model; Lost-Call Systems-Theory; Traffic Performance; Loss Systems in Tandem; Use of Traffic Tables; Queuing Systems-The Second Erlang Distribution; Probability of Delay; Finite Queue Capacity; Some Other Useful Results; Systems with a Single Server; Queues in Tandem; Delay Tables; Applications of Delay Formulae.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III
SWITCHING NETWORKS   **08 hrs**
Introduction; Single Stage Networks; Gradings-Principle; Design of Progressive Gradings; Other Forms of Grading; Traffic Capacity of Gradings; Application of Gradings; Link Systems-General, Two Stage Networks; Three Stage Networks; Four Stage Networks; Discussion; Grades of Service of Link Systems.
I (5.1, 5.2, 5.3, 5.4, 5.5)

UNIT IV
TIME DIVISION SWITCHING   **07 hrs**
Basic Time Division Space Switching; Basic Time Division Time Switching; Time Multiplexed Space Switching; Time Multiplexed Time Switching; Combination Switching; Three Stage Combination Switching.
II (6.1, 6.2, 6.3, 6.4, 6.5, 6.6)

UNIT V
CONTROL OF SWITCHING SYSTEMS   **07 hrs**
Introduction; Call Processing Functions-Sequence of Operations; Signal Exchanges; State Transition Diagrams; Common Control; Reliability; Availability and Security; Stored Program Control.
I (7.1, 7.2, 7.3, 7.4, 7.5)

UNIT VI
SIGNALLING   **08 hrs**
Introduction; Customer Line Signaling; Audio Frequency Junctions and Trunk Circuits; FDM Carrier Systems-Outband Signaling; Inband (VF) Signaling; PCM Signaling; Inter Register Signaling; Common Channel Signaling Principles-General Signaling Networks; CCITT Signaling System Number 6; CCITT Signaling System Number 7; The High Level Data Link Control Protocol; Signal Units; The Signaling Information Field.
I (8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8, 8.9)

UNIT VII

PACKET SWITCHING **07 hrs**

Introduction; Statistical Multiplexing; Local Area and Wide Area Networks-Bus Networks; Ring Networks; Comparison of Bus and Ring Networks; Optical Fiber Networks; Large Scale Networks-General; Datagrams and Virtual Circuits; Routing; Flow Control; Standards; Frame Relay; Broadband Networks-General; The Asynchronous Transfer Mode; ATM Switches.

I (9.1, 9.2, 9.3, 9.4, 9.5)

UNIT VIII

NETWORKS **07 hrs**

Introduction; Analog Networks; Integrated Digital Networks; Integrated Services Digital Networks; Cellular Radio Networks; Intelligent Networks; Private Networks; Charging; Routing-General, Automatic Alternative Routing.

I (10.1, 10.2, 10.3, 10.4, 10.5, 10.6, 10.7, 10.9, 10.10)

Text Books:

 I. Telecommunications Switching, Traffic and Networks, J.E.Flood, Pearson Education, 2006.
II. Telecommunication Switching Systems and Networks, Thiagarajan Viswanathan, Prentice Hall of India Pvt. Ltd, 2006.

Reference Book:
1. Digital Telephony, John C Bellamy, John Wiley International Student Edition.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE93   **LOGIC DESIGN LAB**

List of Experiments

1. **Study of Logic Gates:** Truth-table verification of OR, AND, NOT, XOR, NAND and NOR gates; Realization of OR, AND, NOT and XOR functions using universal gates.
2. **Half Adder / Full Adder:** Realization using basic and XOR gates.
3. **Half Subtractor / Full Subtractor:** Realization using NAND gates.
4. **Parallel Adder / Subtractor:** Perform adder and subtractor operation using IC7483 chip.
5. **4-Bit Binary-to-Gray & Gray-to-Binary Code Converter:** Realization using XOR gates.
6. **4-Bit and 8-Bit Comparator:** Implementation using IC7485 magnitude comparator chips.
7. **Multiplexer:** Truth-table verification and realization of Half adder and Full adder using IC74153 chip.
8. **Demultiplexer:** Truth-table verification and realization of Half subtractor and Full subtractor using IC74139 chip.
9. **LED Display:** Use of BCD to 7 segment decoder / driver chip to drive LED display.
10. **Flip Flops:** Truth-table verification of JK Master Slave FF, T-type and D-type FF using IC7476 chip.
11. **Asynchronous Counter:** Realization of 4-bit up counter and Mod-N counter using IC7493 chip.
12. **Synchronous Counter:** Realization of 4-bit up/down counter and Mod-N counter using IC74192 chip.
13. **Shift Register:** Study of shift right, SIPO, SISO, PIPO and PISO operations using IC7495 chip.
14. **Ring counter and Twisted Ring Counter**: Realization using IC7495 chip.
15. **RAM:** Study of RAM (2K x 8 RAM) operation.
16. **DAC Operation:** Study of 8-bit DAC (IC 08/0800 chip).

Note:
- Minimum of 14 experiments to be conducted.
- All the experiments can be performed using IC Trainer Kits.

DE63   **DIGITAL COMMUNICATIONS**

UNIT I
INTRODUCTION   **02 hrs**

Sources and Signals; Basic Signal Processing Operations in Digital Communication; Channels For Digital Communications.
I (1.1, 1.2, 1.3)

FUNDAMENTAL LIMITS ON PERFORMANCE   **05 hrs**

Uncertainty, Information and Entropy; Source Coding Theorem; Huffman Coding; Discrete Memoryless Channels; Mutual Information; Channel Capacity; Channel Coding theorem.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7)

UNIT II
SAMPLING PROCESS   **07 hrs**

Sampling Theorem; Quadrature Sampling of BP Signal; Reconstruction of a Message Process from its Samples; Signal Distortion in Sampling; Practical Aspects of Sampling and Signal Recovery; Pulse Amplitude Modulation; Time Division Multiplexing.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III
WAVEFORM CODING TECHNIQUES   **08 hrs**

Pulse Code Modulation; Channel Noise and Error Probability; Quantization Noise And Signal to Noise Ratio; Robust Quantization; Differential PCM; Delta Modulation.
I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6)

UNIT IV

BASE-BAND SHAPING FOR DATA TRANSMISSION   **08 hrs**

Discrete PAM Signals; Power Spectra of Discrete PAM Signals; Inter Symbol Interference; Nyquist's Criterion for Distortionless Base-Band Binary Transmission; Correlative Coding; Eye Pattern, Base-Band M-ary PAM Systems; Adaptive Equalization for Data Transmission.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8)

UNIT V

DIGITAL MODULATION TECHNIQUES   **08 hrs**

Digital Modulation Formats; Coherent Binary Modulation Techniques; Coherent Quadrature Modulation Techniques; Non-Coherent Binary Modulation Techniques; Comparison of Binary And Quaternary Modulation Techniques; M-ary Modulation Techniques; Effect of Inter Symbol Interference; Synchronization.
I (7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.10, 7.12)

UNIT VI
DETECTION AND ESTIMATION   **07 hrs**

Gram-Schmidt Orthogonalization Procedure; Geometric Interpretation of Signals; Response of Bank of Correlators to Noisy Input; Detection of Known Signals in Noise; Probability of Error; Correlation Receiver; Matched Filter Receiver; Detection of Signals with Unknown Phase in Noise.
I (3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9)

UNIT VII
SPREAD SPECTRUM MODULATION   **08 hrs**

Pseudo Noise Sequences; Notion of Spread Spectrum; Direct Sequence Spread Coherent Binary PSK; Signal Space Dimensionality and Processing Gain; Probability of Error; Frequency Hop Spread Spectrum.
I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6)

UNIT VIII

APPLICATIONS **07 hrs**

Applications of Waveform Coding Techniques; Applications of Digital Modulation Techniques; Applications of Spread Spectrum Modulation.
I (5.8, 7.13, 9.7)

Text book:

I. Digital Communications, Wiley Student Edition, Simon Haykin

Reference books:

1. Digital and Analog Communication Systems, K. Sam Shanmugham, John Wiley.
2. An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE65   **CONTROL ENGINEERING**

UNIT I
INTRODUCTION   **03 hrs**
Control Systems: Introduction, Examples of Control Systems; Open-loop and Closed-loop Control Systems; Feedback; Characteristics of Feedback; Analog and Digital Control Systems; Control System Models.
I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8)

CONTROL SYSTEMS TERMINOLOGY   **04 hrs**
Block Diagram: Fundamentals; Block Diagram: Feedback and Closed-loop Systems; Block Diagram of Discrete-time Systems; Supplementary Terminology; Servomechanisms; Regulators.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7)

UNIT II
DIFFERENTIAL EQUATIONS AND LINEAR SYSTEMS   **04 hrs**
System Equations; Partial and Ordinary Differential Equations; Time Variability and Time-Invariance; Linear and Non-linear Differential Equations; The Differential Operator D and the Characteristic Equation; Linear Independence and Fundamental Sets; Solution of Linear Constant-Coefficient Ordinary Differential Equations; Free, Forced and Total Responses; The Steady State and Transient Responses; Singularity Functions: Steps, Ramps, Impulses; Second-Order Systems; Linearity and Superposition; Causality and Physically Realizable Systems.
I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, 3.12, 3.13, 3.14, 3.18, 3.19)

LAPLACE TRANSFORM APPLICATIONS   **04 hrs**
Laplace Transform and its inverse; Properties of Laplace Transform; Application of Laplace Transform to The Solution of Linear Constant – Coefficient Differential Equations; Partial Fraction Expansions; Complex Plane: Pole-Zero Maps; Graphical Evaluation of Residues; Second-Order Systems.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.11, 4.12, 4.13: Example 4.20 excluded.)

UNIT III
STABILITY   **02 hrs**
Stability Definitions; Characteristic Root Locations; Routh-Hurwitz Stability Criterion; Continued Fraction Stability Criterion.
I (5.1, 5.2, 5.3, 5.4, 5.5)

TRANSFER FUNCTIONS   **02 hrs**
Definition and Properties of a Continuous System Transfer Function; Transfer functions: Compensators and Controllers; Continuous System Time and Frequency Responses; Transfer Functions of Analogous Systems.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.9)

BLOCK DIAGRAM ALGEBRA   **04 hrs**
Introduction; Blocks in Cascade; Canonical form of a Feedback Control System; Block Diagram Transformation Theorems; Unity Feedback Systems; Superposition of Multiple Inputs: Reduction of Block Diagrams.
I (7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.7, 7.8)

UNIT IV
SIGNAL FLOW GRAPHS   **07 hrs**
Fundamentals of Signal Flow Graphs; Signal Flow Graph Algebra and Definitions; Construction of Signal Flow Graphs; General Input-Output Gain Formula; Transfer Function Computation of Cascaded Components; Block Diagram Reduction using Signal Flow Graphs.
I (8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8)

UNIT V

SYSTEM SENSITIVITY & CLASSIFICATION   **05 hrs**

Introduction; Sensitivity of Transfer Functions (z-Transforms excluded); Output Sensitivity to Parameters; Classification of Continuous Feedback Systems by Type; Position, Velocity and acceleration Error Constants for Continuous Unity Feedback Systems; Error Constants for more General Systems.

I (9.1, 9.2, 9.3 (State Variables excluded), 9.4, 9.5, 9.6, 9.7, 9.9, 9.10)

ANALYSIS AND DESIGN: OBJECTIVES AND METHODS   **02 hrs**

Objectives and Methods of Analysis; Design Objectives; System Compensation; Design Methods.

I (10.1, 10.2, 10.3, 10.4, 10.5, 10.6)

UNIT VI

NYQUIST ANALYSIS   **07 hrs**

Plotting Complex Functions of a Complex Variable; Definitions; Properties of the Mapping P(s); Polar Plots and their Properties; Nyquist path, Nyquist Stability Plot; Nyquist Stability Plots of Practical Feedback Control Systems; Nyquist Stability Criterion; Relative Stability.

I (11.1, 11.2, 11.3, 11.4, 11.5, 11.6, 11.7, 11.8, 11.9, 11.10, 11.11; [P (z) and Discrete-Systems excluded])

UNIT VII

ROOT-LOCUS ANALYSIS   **08 hrs**

Variation of Closed-loop System Poles: The Root-Locus; Angle and Magnitude Criteria; Number of Loci; Real Axis Loci, Asymptotes; Breakaway Points, Departure & Arrival Angles; Construction of Root-Locus; Closed-loop Transfer Function and Time–Domain Response; Gain and Phase Margins from Root-Locus; Damping Ratio from the Root-Locus.

I (13.1, 13.2, 13.3, 13.4, 13.5, 13.6, 13.7, 13.8, 13.9, 13.10, 13.11, 13.12)

UNIT VIII

BODE ANALYSIS   **08 hrs**

Logarithmic Scales and Bode Plots; Bode Form, Gain and Plots of Continuous Time Functions; Construction of Bode Plots for Continuous–Time Systems; Relative Stability; Closed-loop Frequency Response; Determination of Transfer Function from Bode Plot.

I (15.1, 15.2, 15.3, 15.4, 15.5, 15.7, 15.8, 15.9)

Text Book:

I. Feedback and Control Systems (Schaum's Outlines), Joseph J DiStefano III, Allen R. Stubberud and Ivan J. Williams, 2nd Edition, 2007, Tata McGraw-Hill Publishing Company Ltd.

Reference Books:

1. Control Engineering Pocket Book, W. Bolton, Newnes Butterworth Indian Edition, Delhi.
2. Modern Control Systems, Richard C. Dorf & Robert H Bishop, 10th Edition 2007, Pearson Education, Prentice-Hall.
3. Modern Control Engineering, D. Roy Choudhury, Prentice Hall India Pvt Ltd (2006).

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE66   **WIRELESS & MOBILE COMMUNICATIONS**

UNIT I
INTRODUCTION   **07 hrs**
History of Cellular Systems; Characteristics of Cellular Systems; Fundamentals of Cellular Systems; Cellular System Infrastructure; Satellite Systems; Network Protocols; Ad Hoc and Sensor Networks; Wireless MANs, LANs and PANs.
I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8)

UNIT II
MOBILE RADIO PROPAGATION   **06 hrs**
Introduction; Types of Radio Waves; Propagation Mechanisms; Free-Space Propagation; Land Propagation; Path Loss; Slow Fading; Fast Fading; Doppler Effect; Delay Spread; Intersymbol Interference; Coherence Bandwidth; Cochannel Interference.
I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, 3.12, 3.13)

CHANNEL CODING AND ERROR CONTROL   **02 hrs**
Introduction; Linear Block Codes; Cyclic Codes; Cyclic Redundancy Check; Convolutional Codes; Interleaver; Turbo Codes.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III
CELLULAR CONCEPT   **04 hrs**
Introduction; Cell Area; Signal Strength and Cell Parameters; Capacity of a Cell; Frequency Reuse; How to form a Cluster?; Cochannel Interference; Cell Splitting; Cell Sectoring.
I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9)

MULTIPLE RADIO ACCESS   **03 hrs**
Introduction; Multiple Radio Access Protocols; Contention-Based Protocols.
I (6.1, 6.2, 6.3)

UNIT IV
MULTIPLE DIVISION TECHNIQUES   **04 hrs**
Introduction; Concepts and Models for Multiple Divisions; Modulation Techniques.
I (7.1, 7.2, 7.3)

CHANNEL ALLOCATION   **03 hrs**
Introduction; Static Allocation versus Dynamic Allocation; Fixed Channel Allocation (FCA); Dynamic Channel Allocation (DCA); Allocation in Specialized System Structure.
I (8.1, 8.2, 8.3, 8.4, 8.6)

UNIT V
SATELLITE SYSTEMS   **04 hrs**
Introduction; Types of Satellite Systems; Characteristics of Satellite Systems; Satellite System Infrastructure; Call Setup; Global Positioning System.
I (11.1, 11.2, 11.3, 11.4, 11.5, 11.6)

MOBILE COMMUNICATION SYSTEMS   **04 hrs**
Introduction; Cellular System Infrastructure; Registration; Handoff Parameters and Underlying Support; Roaming Support; Multicasting.
I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6)

UNIT VI
EXISTING WIRELESS SYSTEMS   **08 hrs**
Introduction; AMPS; IS-41; GSM; IS-95; IMT-2000.
I (10.1, 10.2, 10.3, 10.4, 10.6, 10.7)

UNIT VII

AD HOC AND SENSOR NETWORKS **07 hrs**

Introduction; Characteristics of MANETs; Applications; Routing; Table-Driven Routing Protocols; Source-Initiated On-Demand Routing; Wireless Sensor Networks; Fixed Wireless Sensor Networks.

I (13.1, 13.2, 13.3, 13.4, 13.5, 13.6, 13.8, 13.9)

UNIT VIII

WIRELESS MANs, LANs AND PANs **05 hrs**

Introduction; Wireless Metropolitan Area Networks (WMANs); Wireless Local Area Networks (WLANs).

I (14.1, 14.2, 14.3)

RECENT ADVANCES **03 hrs**

Introduction; Ultra-Wideband Technology; Directional and Smart Antennas.

I (15.1, 15.2, 15.8)

Text Book:

 I. Introduction to Wireless and Mobile Systems, Second Edition (2007), Dharma Prakash Agrawal and Qing-An Zeng, Thomson India Edition.

Reference Book:

1. Wireless Communications-Principles and Practice, Second Edition (2007), Theodore S. Rappaport, Prentice Hall of India Pvt Ltd.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE67   **EMBEDDED SYSTEMS**
UNIT I
INTRODUCTION TO EMBEDDED SYSTEMS   **07 hrs**
Embedded Systems Overview; Design Challenge; Processor Technology; IC Technology; Design Technology; Trade-Offs.
I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6)
UNIT II
CUSTOM SINGLE PURPOSE PROCESSORS: HARDWARE   **07 hrs**
Introduction; Combinational Logic; Sequential Logic; Custom Single Purpose Processor Design; RT-level Custom Single Purpose Processor Design; Optimizing Custom Single Purpose Processors.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6)
UNIT III
GENERAL PURPOSE PROCESSORS: SOFTWARE   **08 hrs**
Introduction; Basic Architecture; Operation; Programmer's View; Development Environment; ASIPs; Selecting a Microprocessor; General Purpose Processor Design.
I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8)
UNIT IV
STANDARD SINGLE-PURPOSE PROCESSORS: PERIPHERALS   **08 hrs**
Introduction; Timers, Counters and Watchdog Timer; UART; Pulse Width Modulators; LCD Controllers; Keypad Controllers; Stepper Motor Controllers; Analog to Digital Converters; Real Time Clock.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9)
UNIT V
MEMORY   **08hrs**
Introduction; Memory Write Ability and Storage Permanence; Common Memory Types; Composing Memory; Memory Hierarchy and Cache; Advanced RAM.
I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6)
UNIT VI
INTERFACING   **08 hrs**
Introduction; Communication Basics; Microprocessor Interfacing: I/O Addressing; Microprocessor Interfacing: Interrupts; Microprocessor Interfacing: Direct Memory Access; Arbitration; Multilevel Bus Architecture; Advance Communication Principles; Serial Protocols; Parallel Protocols; Wireless Protocols.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11)

UNIT VII
INTRODUCTION TO REAL TIME OPERATING SYSTEMS   **07hrs**
Tasks and Task States; Tasks and Data; Semaphores and Shared Data.
II (6.1, 6.2, 6.3)
UNIT VIII
CASE STUDIES OF PROGRAMMING WITH RTOS   **07hrs**
Case Study of Coding for An Automatic Chocolate Vending Machine; Case Study of Coding for Sending Application Layer Byte Streams on TCP/IP Network; Case Study of An Embedded System for An Adaptive Cruise Control System in a Car.
III (11.1, 11.2, 11.3)

Text Books:
 I. Embedded System Design, A Unified Hardware/Software Introduction, Frank Vahid / Tony Givargis, 2006 reprint, John Wiley Student Edition.
 II. An Embedded Software Primer, David .E. Simon, Fourth Impression 2007, Pearson Education.
III. Embedded Systems, Raj Kamal, 13th reprint 2007, Tata-McGrawHill Publications.

Reference Book:
1. Embedded Microcomputer Systems, Valvano, Thomson.
Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE68   **TELEVISION ENGINEERING**

UNIT I
APPLICATIONS OF TELEVISION   **02 hrs**
Video, Audio, Television & Radio Signals; Television Broadcasting; Television Studio Operations; Video Tape Recorders; Cable TV.
I (1.1, 1.2, 1.3, 1.4, 1.5)

TELEVISION PICTURE   **03 hrs**
Picture Elements; Horizontal and Vertical Scanning; Video Signal Information; Motion Pictures; Frame and Field Frequencies; Horizontal and Vertical Scanning Frequencies; Horizontal and Vertical Synchronization, Blanking; 3.58 MHz Color Signal; Picture Qualities; Television Broadcast Channels; Standards of Transmission.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11, 2.12)

VIDEO CAMERAS AND CAMCORDERS   **03 hrs**
How a Video Camera Operates; Evolution of Pickup Devices; Charge Coupled Pickup Devices; Optical Color Separation.
I (3.1, 3.2, 3.3, 3.4)

UNIT II
PICTURE TUBES   **07 hrs**
Picture Tube Construction; Anode High Voltage; Screen Phosphors; Electron Gun; Electrostatic Focus; Magnetic Deflection; Tricolor Picture Tubes; Projection TV Systems; Picture Tube Precautions; Problems with Picture Tubes.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.10, 4.11, 4.12)

UNIT III
SCANNING & SYNCHRONIZING   **07 hrs**
Saw Tooth Waveform for Linear Scanning; Interlaced Scanning Pattern; Sample Frame of Interlaced Scanning; Flicker; Raster Distortions; Synchronizing Pulses; Construction of the Composite Video Signal.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 7.1)

UNIT IV
COLOR TV CIRCUITS & SIGNALS   **08 hrs**
Red, Green & Blue Video Signals; Color Addition; Definition of Color TV Terms; Encoding the Picture Information; Decoding the Picture Information; Y-signal for Luminance.
I (8.1, 8.2, 8.3, 8.4, 8.6, 8.7)

UNIT V
COLOR TV CIRCUITS & SIGNALS (CONTD…)   **07 hrs**
Types of Color Video Signals; Color Synchronization Burst; Colorplexed Composite Video Signal; Desaturated Colors With White; Color Resolution and Bandwidth; Color Subcarrier Frequency; Color TV Systems.
I (8.8, 8.9, 8.11, 8.12, 8.13, 8.14, 8.15)

UNIT VI
VIDEO TEST SIGNALS   **08 hrs**
EIA Test Pattern; Resolution Wedges in the Test Pattern; Test for Streaking or Smear in the Picture; Test for Ringing in the Picture; Broadcast Test Pattern Signals; Ball Chart for Checking Camera Linearity; EIA Standard for Color-Bar Signal; Window Signal; Sine-Squared Test Signal; Stair-Step Test Signals.
I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7, 9.8, 9.9, 9.10)

UNIT VII

TV RECEIVER SIGNAL CIRCUITS **08 hrs**

Superheterodyne Receivers; Television Receiver Block Diagram; Functional Blocks for the RF Signals; Functional Blocks for the Luminance and Chrominance Signals; Functional Blocks for Synchronization and Deflection; DC Power Source Block; Automatic Control Circuits; Functional Blocks for the Sound System.

I (14.1, 14.2, 14.3, 14.4, 14.5, 14.6, 14.7, 14.8)

UNIT VIII

TELEVISION AND VIDEO SERVICING **07 hrs**

Safety; Performance testing; Service Literature; Three Steps to Effective Trouble Shooting; Observe and Pinpoint the likely Block; Test for Signal Tracing and Signal Injection; Find Bad Part by Component Tracing; Test Equipment; Replacement Parts; Removable and Replacement of Defective Components; Final Adjustments and Performance Tests; Interference Patterns in the Picture.

I (21.1, 21.2, 21.3, 21.4, 21.5, 21.6, 21.7, 21.8, 21.9, 21.10, 21.11, 21.12)

Text Book:
 I. Basic Television and Video Systems, Bernard Grob and Charles E. Herndon, Sixth Edition, 1999, McGraw Hill International Edition.

Reference Books:
1. Television Engineering, Aravind M. Dhake, TMH Publication.
2. Monochrome & Color T.V., R. R. Gulati, New Age International (P).

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE69   **DATA COMMUNICATION & NETWORKS**

UNIT I

DATA COMMUNICATIONS, DATA NETWORKING, AND THE INTERNET   **04 hrs**
Data Communications and Networking for Today's Enterprise; A Communications Model; Data Communications; Networks; The Internet.
I (1.1, 1.2, 1.3, 1.4, 1.5)

PROTOCOL ARCHITECTURE, TCP/IP, AND INTERNET-BASED APPLICATIONS   **03 hrs**
The Need for a Protocol Architecture; The TCP/IP Protocol Architecture; The OSI Model; Standardization within a Protocol Architecture.
I (2.1, 2.2, 2.3, 2.4)

UNIT II

DATA TRANSMISSION   **05 hrs**
Concepts and Terminology; Analog and Digital Data Transmission; Channel Capacity.
I (3.1, 3.2, 3.4)

TRANSMISSION MEDIA   **03 hrs**
Guided Transmission Media; Wireless Transmission.
I (4.1, 4.2)

UNIT III

SIGNAL ENCODING TECHNIQUES   **05 hrs**
Digital Data, Digital Signals; Digital Data, Analog Signals; Analog Data, Digital Signals; Analog Data, Analog Signals.
I (5.1, 5.2, 5.3, 5.4)

DIGITAL DATA COMMUNICATION TECHNIQUES   **03 hrs**
 Types of Errors; Error Detection; Line Configurations.
I (6.2, 6.3, 6.5)

UNIT IV

DATA LINK CONTROL PROTOCOLS   **03 hrs**
Flow Control; Error Control; High-Level Data Link Control (HDLC).
I (7.1, 7.2, 7.3)

MULTIPLEXING   **04 hrs**
Frequency-Division Multiplexing; Synchronous Time-Division Multiplexing; Statistical Time-Division Multiplexing.
I (8.1, 8.2, 8.3)

UNIT V

CIRCUIT SWITCHING AND PACKET SWITCHING   **02 hrs**
Switched Communications Networks; Circuit Switching Networks; Packet-Switching Principles.
I (10.1, 10.2, 10.5)

ROUTING IN SWITCHED NETWORKS   **03 hrs**
Routing in Packet-Switching Networks; Least-Cost Algorithms.
I (12.1, 12.3)

CONGESTION CONTROL IN DATA NETWORKS   **02 hrs**
Effects of Congestion; Congestion Controls.
I (13.1, 13.2)

UNIT VI

LOCAL AREA NETWORK OVERVIEW   **04 hrs**
Background; Topologies and Transmission Media; LAN Protocol Architecture; Bridges.
I (15.1, 15.2, 15.3, 15.4)

HIGH-SPEED LANs   **02 hrs**
The Emergence of High-Speed LANs; Ethernet.
I (16.1, 16.2)

WIRELESS LANs   **02 hrs**
Overview; Wireless LAN Technology.
I (17.1, 17.2)

UNIT VII

INTERNETWORK PROTOCOLS   **07 hrs**
Basic Protocol Functions; Principles of Internetworking; Internet Protocol Operation; Internet Protocol; IPv6.
I (18.1, 18.2, 18.3, 18.4, 18.5)

UNIT VIII

INTERNETWORK OPERATION   **03 hrs**
Multicasting; Routing Protocols.
I (19.1, 19.2)

TRANSPORT PROTOCOLS   **03hrs**
TCP; UDP.
I (20.2, 20.4)

INTERNET APPLICATIONS   **02 hrs**
Electronic Mail: SMTP and MIME.
I (22.1)

Text Book:
 I. Data and Computer Communications, Eight Edition (2007), William Stallings, Pearson Education Low Price Edition.

Reference Book:
1. Data Communications and Networking, Fourth Edition (2006), Behrouz A. Forouzan, Tata McGraw-Hill Special Indian Edition.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE70   **OBJECT ORIENTED PROGRAMMING WITH C++**

UNIT I
OBJECT-ORIENTED PROGRAMMING CONCEPTS   **08 hrs**
Software Evolution, Procedure-oriented Programming, Object-oriented Programming, Object-oriented Languages

LANGUAGE CONSTRUCTS
Introduction, Hello World Program, C++ Program Structure, Accepting User Input, Identifiers, Literals, Keywords, Data Types, Operators in C++, Program Statements
I (1, 2)

UNIT II
ADVANCED CONSTRUCTS   **07 hrs**
Arrays, Multidimensional Arrays, Pointers, Structures
I (3)

UNIT III
CLASSES IN C++   **08 hrs**
Introduction, Data Type – Class, Declaring and Using Classes, Dynamic Objects, Defining Member Functions, Static Data Members and Functions

MEMBER FUNCTIONS
Passing Parameters, Constant Parameters, Default Parameters, Friend Functions
I (4, 5)

UNIT IV
OPERATOR OVERLOADING   **07 hrs**
Adding 'Meaning' to Operators, Syntax for Operator Overloading, Overloading Arithmetic Operators, Overloading Complex Operators, What cannot be Overloaded?

CONSTRUCTORS AND DESTRUCTORS
Defining Constructor, Multiple Constructors, Using Parameterized Constructors in Dynamic Objects, Constructors with Default Arguments, Default Constructor, Copy Constructor, Class Destructor
I (6, 7)

UNIT V
INHERITANCE   **08 hrs**
What is Inheritance, Single Inheritance, Access Modifiers, Multiple Level Inheritance, Public / Non-public Derivations, Types of Inheritance, Calling Sequence for Constructors and Destructors

MULTIPLE INHERITANCE
Multiple Inheritance – An Illustration, Constructor Calling Sequence, Destructor Calling Sequence, Parameter Passing to Base Class Constructors, Access Modifiers, Protected Inheritance, Virtual Classes
I (8, 9)

UNIT VI
POLYMORPHISM   **08 hrs**
The Meaning of Polymorphism, Types of Polymorphism, Static Polymorphism, Dynamic Polymorphism, Virtual Functions

HANDLING EXCEPTIONS
Exceptional conditions, The Try/Catch/Throw Constructs, Throwing Exceptions, Rethrowing Exceptions
I (10) (Mentioned topics in 11)

UNIT VII

TEMPLATES   **07 hrs**

Need for Templates, Types of Templates, Function Templates, Class Templates, User-defined Data Types as Parameters

I (12)

UNIT VIII

C++ I/O   **07 hrs**

The C++ I/O Systems, Streams, File I/O, Random Access Files

I (13)

Text Book:

I.   Object-oriented Programming with C++, Poornachandra Sarang, PHI, 2004

Reference Book:

1.   Big C++, Cay Horstmann, Timothy A. Budd, Wiley India, 2005

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE71   **POWER ELECTRONICS**

UNIT I
POWER ELECTRONICS   **03 hrs**
Introduction; What is Power Electronics?; Why Power Electronics?; Power Semiconductor Switches; Power Losses in Real Switches; Types of Power Electronics Circuits; Applications of Power Electronics.
I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7)

POWER DIODES   **04 hrs**
Introduction; The PN Junction Diode; The Voltage-Current Characteristic of a Diode; The Ideal Diode; The Schottky Diode; Diode Circuit Analysis; Diode Losses; Principal Ratings for Diodes; Diode Protection; Testing a Diode; Series and Parallel Operation of Diodes.
I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11)

UNIT II
POWER TRANSISTORS   **07 hrs**
Introduction; Power Bipolar Junction Transistors (BJTs); Power Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs); Insulated-Gate Bipolar Transistors (IGBTs); Unijunction Transistors (UJT).
I (3.1, 3.2, 3.3, 3.4, 3.5)

UNIT III
THYRISTOR DEVICES   **08 hrs**
Introduction; The Silicon Controlled Rectifier (SCR); SCR Characteristic Curves; Testing SCRs; SCR Ratings; Junction Temperature Rating; Increasing SCR Ratings; Series and Parallel SCR Connections; Power Loss; SCR Protection; Gate Circuit Protection; SCR Gate-Triggering Circuits; Triggering SCRs in Series and in Parallel; SCR Turn-Off (Commutation) Circuits; Other types of Thyristors.
I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10, 4.11, 4.12, 4.13, 4.14, 4.15)

UNIT IV
SINGLE-PHASE CONTROLLED RECTIFIERS   **07 hrs**
Introduction; Half-Wave Controlled Rectifiers; Full-Wave Controlled Center-Tap Rectifiers; Full-Wave Controlled Bridge Rectifiers; Half-Controlled or Semi-Controlled Bridge Rectifiers; Dual Converters.
I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6)

UNIT V
THREE-PHASE CONTROLLED RECTIFIERS   **08 hrs**
Introduction; Half-Wave (Three-Pulse) Controlled Rectifiers; Full-Wave (Six-Pulse) Controlled Bridge Rectifier; Full-Wave Half-Controlled Bridge Rectifiers with FWD.
I (8.1, 8.2, 8.3, 8.4)

UNIT VI
DC CHOPPERS   **07 hrs**
Introduction; The Principles of Basic DC Choppers; Step-Down (Buck) Choppers; Step-Up (Boost) Choppers; Buck-Boost Choppers.
I (9.1, 9.2, 9.3, 9.4, 9.5)

UNIT VII
INVERTERS   **08 hrs**
Introduction; The Basic Inverter; Voltage Source Inverters (VSI); Pulse-Width Modulation (PWM); Pulse-Width Modulated (PWM) Inverters; Other Basic Types of Single-Phase Inverters; The Ideal Current Source Inverter (CSI).
I (10.1, 10.2, 10.3, 10.5, 10.6, 10.7, 10.9)

UNIT VIII

AC VOLTAGE CONTROLLER   **05 hrs**
Introduction; AC Power Control; Integral Cycle Control; AC Phase Control; Cycloconverters.
I (11.1, 11.2, 11.3, 11.4, 11.7)

STATIC SWITCHES   **03 hrs**
Introduction; Comparison of Static and Mechanical Switches; Static AC Switches; Three-Phase Static Switches; Hybrid Switches; The Solid State Relay (SSR); Static Tap-Changing Control; The Static VAR Controller (SVC).
I (12.1, 12.2, 12.3, 12.4, 12.5, 12.6, 12.7, 12.8)

Text Book:
 I. Power Electronics for Technology, First Impression (2006), Ashfaq Ahmed, Purdue University - Calumet, Pearson Education.

Reference Book:
1. Power Electronics – Circuits, Devices and Applications, Third Edition (2004), Muhammad H. Rashid, Prentice Hall of India Pvt. Ltd.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE94   **ANALOG & DIGITAL COMMUNICATIONS LAB**

List of Experiments

1. **Passive Attenuators:** T and π type – Design and study of attenuators for the given attenuation, source and load impedances.
2. **1st Order Active Filters:** Low pass and High pass – Design for a given cutoff frequency, passband gain and to obtain frequency response curve.
3. **Class C Tuned Amplifier:** Design for a particular tuned frequency, plot of Efficiency Vs Load and to obtain optimum load.
4. **Collector Amplitude Modulation:** Display of AM output, calculation of modulation index.
5. **AM Detector using Envelope Detector:** To study the variation of output signal amplitude and AVC output with variations in AF input.
6. **DSBSC generation using Diodes:** Study of output waveforms for variations in the input.
7. **FM Modulation:** Study and display of waveforms.
8. **FM Detection:** Study and display of waveforms.
9. **PAM:** Generation and demodulation – Observe input and output waveforms.
10. **PWM:** Generation for the given analog frequency and study of PWM output.
11. **OPAMP preemphasis and deemphasis:** Design for a given time constant and plot of Gain Vs Frequency.
12. **Transistor Mixer:** Demonstration of mixing action of RF and oscillator frequency to produce IF, to obtain conversion trans-conductance of the mixer.
13. **Verification of sampling theorem** using natural / flat top sampling.
14. **Generation and Detection of ASK:** Study and display of waveforms.
15. **Generation and Detection of PSK:** Study and display of waveforms.
16. **TDM:** Study of TDM and recovery of two band limited signals.

Note: Minimum of 14 experiments to be conducted.

DE64   **PROJECT WORK**

DE64

PROJECT WORK

GENERAL GUIDELINES – PROJECT (DiplETE)

Eligibility

1.   For Eligibility, students may refer para 27

Registration

2.   Eligible students are required to forward their applications for registration of Project Work to the respective IETE Centres/Sub Centres where the examinations are conducted. The applications should include the synopsis of the Project Work, guide's bio-data and his willingness letter to guide the student, along with requisite project fees. Applications for the project must be submitted by the students within 3 weeks after declaration of the result but not later than 05 April / 05 October respectively.

Mid Term Examination

3.   Students can appear in mid term examination (viva voce) of project after three months from the date of project Registration.

Preparation and Submission of Project Reports

4   A student is expected to put in at least 6-hours/week spread over a period of 12 weeks for the project after the same has been approved by the Expert Group.

5.   Two bound copies of the project report are required to be submitted by the student (one copy for Evaluation board & one copy for IETE HQ record) to their respective Centres who will intimate the date, time and venue for appearing before the Evaluation Board & presentation of the Project Work by the student.

Evaluation Board

6.   The Regional Evaluation Board already set up for scrutinizing of the proposals will also form the Evaluation Board for assessment of the final Project Reports with one of the member acting as Chairman of the Evaluation Board. **IETE Centre will only act as facilitator and are not to be associated with the Examination Work**

7   The following points are required to be checked by the Evaluation Board at the time of assessment of the Project Reports.

    (a)   **Incorporation of requisite data in final report.** If the project proposal had been accepted conditionally, Expert Group will ensure that the conditions indicated by the group have been met in entirety.

    (b)   **Time Limit.** The Project Report is required to be completed within a period of one year from the date of approval of the project.

    (c)   **Project Report.** The Project Report should contain the following certificate from the guide:-

CERTIFICATE

This is to certify that this is a bonafide record of the Project Work done satisfactorily at _____ by Mr/Ms. _____ in partial fulfilment of his/ her DipIETE Examination. This report has not been submitted for any other examination and does not form part of any other course undergone by the candidate.

(Signature, Name, Designation
and Address of the Guide with the seal of
the Organization/Institution/Laboratory)

8. **Project Fee**

Project Fee at present is Rs. 1100/-, which is required to be submitted by the student while forwarding his/ her application for the project work. The DD of requisite amount is to be drawn in favour of the IETE Centre.

DE99   **COMMUNICATION SKILLS AND TECHNICAL WRITING**

<div align="center">UNIT I</div>

COMMUNICATION: ITS TYPES AND SIGNIFICANCE   **05 hrs**

Basic Concepts of Communication; Process of Communication; Types of Formal communication; The Media of Communication; Channels of Communication; Barriers in Communication; How to Overcome Barriers to Communication.
I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6)

<div align="center">UNIT II</div>

GRAMMAR   **06 hrs**

Synonyms; Antonyms; Words used as different parts of speech; Spotting errors; Principle of proximity between subject and verb.
I (4.1 to 4.3, 4.6, 4.8)

<div align="center">UNIT III</div>

SYNTAX   **07 hrs**

Sentence Structure; Combination and Transformation of sentences; Verb Patterns in English.
I (5.1 to 5.4)

<div align="center">UNIT IV</div>

READING SKILLS   **05 hrs**

Purpose and Process of Reading; Reading Tactics; Reading Comprehension; Paraphrase; Preparing outlines of paragraph/text.
I (2.1 to 2.3, 2.6, 2.10, 2.11)

<div align="center">UNIT V</div>

WRITING SKILLS   **07 hrs**

Elements of Effective Writing; Job Application, Bio-data, Personal Resume and Curriculum Vitae; Writing Styles; Scientific and Technical Writing; Summary Writing; Writing paragraphs; Writing Essays.
I (3.1, 3.2, 3.5, 3.6, 3.8, 3.9, 3.11)

<div align="center">UNIT VI</div>

LISTENING SKILLS   **06 hrs**

Process of Listening; Hard and Soft Skills; Feedback Skills; Essentials of Good Communications; Types of Listening; Barriers to Listening.
I (8.1 to 8.4, 8.6 to 8.8)

SPEAKING SKILLS

Skills of Effective Speaking; Component of an Effective Talk; Tone of Voice; Body Language; Timing and Duration of Speech; Audio-Visual Aids in Speech.
I (9.1, 9.2, 9.4 to 9.7)

<div align="center">UNIT VII</div>

TECHNICAL REPORT   **06 hrs**

Main considerations in writing a good report; Types and Structure of Reports; Collecting Data; Visual Aids; General Tips for Writing Reports.
I (12.1 to 12.4, 12.8, 12.9)

<div align="center">UNIT VIII</div>

SELF DEVELOPMENT   **06 hrs**

Know yourself; Tips for giving an Interview; Body language for Interviews; Group Discussion; Skills of participating in meeting; Attending Calls.
I (10.1 to 10.4, 10.6)

Text Book
 I. The Functional Aspects of Communication Skills, Prajapati Prasad and Rajendra K. Sharma, S. K. Kataria & Sons, New Delhi, Reprint 2007.

Reference Books :
1. Business Communication, Sinha K. K, S. Chand, New Delhi.
2. Business Communication, Asha Kaul, Prentice Hall of India.
3. Business Correspondence and Report Writing: A Practical Approach to Business and Technical Communication, Sharma, R.C. and Krishna Mohan, Tata McGraw-Hill.
4. A New Approach to English Grammar for High Schools, Madan Sabina, Spectrum Books, New Delhi.

NOTE: Examination procedure.
Theory - consists of written examination for 70 marks.

Oral Test - consists of an Oral Test to test the Communication Skills which includes an oral presentation on any subject, of the choice of students (e.g. About IETE, General knowledge topics etc). This presentation need not be on technical subject. This test carries 30 marks.

Annexure 'I'

No.F.24-7/2002-TS.III
Government of India
Ministry of Human Resource Development
Department of Secondary & Higher Education
* * * * * * * * *

New Delhi, the 10th January, 2006

To

The Secretary General,
Institution of Electronics & Telecommunication Engineers,
Delton House, Lodhi Road,
New Delhi -

Subject:-   Permanent recognition to the Diploma in Electronics and
Telecommunication Engineering (DIPIETE – ETE) run by the
Institution of Electronics and Telecommunication Engineers, New
Delhi.

Sir,

I am directed to inform that the issue of permanent recognition was
discussed by the High Level Committee in its 9th meeting held on 16.11.2005.
While giving the approval to the permanent recognition to the course namely,
Diploma in Electronics and Telecommunication Engineering run by IETE, the
Committee took the policy decision as under:-

"Henceforth, the recognition to the courses, granted by the High Level
Committee shall be permanent till it is withdrawn either due to deficiencies
identified by AICTE or the genuine complaints received against the Institutions."

The Institution is required to put all the details about their educational
activities on the website of the All India Council for Technical Education in the
format prescribed for the purpose. AICTE can conduct a random review of the
courses run by the Institutes to ascertain the standard and level.

Yours faithfully,

(Dr. G. L. Jambhulkar)
Deputy Educational Advisor (NIT)
Tel: 2338 4276
Fax No. 233 84 345
E-mail: technicalsection3@yahoo.co.in

Annexure 'II-A'

<div align="center">

GOVERNMENT OF KARNATAKA

</div>

No. BTE 36 ERS (2) 92   Office of the Secretary,
Board of Technical Examinations,
Bangalore-1,

Dated 22.12.1992.

To

The Secretary,
Institute of Electronic & Telecommunication,
No.2, Institutional Area,
Lodi Road,
NEW DELHI.

Sir,
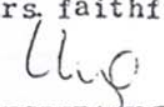
     Sub:- Recognisation by Government of India of
           Diploma Level Examination in Electronic
           conducted by your Institution.

     Ref:- 1. Notification 38 (F.18-9/89 TD-V dt.5.8.92
           of Govt. of India, Ministry of Human Resource
           Development, New Delhi.

           2. G.O.No. GAD 35 SRR 64 dt.20th April 1965
           of Govt. of Karnataka.

I wish to inform you that the Diploma in Electronic
conducted by your institution has been recognised by Government
of India (vide ref. 1). Hence, the Diploma in Electronic
conducted by your institution stands atomatically recognised
by Government of Karnataka as per Karnataka Government Order
cited under reference(2).

Yours faithfully,

SECRETARY,
BOARD OF TECHNICAL EXAMINATIO
BANGALORE

GOVERNMENT OF RAJASTHAN

BOARD OF TECHNICAL EDUCATION,RAJ.JODHPUR

NO.F5(7-11)A/Gen/BTE/99/ 7957   Dated: 30/10/9

Asstt. Secretary(ACAD)

The Institution of Electronics

and Tele communication Engineers,

Institutional Area, Lodi Road,

New Delhi-110003

Sub:Recognition of Diploma I.E.T.E
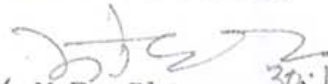
Ref:IETE/769/Exam/99 Dt.16.6.98

Sir,

    It is to inform you that Govt. of Rajasthan Department of Technical Education as per there order No P.1(10) T.E./92 dated 13.10.99(Copy enclosed) has recognised the Diploma in electronics and Telecumminaction awarded by you as equivalent to 3 years Diplome course awarded by this Board.

Yours Faithfully

(M.D. Bhargava 30/10/98)

Dy. Director(conf.)

Encls:As above

68

Annexure 'II-C'

WEST BENGAL STATE COUNCIL OF TECHNICAL EDUCATION
(A Statutory Body Under West Bengal Act XXI of 1995)

No. 1063-SC(T)E   Date 10th Oct., 2002.

From : The Secretary,
W.B.State Council of Tech.Education.
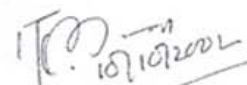
To : The Director, Academic
The Institution of Electronics & Tele-Communication
Engineers (Calcutta Centre),
Salt Lake Electronics Complex,
EP Block, Plot No.JI-7,Sector-V,
Kolkata- 700091.

Sub :- Recognition of Diploma IETE(Diploma Level)in the
field of Electronics & Tele-Communication Engg.

Ref :- Your letter No.IETE/Cal/Recog-SCTE/2001/2002.

It appears that the Diploma level examination in Electronics
conducted by the Institution of Electronics & Tele-Communication
Engineers is recognised by the MHRD, Government of India for the
purpose of employment of posts and services under the Central Govern-
nment in the appropriate field.

In this connection it is intimated that according to existing
procedure any course recognised by Government of India in the
Ministry of Human Resource Development is also recognised by All
State Governments/Union Teretories and as such no further recognition
notification is required to be issued from this end.

(R. C. BHATTACHARYA)
Secretary,
W.B.State Council of Tech. Education.

प्रेषक,

तकनीकी शिक्षा आयुक्त एवं विशेष सचिव,
हरियाणा सरकार, तकनीकी शिक्षा विभाग,
चण्डीगढ ।

सेवा में,
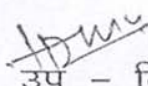
प्रधान सचिव,,
इलैक्ट्रोनिक्स एवं टैलीकम्यूनिकेशन इंजीनियर संस्थान,
2, इंस्टीच्यूशनल ऐरिया, लोदी रोड़,
नई दिल्ली 110 003

यादी कमांक 95 /शैक्षिक,
दिनांक : 18-2-23

विषय :   **Regarding – Recognition of Diploma by Haryana
Govt.**

उपरोक्त विषय पर आपके यादी कमांक : आई.ई.
टी.ई.769/2002/दिनांक 11.12.02 के संदर्भ में ।

2.   इस सम्बन्ध में सूचित किया जाता है कि जो
डिप्लोमा/डिग्रीयां भारत सरकार तथा अखिल भारतीय तकनीकी
शिक्षा परिषद द्वारा मान्यता प्राप्त है वही डिप्लोमे हरियाणा राज्य
द्वारा भी मान्यता प्राप्त हैं ।

उप – निदेशक,
कृतेःतकनीकी शिक्षा आयुक्त एवं
विशेष सचिव, हरियाणा सरकार,
तकनीकी शिक्षा विभाग, चण्डीगढ
7/2/03

ABSTRACT

The Institution of Electronics and Telecommunication Engineers (IETE) conducted by The Institution of Electronics and Telecommunication Engineers, New Delhi. Recognised as equivalent to Diploma in Electronics and Communication Engineering awarded by State Board of Technical Education and Training Tamilnadu. Orders issued.

HIGHER EDUCATION (B2) DEPARTMENT

G.O. Ms. No. 249   DATED: 23.12.02
                                                                              READ

From the Secretary General, the IETE, New Delhi Letter No.IETE/249/Recognition/Te dated 14.11.2000

From the Director of Technical Education Lr No. 6000/CDC/2001 dated 2.1.2001

From the Secretary, Tamil Nadu Public Service Commission, Letter No. 5630/RI/A1/2002, dated 17.6.2002

****

ORDER.

The Secretary General of the Institution of Electronics and Telecommunication Engineers, New Delhi has requested this Government to accord recognition to the Diploma in Electronics and Telecommunication awarded by the Institution of Electronics and Telecommunication Engineers, New Delhi as equivalent to Diploma in Electronics and Communication Engineering awarded by the State Board of Technical Education and Training, Government of Tamilnadu, for the purpose of Employment under Tamilnadu Government.

2.   The above matter was placed before the Committee of recognition for its decision. The Secretary, Tamil Nadu Public Service Commission in his letter cited has stated that the Committee of recognition has recommended to consider the Diploma in Electronics and Telecommunication awarded by the IETE, New Delhi as equivalent to Diploma in Electronics and Communication Engineering awarded by the State Board of Technical Education, Tamilnadu for the purpose of employment and services under Tamilnadu Government for a period of three years from 2001 based on the Ministry of Human Resources Development Recognition.

3.   The Government accordingly direct that, the Diploma in Electronics and Telecommunications awarded by the Institution of Electronics and Telecommunication Engineers, New Delhi be provisionally recognised as equivalent to the Diploma in Electronics and Communication Engineering awarded by the State Board of Technical Education and Training, Tamilnadu for the purpose of employment and services under Tamilnadu Government for a period of three years from 2001 and the recognition accorded may be reviewed after three years.

(BY Order of the Governor)

R. SRIRAM
SECRETARY TO GOVERNMENT

To
The Director of Technical Education, Chennai - 25
The Secretary General, The Institution of Electronics and Telecommunication Engineers, New
Delhi, 2, Institutional Area, Lodi Road, New Delhi - 110 003
The Secretary, Tamil Nadu Public Service Commission, Chennai -2
The P.S to Secretary, Higher Education Department, Chennai -9
The O.S / U.S to Government (Technical Education) Higher Education Department Chennai-9
Copy to   The Personnel and Administrative Reforms Department, Chennai. 9
//FORWARDED/BY ORDER//

Annexure 'E'

GUJARAT UNIVERSITY

No. Exam/3A/Eli/637 0 /2002   Date : 12/9/2002

To,

The Chair Person,
I.E.T.C. 4 — IETE
206, Umiya Shopping Centre
Satelite Road,
Ahmedabad-380 015

Sub:- Recognition of AMIETE/DIPIETE
Course.

Madam,

With reference to your letter No. IETE/Ch/2/2001
dated 6/12/2001 on the subject mentioned above, I am to
inform you that on the recommendation of the Standing
Committee on equivalence of examination of the University
held on 26/8/2002. It has been resolved that the examinations
of AMIETE/DIPIETE are recognized as equivalent to S.E./Degree
examination by this University.

Thanking you.

Yours faithfully,

Registrar

UNIVERSITY OF CALICUT

(Abstract)

Recognition of Diploma in Electronics and Telecommunication Engineering regular Diploma awarded by Institution of Electronics and Telecommunication Engineers, New Delhi as equivalent to 3 years Diploma awarded by State Board of Technical Education – Granted – Orders issued.

GENERAL AND ACADEMIC BRANCH – I 'A' SECTION
No.GAI/A1/6988/05   Dated, Calicut University P.O, 12.08.2009.

Read: 1. Minutes of the meeting of Board of Studies in Electrical, Electronics and Communication Engineering, Instrumentation and Control Engineering Applied Electronics and Instrumentation Engineering (UG) held on 30-03-2006, item No.4.
2. Minutes of the meeting of Faculty of Engineering held on 06-06-2006 item No.5.
3. Minutes of the meeting of Academic Council held on 05-04-08 item No.B-5.

ORDER

The meeting of the Board of Studies in Electrical, Electronics and Communication Engineering, Instrumentation and Control Engineering Applied Electronics and Instrumentation Engineering (UG) held on 30-03-2006, vide paper read first, considered, the recognition of Diploma in Electronics and Telecommunication Engineering (regular Diploma) awarded by the Institution of Electronics and Telecommunication Engineers, New Delhi, and decided to recognise the same as equivalent to 3 years diploma awarded by State Board of Technical Education.

The meeting of Faculty of Engineering held on 06.06.2006 and the Academic Council held on 05.04.2008 as paper read 2nd and 3rd above, approved the decision of the Board of Studies.

Sanction has therefore been accorded to recognise the regular Diploma in Electronics and Telecommunication Engineering awarded by the Institution of Electronics and Telecommunication Engineers, New Delhi as equivalent to 3 years Diploma awarded by State Board of Technical Education.

Orders are issued accordingly

Sd/

DEPUTY REGISTRAR (G&A-I)
For REGISTRAR

To

K.M. Ajas
Karimbil Manalath (H),
Mundathicode (PO),
Trichur – 680595.

Copy to:
1. The Assistant Secretary (Acad)
   Institute of Electronics & Telecommunication Engineers, New Delhi.
2. The Controller of Examinations
3. Director, Technical Education, Government of Kerala
4. Entrance Commissioner, Trivandrum
5. E.R.D.I.
6. GAI/'E' Section
7. PS to VC/PA to PVC/PA to Registrar
8. SF/DF/FC

Forwarded By Order

SECTION OFFICER

From

      The Director,
      Technical Education, U.T.
      Chandigarh.

To

      The Secretary,
      Institution of Electronics &
      Telecommunication Engineers,
      2, Institutional Area Lodi Road,
      New Delhi-110003

      Memo. No. F. 213/EA(P&ED)-90/
      dated, Chandigarh, the

Subject: Recognition of Diploma Level Examination in
      Electronics and Telecommunication conducted
      by the Institution of Electronics and
      Telecommunication Engineers, New Delhi.

      Reference your letter no. IETE/Dip/Exam/92/
dated 21.10.92, on the subject noted above.

      In this connection, it is intimated that the
notification regarding recognition of diploma course cited
as subject accorded/received from the Govt. of India,
Ministry of Human Resource Development, New Delhi
is applicable to all state Govt./Union Territories as
such no further recognition notification is
required to be issued by this Directorate.

                    Director Technical Education,
                    Union Territory, Chandigarh.

भारत सरकार
विज्ञान और प्रौद्योगिकी मंत्रालय
वैज्ञानिक और औद्योगिक अनुसंधान विभाग
टैक्नोलॉजी भवन, नया महरोली मार्ग, नई दिल्ली-110016
GOVERNMENT OF INDIA
MINISTRY OF SCIENCE & TECHNOLOGY
Department of Scientific & Industrial Research
Technology Bhawan, New Mehrauli Road,
New Delhi-110016

तार/Telegram	:	SCIENCTECH / SCINDRECH
दूरभाष/Telephone	:	6567373, 6562134, 6562122,
		6562123, 6562125, 6562128
		6562160 (EPABX)
फैक्स/Fax	:	6960629, 6868607, 6962955
ई मेल/Email	:	

No. 11/274/92-TU-V   **(Registered)**   **Dated: 4 October, 2006**

The Secretary General
The Institution of Electronics and
Telecommunication Engineers
2, Institutional Area
Lodi Road
New Delhi – 110 003

Subject: Renewal of recognition of Scientific and Industrial Research Organisations (SIROs).

Dear Sir,

This has reference to your application for renewal of recognition of **The Institution of Electronics and Telecommunication Engineers, New Delhi,** beyond 31.3.2006 by the Department of Scientific & Industrial Research under the Scheme on Recognition of Scientific and Industrial Research Organisations (SIROs) – 1988.

2.   This is to inform you that it has been decided to accord renewal of recognition to **The Institution of Electronics and Telecommunication Engineers, New Delhi,** from **01.04.2006** to **31.03.2009.** The recognition is subject to terms & conditions mentioned overleaf.

3.   Receipt of this letter may kindly be acknowledged.

Yours faithfully,

(R. R. Abhyankar)
Scientist 'G'

72

RECOGNITION BY GOVERNMENT OF INDIA/STATE GOVERNMENTS/UNIVERSITY

GOVERNMENT OF INDIA

| 1. | Government of India | - | No. F.8-18/95-TS-IV/TS.IIIA dt. 25.09.2000 |

STATE GOVERNMENTS/UNIVERSITY

1.	Govt. of Rajasthan	-	No. F5(7-11)A/Gen/BTE/99/7957 dt. 30.10.1999
2.	Govt. of Karnataka	-	No. BTE 36 ERS (2) 92 dt. Nil
3.	UT of Chandigarh	-	No. F.213.EA (P&EC)- 92
4.	Govt. of Tamil Nadu	-	G.O Ms No. 249 dated 23.8.2002
5.	Govt. of West Bengal	-	No. 1063-SC (T) E dt 10.10.2002
6.	Govt. of Haryana	-	No. 95 dt. 13.02.2003
7.	Govt. of Kerala	-	No. 20795/L-2/05/HED
			Dt. Thiruvananthapuram 9.12.2005
8.	Gujarat University	-	No. Exam/3A/Eli/6310/2002 dt 12./9/2002
9.	University of Calicut	-	No.GAI/AI/6988/05 dated Calicut University P.O., 12.08.2009

TRANSITION FROM OLD SYLLABUS TO REVISED SYLLABUS

1.1   General Guide Lines

1.1.1   The existing syllabi for DiplETE (all streams) have been revised and upgraded. The revised syllabi have been implemented w.e.f June 2009 examination.

1.1.2   The old syllabus will be followed upto Dec 2010 examinations. The students who are unable to clear their DiplETE examinations under old syllabi will automatically stand transferred to revised syllabi after Dec 2010 examinations.

1.1.3   Revised syllabus of DiplETE consists of 15 Theory Papers, 4 Lab Examinations, Project and 1 paper on Communication Skills and Technical Writing Accordingly, a student transiting from old syllabus to revised syllabus shall have to meet the criteria of revised syllabus. However, any paper passed in the old syllabus will be considered   in the revised syllabus and thus in the new syllabus a student , may not be required to pass more than 15 theory papers for DiplETE in the new syllabus . Only in exceptional cases as given in the examples, a student may be required to do the additional paper. Similarly, in the Lab Examination also a student will not be required to do the Lab Examination which he has done in the old syllabus.

1.1.4   The revised syllabus is more students friendly. To help the students for their smooth transition from old syllabi to revised syllabi the following procedure shall be adopted:-

(a)   The subjects of the new syllabus having one to one correspondence in the old syllabus which a student is exempted from /passed will be considered exempted /passed in the new syllabus as well.

(b)   The revised syllabus consists of core subjects and non core subjects in each part. It is mandatory to pass all the core subjects whether transiting from old syllabus to revised syllabus or pursuing only the revised syllabus.

(c)   If a student has passed a subject in old syllabus which is equivalent to core subject in the revised syllabi, he would be considered having passed the subject and will not be required to appear in that subject again. However, in those cases where a subject passed in old syllabi is having no equivalence in the revised syllabi a student will be given credit, in the relevant part for non-core subject only.

(d)   In few cases where a student has passed core or non core subject of a part and in addition has done some subjects which are not there in the revised syllabi, such subjects will be considered as additional subjects. In such cases, for calculating overall grading, the best will be considered, whether they are core, non-core or non equivalent subjects.

(e)   Where 2 subjects from old syllabus are merged into one subject in the revised syllabus, and if the student has passed both the subjects under old syllabus he/she will be given credit of having passed, two papers. In case, the student has passed only one subject out of two in the old syllabi he/she will have to pass the other subject before Dec 2010 exam. In this case, the subject passed in old syllabi will be shown as additional subject and shall not count towards CGPA.

(g)   From Dec 2010 onwards, no examination will be conducted for Elective subjects listed in the old syllabus. Thereafter, the student shall have to appear for the elective subjects from the list of Electives given in the revised syllabus only .

(h)   If an elective subject in the old syllabus is compulsory in the revised syllabus, a student having passed such an elective subject will be deemed to have passed the compulsory paper in revised syllabus.

(i)   **Project** passed in the old syllabus will be treated as passed in the new syllabus also.

(j)   **Lab–DiplETE(ET)** Lab-I (DL01) of old syllabus is not granted any equivalent Lab in the revised syllabus. Therefore students will have to pass lab-I (DE91) in the revised syllabus even if he/ she has passed Lab-I in the old syllabus. Also, those who have passed Lab-II of old syllabus will be exempted in DE92 and DE94 of the revised syllabus.

IETE ACADEMIC AWARDS

IETE has instituted the following academic awards for excellence for AMIETE students to be awarded every year. Awardees are intimated sufficiently in advance and are invited to receive these prestigious awards during students' session of the Annual Technical Convention of IETE. The award consists of a medal and a citation. Details of awards are given below:

DIPIETE Council Award-I for securing the highest percentage with 6.5 CGPA and above grade and completing Part-I of Section A in one attempt without any exemptions.

DIPIETE Council Award-II for securing the highest percentage with 6.5 CGPA and above grade and completing Part-II of Section A in one attempt without any exemptions.

DIPIETE Council Award-III for securing the highest percentage with 6.5 CGPA and above grade and completing Part-I of Section B in one attempt without any exemptions.

DIPIETE Council Award-IV for securing the highest percentage with 6.5 CGPA and above grade and completing Part-II of Section B in one attempt without any exemptions.

DIPIETE Council Award-V for securing the highest percentage with 6.5 CGPA and above grade and completing DIPIETE in 3 years without any exemptions.

DipIETE - Gopal M Dandekar Memorial Award to a girl student for securing the highest percentage with 6.5 CGPA and above marks and completing DipIETE (considering ET & CS streams of current June and previous Dec exams together) in three years without any exemptions.

IETE CENTRES

AHMEDABAD 206, Umiya Vijay Shopping Centre,
Satellite Road,
AHMEDABAD – 380 015.
Ph : 079-26753938
Fax : 079-26733931
Email : ahmedabad@iete.org

ALIGARH Flat No 1&2, 1st Floor
Shah Residency,
Medical Raod,
ALIGARH-202 002
Ph : 0571-270190
Email : aligarh@iete.org

ALLAHABAD C/o J K Institute of Applied Physics,
& Technology
University of Allahabad,
ALLAHABAD – 211 002.
Ph : 0532-2460442
Fax : 0532-2460443
Email : allahabad@iete.org

AMRAVATI 45, Anand, Ganediwal Layout, Camp,
AMRAVATI – 444 602
Ph : 0721-2663908
Email : amravati@iete.org

AURANGABAD C/o Deptt. of Computer Science
& Information Technology,
Dr B A M University Campus,
AURANGABAD – 431 004
Ph : 0240-2403317
Fax : 0240-2403317
Email : aurangabad@iete.org

BANGALORE IETE Building, Bellary Road,
Opp Ganganagar Bus stop
BANGALORE – 560 032
Ph : 080-23331133
Fax : 080-23337231
Email : bangalore@iete.org
Website : www.ieteblr.org

BHOPAL Office Hall No. 3,
Gamantika Parisar,
Jawahar Chowk, TT Nagar,
BHOPAL – 462 003. (M.P)
Ph : 0755-2775597
M : 09425301024
Email : Bhopal@iete.org

BHUBANESWAR Room No. 4,5 & 6
IInd Floor, Barabhuja Commercial
Complex, Khandgiri Square,
BHUBANESWAR – 751 030
Ph: 0674 2384612
Email : bhubaneswar@iete.org

BURDWAN C/o Dept of physics
Burdwan University,
Gopalbag (North),
BURDWAN – 713 104.
Ph : 0342-2657800 Ext. 37
Email : burdwan@iete.org

CHANDIGARH IETE Building,
Sector 30-B (Opp. CSIO)
CHANDIGARH – 160 030
Ph : 0172-2651061
Fax : 0172-2657333
Email : chandigarh@iete.org

CHENNAI 37, Conran Smith Road,
(New No. 169)
Main Entrance Peters Road
Gopalapuram,
CHENNAI – 600 086.
Ph : 044-28350773, 28356045
Fax : 044-28350773
Email : chennai@iete.org

COIMBATORE Amrita Vishwa Vidyapeetham
Amrita University, Ettimadai,
COIMBATORE – 641 105
Ph : 0422-2656422
Fax : 0422-2656274
Email : coimbatore@iete.org

DEHRADUN C/o DEAL Campus, Riapur Road,
DEHRADUN – 248 001.
Ph : 0135-2787257, 2787083
Fax : 0135-2787265, 2787290
Email : dehradun@iete.org

DELHI 16/1-2, Institutional Area,
Pankha Road,
Janakpuri (Opp Vashisht Park),
NEW DELHI – 110 058.
Ph : 28521618
Tele-fax : 011-28520912
Email : delhi@iete.org

DHARWAD	C/o Dept of E & CE S D M College of Enng & Tech., DHARWAD – 580 002. Ph : 0836-2447465 Fax : 0836-2464638 Email : dharwad@iete.org Website :www. sdmcet.ac.in	JABALPUR	Raj Kumari Bhawan Complex, Opp.Sai Baba Mandir South Civil Lines, JABALPUR – 482 001. Ph : 0761-2623797 Email : jabalpur@iete.org
GOA	C/o ETC Deptt., Govt Engineering College, Farmagudi, Ponda, GOA-403401. Ph: 0832 2326341 Fax: 2335021 Email : goa@iete.org	JAIPUR	'D' Block Shopping Centre, 1st Floor, Malaviya Nagar, JAIPUR – 302 017 Ph : 0141-2545924 Email : jaipur@iete.org
GULBARGA	Guru Nanak Dev Engg College Mailoor Road Bidar 585403 Ph : 08482-226949 Fax : 08472-228273 Email : gulbarga@iete.org	JAMMU	7C/C Gandhi Nagar, (Near Triveni Hospital) JAMMU – 180 004. Ph : 01991-285699 Ext. 2010 Email : jammu@iete.org
GUWAHATI	3rd Floor, Eureka Tower, Chandmari, GUWAHATI - 781 003. Ph : 0361-2656166, 2571117 Email : guwahati@iete.org	KANPUR	111/457 1st Floor, Vasundhara Complex, Opp Swagat Hotel, Near Brahm Nagar Crossing, 80 Feet Road, KANPUR – 208 012. Ph : 0512-3259019 Email : kanpur@iete.org
GWALIOR	NAND Bhawan 133-Panchwati Vastra Nagar, (inside water works) Roshani Ghar Road, GWALIOR – 474 009. Email : gwalior@iete.org	KATHMANDU	C/o Nepal Telecom Training Centre Babar Mahal, PB No 5662, Kathmandu, Nepal Ph : 00977-1-4784213 Fax : 00977-1-4784220 Email : kathmandu@iete.org
HYDERABAD	Near Jama-I-Osmania Post Office Osmania University Campus, HYDERABAD – 500 007. Ph : 040-27098025 Telefax : 040-27097175 Email : hyderabad@iete.org Website : www.ietehyd.org	KOCHI	IETE House, XL/216K, Third Floor, Jewel Arcade Building, Layam Road, KOCHI – 682 011. Tele Fax : 0484-2369944 Email : kochi@iete.org
IMPHAL	IETE Building Lamphel Langol Road, IMPHAL. And C/O Manipur Police Wireless Jail Road, 1st MR Complex Imphal 795 001. Ph. 0385 2450141 Fax: 0385 2449738 Email : imphal@iete.org	KOLKATA	No. J 1-7, EP-Block, Sector – V Salt Lake Electronics Complex, Salt Lake, KOLKATA – 700 091. Tele Fax : 033-23574290 Email : kolkata@iete.org Website : ietekol.org
		LUCKNOW	Flat No. 3-D, Khushnuma Complex, 7, Meerabhai Marg, LUCKNOW – 226 001. Tele Fax : 0522-2207779 Fax : 0522-2207763 Email : lucknow@iete.org

SALEM	Dept of ECE Sona College of Techonology, SALEM-636 0005 (M) 09443590048 Ph : 044-4099777 Fax : 044-4099888 Email : salem@iete.org	TIRUPATI	4th Floor, AVR Complex, Balaji Colony, Tirupati-517 502. Ph : 09247007122 Email : tirupati@iete.org
SIVAKASI	Prof & Head Dept of ECE MEPCO Schlenk Engg College Sivakasi, VIRUDHUNAGAR-626 005 (M) 09442775282 Ph: 04562 235000 Fax: 04562 2351111 Email : sivakasi@iete.org	VADODARA	501-506, Fifth Floor, Vraj Siddhi Tower, Khanderao Market Char Rasta, Rajmahal Road, VADODARA – 390 001. Tele Fax : 0265-2422475 Email : vadodara@iete.org Website : ietevadodara.org
SHIMLA Khallini,	Saligram Bhawan, Below Reliance India Mobile, SHIMLA – 171 002. Ph : 0177-2625268 Email : shimla@iete.org	VARANASI	36, Nand Nagar Colony ITI Road, Karaundi VARANASI 211005 Ph: 09235440911 Email : varanasi@iete.org
SHIMOGA	Jawaharlal Nehru National College Of Engineering, Navile SHIMOGA 577 204 KARNATAKA Ph: 08182 276707-09 Email: shimoga@iete.org	VIJAYAWADA	Flat No. 107 & 108 Vijaya Soudha Apartments, High School Road Cross, Patamata, M.G. Road, VIJAYAWADA – 520 010. Ph : 0866-2550974 Email : vijayawada@iete.org
THIRUVENTHAPURAM	Pottakuzhy, Pattom PO THIRUVANANTHA PURAM–695 004. Ph : 0471-2554727 Fax: 2554727 Email : thiruvan@iete.org Website : ietetum.com	VISAKHAPATNAM	IETE Building, Near ECE Department, College of Engg., Andhra University, VISAKHAPATNAM – 530 003. Ph: 0891 2769547 Fax: 0891 2769547 Email : visakha@iete.org
		WARANGAL	3rd Floor, Mayuri Mall Complex Kishanpura, Karim Nagar Road, Hanmakonda WARANGAL – 506 015. Ph: 0870 2543737 Email : warangal@iete.org

MISCELLANEOUS INFORMATION
AWARD FOR DipIETE

1.1 Eligibility

1.1.1 To be eligible to get DiplETE a student is required to score a minimum grade D in individual subjects and minimum grade C in Project, Seminar & Lab examinations, and should have CGPA of 5 or more.

1.2 Procedure for obtaining Certificate of passing DiplETE Section A and B examinations.

1.2.1 Once all requirements to complete DiplETE are met, students are eligible for award of certificate.

1.2.2 Provisional Certificate/Consolidated Grade Sheet is issued on receipt of
(a) A declaration that the student would not appear for any improvement in future.
(b) A Bank draft of requisite fee for DiplETE Certificate.

1.2.3 Final Degree Certificate is sent to the student within 6 months time or handed over during Convocation Ceremony (usually held in December every year with prior information.)

1.2.4 A student on completion of DiplETE and after paying requisite fee is automatically enrolled for AMIETE examination.

1.3 Bonafide Certificate

1.3.1 Bonafide certificate authenticating student's registration with IETE, is issued to those who are yet to complete the course on a payment of Rs 100/-.

1.4 Migration & Character Certificate

1.4.1 For the purpose of admission to other Universities for higher studies ,Migration & Character certificate are also issued from IETE HQ on payment of Rs.100/-(US $20) for each

1.5 Transcripts

1.5.1 Transcripts (certifying written records) ,student's details, recognition of course passed, duration of the course, medium of instructions, required by Universities abroad. Can be obtained from IETE HQ on payment of Rs.100/- (US $ 20) for each transcript.

1.6 Duplicate Final Grade Sheet and Certificate

1.6.1 A student is required to submit an application along with the following documents, in case he requires duplicate Grade Sheet /Certificate.

(a) Fee in the form of (DD) in favour of **IETE, and New Delhi,** for Rs 500/- each for Grade sheet and certificate.
(b) An affidavit (on stamp paper of Rs 10/-) affirming and verifying the loss etc. duly signed by a notary.

1.7 Semester Grade Sheet

1.7.1 Duplicate Grade Sheet for the past semester examinations can be obtained on payment of Rs 100/- per semester.

The Institution of Electronics and Telecommunication Engineers

2, Institutional area, Lodhi Road, New Delhi-110 003

EXEMPTION APPLICATION FORM

Dear Sir/Madam,

1.   I student membership No...........................Name..of stream..........................request you to grant me exemption based on my qualification in the following subject.

Sub Code	Subject	Qualification based on which exemption asked for
(a)		
(b)		
(c)		
(d)		

(For more subjects, use photo copy of this from)

2.   A DD of Rs...............................bearing machine no..........................of ....is enclosed herewith as exemption fee.

3.   I am enclosing following documents (Photo-copies duly attested)
    (a)   Final/Provisional certificate.
    (b)   Marksheets of all semesters.
    (c)   Copy of the syllabus of the course (If not covered in _____).
    (d)   Any other document.

4.   Email address :...

5.   Phone No....................................

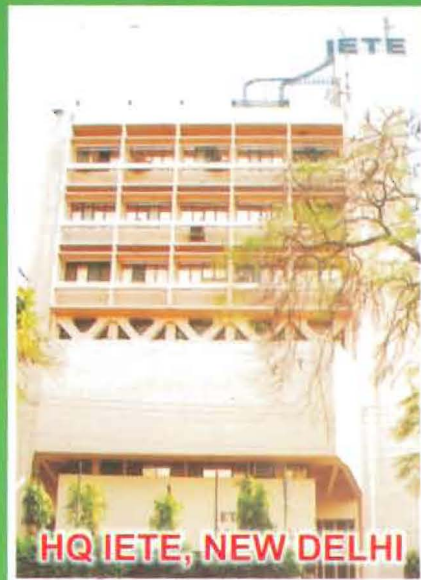   **(Signature of Student)**

Note :
1.   Fee for exemption for DipIETE, it is Rs 400/- per subject.
2.   This application is not to be clubbed with exam form.

IETE BUILDINGS

DELHI CENTRE

THIRUVANANTHAPURAM CENTRE

NOIDA CENTRE

HQ IETE, NEW DELHI

BANGALORE CENTRE

ALLAHABAD CENTRE
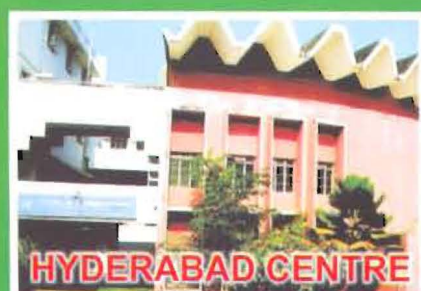
VISAKHAPATNAM CENTRE

NAGPUR CENTRE

KOLKATA CENTRE

HYDERABAD CENTRE

CHANDIGARH CENTRE

Government of India
Ministry of Human Resource Development
Department of Education

Copy of MHRD Letter No.F.24-7/2002-TS.III Dated 10th January, 2006.

To,

The Secretary General,
Institution of Electronics & Telecommunication Engineers,
Delton House, Lodhi Road,
New Delhi

Subject:- Permanent recognition to the Diploma in Electronics and Telecommunication
Engineering (DIPIETE-ETE) run by the Institution of Electronics and Telecommunication
Engineers, New Delhi

Sir,

I am directed to inform that the issue of permanent recognition was discussed by the High Level Committee in its 9th meeting held on 16.11.2005. While giving the approval to the permanent recognition to the course namely, Diploma in Electronics and Telecommunication Engineering run by IETE, the Committee took the policy decision as under.

"Henceforth, the recognition to the courses, granted by the High Level Committee shall be permanent till it is withdrawn either due to deficiencies identified by AICTE or the genuine compliants received against the Institutions."

The Institution is required to put all the details about their educational activities on the website of the ALL India Council for Technical Education in the format prescribed for the purpose. AICTE can conduct a random review of the courses run by the Institutes to ascertain the standard and level.

Yours faithfully,
Sd/-
(Dr. G. L. Jambhulkar)
Deputy Educational Advisor

Extract of Notification dated 16 Jan 2006

Extract of Notification No. F.24-7/2002 - TS.III. On the recommendations of the High Level Committe for recognition, Government of India have decided to recognize the Diploma in Computer Science & Engineering, DIPIETE (Computer Science & Engineering) conducted by the Institution of Electronics & Telecommunication Engineers, New Delhi, till further orders for the purpose of employment to the posts and services under the Central Government in the appropriate field.

The recognition will be effective from the year 2002, till further orders.