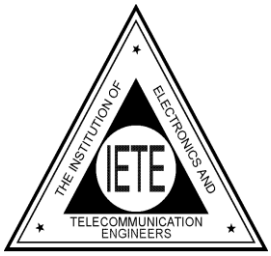
Regulations & Syllabi for DipIETE Examination (Electronics & Telecommunication)



सह वीर्यं करवावहै

Published under the authority of the Governing Council of
The Institution of Electronics and Telecommunication Engineers
2, Institutional Area, Lodi Road, New Delhi – 110 003 (India)
(2013 Edition)

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Prospectus
Containing
Regulations & Syllabi for
DiplETE Examination
(Electronics & Telecommunication)

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INTRODUCTION

The Institution of Electronics and Telecommunication Engineers (IETE), formerly the Institution of Telecommunication Engineers (ITE) was founded in 1953 by a small group of professionals for the advancement of Telecommunication and Electronics in India. Today the Institution has grown in its status to international levels with its manifold activities for furthering the cause of development in the key sectors of national economy namely Electronics, Telecommunications, Computer Science & Engineering, Information Technology and allied disciplines. The emphasis of the current activities is on creation of a concrete base of trained manpower in these fields at various levels of competence and also to contribute gainfully towards the continued professional development needs of existing technical personnel. The IETE also provides a platform for meaningful interaction among professionals from the Industry, R&D Organisations, Educational Institutions and Government Departments.

MEMBERSHIP

1. The IETE is a professional society devoted to the advancement of Electronics and Telecommunication, Computer Science Engineering and Information Technology. The Institution is headed by Governing Council, elected from its large base of corporate members in India and abroad. It confers professional status by way of admitting such persons, as may be qualified to various classes of membership such as Honorary Fellow, Distinguished Fellow, Fellow, Member, Associate Member, Diploma Member, Associate and Student Member. Organizational Membership is also open to Public/Private Sector Companies, Institutions, R&D Laboratories and Government Organizations.

OBJECTIVES

2. The IETE focuses on advancing the science and technology of electronics, telecommunications, computers, information technology and related areas. The objectives of the Institution, inter-alias includes;

- Organise conferences, symposia, workshops and brainstorming sessions involving all concerned professionals, students and industry associations for the advancement of the Disciplines.
- Provide a forum for discussion on national policies and to provide suitable inputs to policy makers.
- Promote and conduct basic engineering and continuing technical education programme for human resource development.
- Bring out quality publications for all levels of readership.
- Honour outstanding professionals.

EXAMINATIONS

3. The IETE conducts the Diploma Level (DIPIETE) Examination, in order that a student qualifies and becomes a Diploma Member. At the time of enrolment a student is enrolled as Student Diploma (SD). On successful completion of the curriculum and clearance of requisite membership fee, he is made a Diploma member of IETE. Such members are then eligible to pursue AMIETE course without paying any enrolment fee. The DIPIETE examination is recognized by the Ministry of Human Resource Development (MHRD)- **Appendix 'F'** similar recognition has also been given by several State Governments - **Appendix 'G** '.

FACILITIES FOR STUDENTS

4. The IETE helps the students by extending library facilities, laboratory assistance, and coordination of IETE Students Forums and by providing necessary guidance at its IETE Centres. To spread its many fold technical activities in all the regions of the country, IETE has established so far 65 Centres spread all over the country including a centre at Kathmandu and examination centre at Abhu Dhabi. IETE also has mutual arrangements with similar professional bodies like the Institution of Engineers (India), CSI, IEEE (USA), IEEE Com Soc and IET (UK) for availing each other's facilities for the benefit of its members.

SOLUTIONS TO QUESTION PAPERS

5. To help the students, IETE has printed solutions to Questions papers for DipIETE stream. List of subjects for which solutions are printed is available on the website www.iete.org

LABORATORY MANUAL

6. All students of DipIETE pursuing new scheme implemented from Jun 09 exams are required to procure lab-manuals and conduct their experiments and record the same in the concerned lab-manuals. The manuals of all the lab examination have been printed. Students can obtain these manuals as under:

(a) From Reception counter at IETE HQ on payment of Rs.225/- per manual without CD and Rs.300/- per manual with CD.

(b) Through post by sending a DD in favour of Secretary General, IETE payable at New Delhi towards cost of Manuals plus postal charges. The postal charge is Rs.50/- per manual.

(c) These manuals are also available at all IETE Centres. Students are advised to approach the nearby Centre for the same.

ASSISTANCE IN PLACEMENT

7. IETE makes effort to assist in the placement of students with the help of a Placement Cell established at IETE HQ, New Delhi.

RECOGNITION

8. The IETE is recognized by the Government of India as an EDUCATIONAL INSTITUTION OF NATIONAL EMINENCE. The IETE has also been recognized by the Government of India, Ministry of Science and Technology, Dept. of Scientific and Industrial Research as a SCIENTIFIC AND INDUSTRIAL RESEARCH ORGANISATION (SIRO).

STUDENT INTERACTION CELL

9. With a view to quickly resolve student queries, a single window to address all types of queries, problems and to help students, a Student Interaction Cell has been established at IETE HQ, New Delhi. This Cell is at the ground floor of the IETE HQ building. Student can approach SIC by:-

- Tel No 011-43538853 Toll free No. 18001025488
- Email: sic@iete.org Fax : 011-24649429

10. If the students' queries are not answered or resolved within a reasonable time, students may contact Secretary General, IETE through personal meeting or phone (011-43538821/22) or email (sec.gen@iete.org). **Students are not to approach any other section of the HQ as their queries/problems shall not be entertained by them.**

IMPORTANT INFORMATION

Students are advised to give their
Mobile No. & Email ID for better and faster communication

DIPIETE EXMINATION

REGULATIONS & SYLLABI

INTRODUCTION

11. IETE conducts DIPIETE Examination in the following two streams.
    (a) Electronics and Telecommunication Engineering (ET)
    (b) Computer Science and Engineering (CS)
    The block and outline syllabi of these streams are given in this booklet and detailed syllabi of (ET) stream is appended at appendix "E".

ELIGIBILITY

12. A candidate desirous of taking up the DIPIETE Examination should first be enrolled as Student (D) member as per Byelaw 17 of the Institution, which is reproduced below: -

- **Bye law 17 – Student (D) Member**

Every candidate for election to the class of Student (D) shall satisfy the Council that he/she is not less than 14 years of age and has minimum pass in Class X conducted by a Recognised Board of Education with General Science (Physics) and Mathematics or its equivalent as prescribed by the Council from time to time; and

(a) is sponsored by a Corporate Member of the Institution, and either

(b) that he/she is or has been a student of Electronics Engineering/ Telecommunication Engineering/ Electrical Engineering/ Physics/ Computer Engineering as applicable, from a University/ College/School approved by the Council

OR

(c) that he/she is or has been an engineering pupil/apprentice/assistant in a recognized firm, society or organization engaged in engineering or allied activities.

ENROLMENT

13 A candidate is required to apply for enrolment on the prescribed form (IETE-4), which is contained in this syllabus. The form also includes the conditions for eligibility.

CORPORATE MEMBER'S RECOMMENDATION AND CERTIFICATES

14. Every application form for student member must be proposed by a corporate member of the IETE and the copies of certificates (age, educational/experience) should be attached duly attested by a corporate member/Gazetted Officer, failing which the application shall not be entertained. For this purpose, the candidate may contact the office of the local centres of IETE. The list of corporate members is available with them. However, in case of any difficulty in getting the enrolment proposed, the form may be submitted directly to the IETE HQ for further action.

ENROLMENT FEE

15. Fees to be paid for enrolment are as given in Form IETE-4 contained in this syllabus. The enrolment fees payable by student members are as under: -

	Member in India (Rs)	**Member Abroad** (US $)
(a) Application Fee	200.00	40.00
(b) Admission Fee	200.00	40.00
(c) Building-cum-Lib. Fund	1300.00	260.00
(d) Composite Subscription (for five years)	2500.00	360.00
(e) Lab Infrastructure Fee	600.00	100.00
(f) Development Fee	500.00	100.00
(g) Establishment Fee	700.00	100.00
	6000.00	1000.00

16. Enrolment fee is to be paid in one instalment at the time of enrolment. The student membership will be valid for 10 consecutive examinations from the date of enrolment. Thereafter, the student members not completing their DIPIETE Examination are to seek re-enrolment for further 10 examinations by remitting applicable amount before or immediately after the expiry of the membership period to continue their membership to enable them to appear in the remaining papers and complete DIPIETE. Any examination chance not availed by a student due to whatsoever reason will be counted within 10 examinations.

MINIMUM PERIOD OF MEMBERSHIP

17. A Student member shall be allowed to appear in the DIP IETE Examination only after he/she has been enrolled as Student (D) member with the Institution. Only those Students (D) members enrolled on or before 28/29th February and 31st August, will be allowed to appear in the next DIPIETE Examination of the Institution, held in June and December respectively. Membership should be alive at the time of submitting the examination application form.

TIME LIMIT TO COMPLETE DIPIETE

18. A student is required to complete DIPIETE Examination within two enrolment periods of 10 consecutive examinations each from the date of initial enrolment. The student will, therefore, be permitted to seek only one renewal of membership. Renewal is to be applied for before or immediately after the expiry of initial enrolment with continuity of enrolment maintained by the student. Any delayed re-enrolment entailing missed chances will be counted towards total number of examinations and no relaxation in this regard will be permissible. If the request for renewal is made after the stipulated period of two enrolments, admission will be treated as a fresh enrolment and no benefit in terms of exemptions in respect of subject(s) passed or exempted during the earlier enrolment will be granted. Students must renew their membership in time. Otherwise they will not be allowed to appear in the DIPIETE examination. No notice will be sent to the students for renewal of membership.

19. **The course curriculum and outline Syllabi for both the streams are given as follows: -**

(a) Course Curriculum (ET) (Appendix-A)
(b) Outline Syllabus (ET) (Appendix-B)
(c) Course Curriculum (CS) (Appendix-C)
(d) Outline Syllabus (CS) (Appendix-D)

The detailed syllabus of the Electronics & Telecommunication stream is given at **Appendix 'E'.**

DIPIETE EXAMINATION

20. DIPIETE examination is divided in two Sections viz. Section A & B with a total 17 theory papers (8 in Section A and 9 in Section B) and 4 labs (2 labs in Section A and 2 labs in Section B). Each Section is divided in two parts viz. Part-I and Part-II. In addition a student has to undergo a project work, seminar and a Course in Communication Skills & Technical Writing. The course on Communication Skills & Technical Writing is mandatory but would not count towards overall CGPA.

21. Distribution of subjects is as under:

(a) Section A
(i) PART-I — Four subjects & 1 Lab
(ii) PART-II — Four subjects & 1 Lab

(b) Section B
(i) PART-I — Five subjects & 1 Lab
(ii) PART-II — Four subjects & 1 Lab
(2 compulsory & 2 from elective subjects)

(C) Project Work
(d) Seminar
(f) Course in Communication Skills & Technical Writing
(Any time during the course)

22. The student should appear in Section A Part-I first and then in Part-II. If a student appears in a part in first attempt, he can appear in the subsequent part in next attempt even though he/she may not have passed in the subjects of the previous part.

Not withstanding above, a student will not be allowed to complete the curriculum in less than three years unless he has been exempted in some subjects.

LAB EXAMINATION

23. Eligibility for Lab, Seminar and Project Examination -

The students are advised to look into the web site www.iete.org for the eligibility criteria for appearing in the Lab, Seminar and Project examination.

COMMUNICATION SKILLS & TECHNICAL WRITING

24. **The course on Communication Skills & Technical Writing** is compulsory for all students. However, the course does not contribute to the overall CGPA. A minimum of 35% marks combining theory and oral test has to be obtained by the student at any time before the completion of his/her DipIETE. The student has to appear for both in one exam. (Either in June or in December)This course consists of theory and oral test. Accordingly, "PASS" or "FAIL" will be reflected in the Grade Sheet.

(a) **Theory :** This consists of written examination for 80 marks.

(b) **Oral Test :** consists of an Oral Test to test the Communication Skills which includes an oral presentation on any subject of the choice of students (e.g. About IETE, General knowledge topics etc). This presentation need not be on technical subjects. This test carries 20 marks.

EXEMPTIONS

25. Exemption may be granted in various papers to the students who have passed similar subjects from elsewhere or other courses. Such exemptions are granted to a candidate passing the subject and successfully completing the course/curriculum from recognized Institutions/Colleges and approved by the IETE Governing Council.

Candidates seeking exemption are required to submit the following documents along with requisite fee:

(a) Application form for exemption.
(b) Certificate of the course/curriculum completed by the student.
(c) Mark sheets duly attested.
(d) Certified copy of syllabi from which the candidate has passed the course.
(e) Fee @ Rs. 700/- per subject for which exemption is sought.

Candidates are advised to apply for exemption, if required, at the earliest opportunity. All cases of exemptions are considered by the Academic Committee of the Institution. For all subjects where exemption are granted will be communicated to the students in the Grade sheet of the first examination after the exemption is sought as it generally takes two month to process an application for exemption. Exemption will generally be granted if the major portion of the syllabi matches with IETE Syllabus. **THE DECISION OF THE ACADEMIC COMMITTEE WILL BE FINAL AND BINDING TO ALL CONCERNED. NO REPRESENTATION IN THIS RESPECT WILL BE ENTERTAINED.**

AWARD OF DIPIETE

26. Every Student member (SD) successfully completing Sections A&B subjects including lab examinations with project work and a course in Communication Skills & Technical Writing of DIPIETE Examination as per regulations prescribed by the Governing Council from time to time shall be eligible to become a member (DipIETE). On payment of requisite fee for membership, he/she will be awarded a certificate of having passed the DIPIETE examination of the Institution and shall then be eligible for transfer to the class of DipIETE. To pass DipIETE Examination, a student is required to score a minimum
grade of 'D' having a grade point of 4 for each subject and having an aggregate of 5 CGPA. However for Project and lab examination, he/she should get a minimum grade of C having a grade point of 5.

CGPA SYSTEM

27. CGPA System which is followed by IETE is given below:

(a) Subject wise grade and grade points are as given below:-

Grade	Grade Point
A+	10
A	9
B+	8
B	7
C+	6
C	5
D	4
F,F+	Fail

(b) CGPA will be calculated as under only for the subjects where a student has passed:-

$$CGPA = \frac{C_1 G_1 + C_2 G_2 \text{ ------ } + C_n G_n}{C_1+C_2+C_3 \text{ ------ } C_n}$$

Where G_1 G_2 ------denote the grade point scored.
C_1 C_2 ------denote the credits of subjects.

All theory Subjects & Lab Carry 4 Credits.
Project work Carries 8 Credits.

(c) The award of division/classification will be as under :-

(i)	CGPA of 9 or more	-	Distinction
(ii)	CGPA 6.5 or more but less than 9	-	First Division
(iii)	CGPA 5 or more but less than 6.5	-	Second Division
(iv)	Less than 5	-	FAIL (No award Will be given)

(d) CGPA is converted into percentage with a multiplier of 9.5.

EXAMINATION APPLICATION

28. Applications to appear in any of the subjects of the DIPIETE Examination must be made on the prescribed OMR Examination Form and accompanied by the requisite examination fee. The prescribed application form is given initially free of cost along with prospectus and later on with a grade sheet where a student has appeared for an examination. OMR Examination application form can also be obtained by the students on payment of Rs. 20/- from any IETE Centre or HQ IETE. No action will be taken on an incomplete application. Students are advised to ensure that they have filled all the columns and have enclosed relevant documents. For exemptions, separate form is to be used. Generally, after the acceptance of examination form of the students, change of examination centre is not encouraged. However in exceptional cases, change of exam Centre will be allowed with an additional charge of Rs. 500/-. For any correction in the examination form after processing an additional amount of Rs 500/- will be charged as reprocessing fee.
Change of streams will be allowed with an additional charge of Rs. 600/-.

EXAMINATION FEE

29. Students are to submit their Examination Application form along with the fee as given below. The fee may get revised from time to time and the students are required to submit their application form along with the latest fee structure in force.

The present fee structure is given below:

		In India (Rs)	**Abroad (US $)**	**Remarks**
(a)	Theory papers/per subject	700.00	80.00	To be deposited along with
(b)	Exemption/per subject	700.00	80.00	exam application form.
(c)	Written Test on Communication Skills & Technical Writing	700.00	80.00	
(d)	Project work	1200.00	220.00	
(e)	Each Lab Examination	500.00	80.00	To be deposited at
(f)	Oral Test on Communication Skills & Technical Writing	500.00	80.00	respective IETE Centre

Note: (a) Fees will be charged per subject irrespective of whether it is for improvement OR re-appearance OR remaining paper OR additional paper OR exemption.

(b) Examination/Exemption fee once paid are neither refundable nor transferable to a subsequent examination.

(c) Enrolment Form, Examination Form and Exemption Form are to be sent separately with requisite fee along with each form.

LAST DATE FOR RECEIPT OF EXAMINATION APPLICATION

30. The last date for receipt of examination form duly filled in at the IETE HQ office for June/Dec examination respectively are as under:-

- Without late fee — 25 Apr/25 Oct
- With late fee (of Rs.1500/-) — 10 May/10 Nov.

Application received after these dates will not be considered.

DATE SHEET

31. The examinations are held twice a year from 15th June and 15th December and are conducted on all days including holidays and Sundays. These dates are firm and changes if any, will be notified to students along with admit cards and through our website **www.iete.org** and at the Local centre.

ADMIT CARD

32. Admit Cards will be sent to all the students to reach them by about 05th of June/December. Admit Cards of eligible students will also be available on our Websites www.iete.org and can be downloaded. Students will be allowed to appear for examination with these downloaded admit card along with their identity card. In the case of non-receipt of Admit-Card by above dates or the admit card not available on the website, the student must approach the concerned Examination Centre or IETE HQ and obtain permission to appear in the examination. No complaint in respect of non-receipt of Admit Card will be entertained once the Examination is over. A student is required to carry his IETE Identity Card and Admit Card issued by IETE for appearing in examination.

EXAMINATION CENTRES

33 Students should appear for all theory papers and practicals in the same Examination Centre. The Examination Centres for exams will be changed by IETE HQ only in special cases after getting the proof of documents. The Exam Centres marked as * are closed. For latest list of examination Centres students are requested to refer to our Website **www.iete.org**

CENTRES	CENTRE CODE	CENTRES	CENTRE CODE
Abu-Dhabi	17	Kochi	32
Ahmedabad	01	Kolkata	04
Allahabad	25	Kozhikode	52
Aligarh*	24	Mumbai	03
Amravati	53	Mysore	33
Aurangabad*	43	Nagpur	37
Bangalore	02	Nashik	39
Bhubaneswar	27	Noida	38
Bhopal	36	Palakkad	41
Chandigarh	05	Patna	46
Chennai	12	Pilani	30
Coimbatore*	47	Pune	14
Dharwad	49	Raipur*	51

Dehradun	26	Rajkot	44
Delhi	06	Ranchi	48
Guwahati	07	Shimla	45
Gwalior*	50	Thiruvananthapuram	16
Hyderabad	08	Vadodara	42
Imphal	31	Varanasi	13
Jabalpur	23	Vijayawada	15
Jaipur	09	Visakhapatnam	34
Jammu*	35		
Kanpur	10		
Kathmandu	19		

USE OF UNFAIR MEANS

34. If a student is found to have resorted to or made attempt to use **Unfair Means**, the Board of Examination may on receipt of report to that effect either from the Exam Superintendent or from invigilator or from the Evaluator/expert, take such action in respect of the student concerned as it thinks fit. The Examination Superintendent of the examination has absolute powers to expel the candidate from the examination hall, if in his opinion the student has adopted unfair means. The disciplinary action against the candidate may consist of punishment(s) extending from cancellation of the paper(s) to debarring from future examinations.

RESULTS

35. Results of the examinations will be announced on or before 10th February and 10h August for December & June examinations respectively and communicated to the candidates through Result Sheets separately. Results will be available on IETE Website **www.iete.org**

RECOUNTING

36. It may be noted that there is **no provision of re-evaluation** of answer books. Therefore request for re-evaluation are out rightly rejected.

Recounting of scores, if requested, can be done by paying Rs.200/- (US$40) per subject. Requests for recounting of scores must be received at IETE HQ within 15 days from the date of announcement of results on **a separate application**.

IMPROVEMENT OF GRADES

37. A student who has passed in a subject may appear for improvement. He may take any number of chances irrespective of Grades previously obtained. If the student secures lower Grade than already secured, the original grade will hold good. Fee for improvement is Rs 500/- (US$80) per paper. However, no improvement is permitted in Lab examination and Project work. Improvement is also allowed after completion of the examinations. After completion, students are required to give an Undertaking that they want/do not want to appear in any subject for improvement. Provisional Certificate/Certificate/final Grade Sheet will be issued only after receipt of undertaking that no improvements are required and the payment of Diploma Membership fee.

AWARDS FOR ACADEMIC EXCELLENCE

38. Six awards have been instituted to give incentive to student members for high level of performance in the DIPIETE Examinations.

LEGAL MATTERS

39. Adjudication in respect of legal cases concerning IETE HQ will be as per Bye-law 95 of the Institution which is reproduced below: -

"All Legal cases concerning IETE HQ shall lie within the jurisdiction of Delhi courts only"

For more information kindly visit http://www.iete.org

AFFILIATION/ACCREDITATION

40. The Institution of Electronics and Telecommunication Engineers (IETE) neither recognises nor accepts affiliations of any private coaching Institute. Students in the past have reported that some private institutions claim that they run classes/coaching on behalf of IETE. It is reiterated that IETE does not authorise any private institution to run classes on behalf of IETE. Therefore IETE is not responsible for false/spurious Private Coaching Institutes.

CORRESPONDENCE WITH IETE HQ

41. Important announcements concerning students and examinations will be available on the website www.iete.org and are also published in IETE Journal of Education which is issued twice a year) to the DIPIETE Student members who have paid their subscriptions to date. For other facilities like participation in technical lectures, symposia etc. nearest IETE Centre/Sub-Centre may be contacted. All correspondence must be addressed to the Secretary General of the Institution (by designation and not by name). Remittances shall be made by way of crossed Bank Draft only. Facilities for making payments on-line will also be available shortly. Bank drafts should be drawn in favour of Secretary General, IETE, New Delhi payable at New Delhi .Cash is accepted by hand at Accounts Section at IETE HQ only .Whenever depositing fee by cash, students must obtain receipt and attach photocopy of the same along with application. MONEY ORDER WILL NOT BE ACCEPTED.

CHANGE OF ADDRESS

42. Students are advised to intimate their change of address to IETE HQ immediately, quoting their Membership Number, complete address with Pin Code.

Students are advised to provide their e-mail ID, telephone no and mobile no with their latest address in all correspondence.

43. MISCELLANEOUS INFORMATION

- Acknowledgement for receipt of enrollment forms and declaration of exam results are given through SMS and Web.
- **All students' related information is displayed on web site www.iete.org. and**
- Students are advised to visit our web site regularly.
- **All payment of fees can also be made on-line. For details refer our website www.iete.org.**

Scheme and Structure for the Programme of DIPIETE in Electronics & Telecommunication

Appendix - "A"

SECTION A

Part - I

Sl No	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DE 101	Engineering Mathematics - I *	4	-
2	DE 102	Fundamentals of Electrical & Electronics *	4	-
3	DE 103	Computer Fundamentals & C Programming *	4	-
4	DE 104	Electronic Engineering Materials	4	-
5	DE 141	C Programming Lab	-	4
		Total Credits	16	4

Part - II

Sl No	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DE 105	Engineering Mathematics – II *	4	-
2	DE 106	Analog Electronics	4	-
3	DE 107	Networks & Transmission Lines	4	-
4	DE 108	Logic Design *	4	-
5	DE 142	Analog Electronics Lab	-	4
		Total Credits	16	4

All the students have to pass a course in "Communication Skills & Technical Writing" which will not be counted for the overall percentage

DE 137	Communication Skills & Technical Writing(Oral)*	20	Marks
DE 138	Communication Skills & Technical Writing(Written)*	80	Marks

SECTION B

Part - I

SN	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DE 109	Electronic Instrumentation & Measurements	4	-
2	DE 110	Power Electronics	4	-
3	DE 111	Microprocessors & Microcontrollers*	4	-
4	DE 112	Analog Communications	4	-
5	DE 113	Telecommunication Switching Systems	4	-
6	DE 143	Logic Design Lab	-	4
		Total Credits	20	4

Part - II

SN	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DE 114	Digital Communications	4	-
	DE 115	Embedded Systems	4	-
2		Elective – I (from Group A)	4	-
3		Elective – II (from Group B)	4	-
4	DE 144	Analog & Digital Communications Lab	-	4
5	DE 135	Project Work ;	-	8
6	DE 136	Seminar	-	4
		Total Credits	16	16

GROUP A
Students can chose any one of the following elective subjects

Students can choose any one of the following as an Elective I subject

SN	Sub Code	Title
1	DE 116	Wireless & Mobile Systems
2	DE 117	Television Engineering and Broadcasting
3	DE 118	Data Communication & Networks **
4	DE 119	Advanced Communication Systems

GROUP B
Students can chose any one of the following elective subjects

Students can choose any one of the following as an Elective II subject

SN	Sub Code	Title
1	DE 120	Control Engineering
2	DE 121	Verilog HDL and VLSI Design
3	DE 122	Object Oriented Programming with C++ **
4	DE 123	Java and Web Programming **

Note: Common to ET / CS Streams

****** Syllabus same as that of core subject for DIPIETE - CS

OUTLINE SYLLABUS
DIPIETE (ELECTRONICS & TELECOMMUNICATION
Appendix 'B'

DE 101 ENGINEERING MATHEMATICS – I

- Differential Calculus
- Integral Calculus
- Linear Algebra
- Differential Equations
- Algebra
- Trigonometry
- Coordinate Geometry

DE 102 FUNDAMENTALS OF ELECTRICAL AND ELECTRONICS

- Electromagnetism
- DC Circuits and AC Circuits
- DC Motor
- Transformer and Induction Motor
- Basic Semiconductor and PN Junctions
- Semiconductor Diodes
- Diode Applications
- Bipolar Junction Transistor
- BJT Biasing
- Amplifiers and Oscillators

DE 103 COMPUTER FUNDAMENTALS & C PROGRAMMING

- Computer Basics
- Data Representation
- Input / Output Units
- Computer Languages
- Operating Systems
- Microcomputers
- Computer Networks
- Constants, Variables and Data Types
- Operators and Expressions
- Managing Input and Output Operations
- Decision Making and Branching
- Decision Making and Looping
- Arrays
- User – Defined Functions
- Pointers
- File Management

DE 104 ELECTRONIC ENGINEERING MATERIALS

- Conducting Materials
- Dielectric Properties of Materials in Static Fields
- Dielectric Materials in Alternating Fields
- Magnetic Materials
- Semi conducting Materials
- Semi conducting Devices
- Materials for Electronic Components
- Fabrication of Semiconductors

DE 104 C PROGRAMMING LAB

DE 105 ENGINEERING MATHEMATICS – II

- Differential Calculus
- Integral Calculus
- Complex Numbers
- Vector Algebra
- Linear Differential Equations of Higher order
- Infinite Series
- Laplace Transforms

DE 106 ANALOG ELECTRONICS

- Integrated Circuit Fabrication
- AC Analysis of BJT Circuits
- Field Effect Transistors
- Power Amplifiers
- Optoelectronic Devices
- Operational Amplifier
- Operational Amplifier Characteristics
- Operational Amplifier Applications

- Comparators and Waveform Generators
- 555 Timer Applications
- Voltage Regulators
- DAC and ADC

DE 107 NETWORKS AND TRANSMISSION LINES

- Laplace Transformation
- Network Theorems
- Network Parameters
- Resonance Circuits and Selectivity
- Transmission Lines
- Open and Short-Circuited Lines
- Line with any Termination
- Ultra High Frequency Lines
- Filters and Attenuators

DE 108 LOGIC DESIGN

- Introductory Concepts
- Number Systems and Codes
- Describing Logic Circuits
- Combinational Logic Circuits
- Flip-Flops and Applications
- Digital Arithmetic Operations and Circuits
- MSI Logic Circuits
- Flip-Flops and Applications
- Counters and Registers
- Synchronous Counter Design
- Memory Devices

DE 142 ANALOG ELECTRONICS LAB

DE109 ELECTRONIC INSTRUMENTATION AND MEASUREMENTS

- Measurement Fundamentals
- Measurement of Resistance, Inductance and capacitance
- Instruments to measure Current and Voltages
- Digital measuring Instruments
- Signal Generators and Oscilloscope
- Signal Analysis Instruments and R.F Power measurement Techniques
- Recorders
- Transducers and Data Acquisition System

DE 110 POWER ELECTRONICS

- Power Electronics
- Power Diodes
- Power Transistors
- Thyristor Devices
- Single-Phase Controlled Rectifiers
- Three-Phase Controlled Rectifiers
- DC Choppers
- Inverters
- AC Voltage Controller
- Static Switches

DE 111 MICORPROCESSORS & MICROCONTROLLERS

- Introduction to Microprocessors
- Assembly Language Programs
- Interrupts in 8085
- Programs Using Interface Modules
- Intel 8259A- Programmable Interrupt Controller
- Intel 8253 – Programmable Interval Timer
- 8051 Microcontroller

DE 112 ANALOG COMMUNICATIONS

- Introduction to Communication Systems
- Noise
- Amplitude Modulation
- Single-Sideband Techniques
- Frequency Modulation
- Radio Receivers

- Radiation and Propagation of Waves
- Waveguides, Resonators and Components
- Antennas
- Pulse Communications
- Broadband Communications Systems

DE 111 TELECOMMUNICATION SWITCHING SYSTEMS

- Switching Systems
- Telecommunications Traffic
- Switching Networks
- Time Division Switching
- Control of Switching Systems
- Signaling
- Packet Switching
- Networks

DE 143 LOGIC DESIGN LAB

DE 114 DIGITAL COMMUNICATIONS

- Introduction
- Fundamental Limits on Performance
- Sampling Process
- Waveform Coding Techniques
- Base-Band Shaping for Data Transmission
- Digital Modulation Techniques
- Detection and Estimation
- Spread Spectrum Modulation
- Applications

DE115 EMBEDDED SYSTEMS

- Introduction to Embedded Systems
- Custom Single Purpose Processors: Hardware
- General Purpose Processors: Software
- Standard Single-Purpose Processors: Peripherals
- Memory
- Interfacing
- Introduction to Real Time Operating Systems
- Case Studies of Programming with RTOS

ELECTIVE - I
ELECTIVE - II

DE 144 ANALOG & DIGITAL COMMUNICATIONS LAB

DE 135 PROJECT WORK:

DE 136 SEMINAR

DE116 WIRELESS & MOBILE SYSTEMS

- Introduction
- Channel Coding and Error Control
- Mobile Radio Propagation
- Cellular Concept
- Multiple Radio Access
- Multiple Division Techniques for traffic Channels
- Traffic Channel Allocation
- Mobile Communication Systems
- Existing Wireless Systems
- Satellite Systems
- Ad Hoc Networks
- Sensor Networks
- Recent Advances
- Wireless LANs, MANs and PANs

DE 117 TELEVISION ENGINEERING & BROADCASTING

- Elements of Television System, Analysis, Synthesis of Television

Pictures and Composite Video Signal
- Signal Transmission and Channel Bandwidth
- Television Picture Tubes and Camera Tubes
- Basic Television Broadcasting and Reception
- Video Section
- Sound Section
- Vertical and Horizontal Deflection Circuits
- Colour Television
- Television Applications

DE 118 DATA COMMUNICATION & NETWORKS
- Data Communications, Data Networking, and the Internet
- Data Transmission
- Transmission Media
- Protocol Architecture, TCP/IP, and Internet-Based Applications
- Signal Encoding Techniques
- Digital Data Communication Techniques
- Data Link Control Protocols
- Multiplexing
- Circuit Switching and Packet Switching
- Routing in Switched Networks
- Congestion Control in Data Networks
- Local Area Network Overview
- High-Speed LANs
- Wireless LANs
- Internetwork Protocols
- Internetwork Operation
- Transport Protocols

DE 119 ADVANCED COMMUN ICATION SYSTEMS
- Optical Fiber Transmission Media
- Cellular Telephone Concepts
- Cellular Telephone Systems
- Introduction to Data Communications and Networking
- Fundamental Concepts of Data Communications
- Data-Link Protocols and Data Communication Networks
- Satellite Communications
- Satellite Multiple Accessing Arrangements

DE 120 CONTROL ENGINEERING
- Modeling of Systems
- Block Diagrams and Signal Flow Graphs
- Feedback Characteristics of Control Systems
- Control Systems and Components
- Time Response Analysis
- Concepts of Stability
- Root Locus Technique
- Frequency Domain Analysis
- Stability in Frequency Domain
- Nyquist Analysis
- Compensation

DE 121 VERILOG HDL AND VLSI DESIGN
- Overview of Digital Design with Verilog HDL
- Gate Level and Dataflow Modeling
- Behavioral Modeling
- Tasks and Functions
- A Review of Microelectronics and an Introduction to MOS Technology
- Basic Electrical Properties of MOSA Circuits
- MOS Circuit Design Processes
- Practical Aspects and Testability

DE 122 OBJECT ORIENTED PROGRAMMING WITH C++

- Object-oriented Programming Concepts
- Language Constructs
- Advanced Constructs
- Classes in C++
- Member Functions
- Operator Overloading
- Constructors and Destructors
- Inheritance
- Multiple Inheritance
- Polymorphism
- Handling Exceptions
- Templates
- C++ I/O

DE 123 JAVA & WEB PROGRAMMING

- Java Evolution
- Overview of Java Language
- Constants, Variables, and Data Types
- Operators and Expressions
- Decision Making and Branching
- Decision Making and Looping
- Classes, Objects and Methods
- Arrays, Strings and Vectors
- Interfaces: Multiple Inheritance
- Packages: Putting Classes Together
- Multithreaded Programming
- Managing Errors and Exceptions
- Managing Input/Output Files in Java
- Web Basics and Overview
- Creating Web Pages: XHTML
- Advanced XHTML
- Design Basics
- Information Architecture and Page Layout
- CSS, Forms and form Processing
- Client –Side Scripting: JavaScript

DE 137 (ORAL) COMMUNICATION SKILLS AND DE 138 (WRITTEN) TECHNICAL WRITING

- Communication: Its Types and Significance
- Grammar
- Syntax
- Reading Skills
- Writing Skills
- Listening Skills
- Speaking Skills
- Technical Report and Scientific Report
- Campus Recruitment, Interview and Group Discussion
- Meeting Negotiations, Phone and Mobile Phone Skills

Scheme and Structure for the Programme of DIPIETE in Computer Science & Engineering

Appendix - "C"

SECTION A

Part - I

Sl No	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DC 101	Engineering Mathematics – I *	4	-
2	DC 102	Fundamentals of Electrical & Electronics *	4	-
3	DC 103	Computer Fundamentals & C Programming *	4	-
4	DC 104	Data Structures	4	-
5	DC 141	C & Data Structures Lab	-	4
		Total Credits	16	4

Part - II

Sl No	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DC 105	Engineering Mathematics – II *	4	-
2	DC 106	Object Oriented Programming with C++	4	-
3	DC 107	Computer Organization	4	-
4	DC 108	Logic Design *	4	-
5	DC 142	OOPS Lab	-	4
		Total Credits	16	4

All the students have to pass a course in "Communication Skills & Technical Writing" which will not be counted for the overall percentage

DC 137	Communication Skills & Technical Writing(Oral)*	30	Marks
DC 138	Communication Skills & Technical Writing(Written)*	70	Marks

SECTION B

Part - I

Sl No	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DC 109	Analysis & Design of Information Systems	4	-
2	DC 110	Operating Systems & Systems Software	4	-
3	DC 111	Microprocessors & Microcontrollers *	4	-
4	DC 112	Database Management Systems	4	-
5	DC 113	Java & Web Programming	4	-
6	DC 143	Java & Web Programming Lab	-	4
		Total Credits	20	4

Part - II

Sl No	Sub Code	Title	Examination Credits	
			Theory	Practicals
1	DC 114	Data Communication & Networks	4	-
2	DC 115	Software Engineering	4	-
3		Elective – I(from Group A)	4	-
4		Elective – II(from Group B)	4	-
5	DC 144	DBMS Lab	-	4
6	DC 135	Project Work: Phase - II	-	8
7	DC 136	Seminar	-	4
		Total Credits	16	16

GROUP A **Students can chose any one of the following elective subjects**		
Students can choose any one of the following as an Elective I subject		
Sl No	**Sub Code**	**Title**
1	DC 116	Computer Graphics & Visualization
2	DC 117	C# & .Net
3	DC 118	Internet Applications
4	DC 119	Cloud Computing

GROUP B **Students can chose any one of the following elective subjects**		
Students can choose any one of the following as an Elective II subject		
Sl No	**Sub Code**	**Title**
1	DC 120	Software Testing
2	DC 121	Embedded Systems **
3	DC 122	Mobile Applications Development
4	DC 123	Network Management

Note:

* Common to ET / CS Streams

** Syllabus same as that of core subject for DIPIETE - ET

OUTLINE SYLLABUS Appendix 'D'
DIPIETE (COMUTER SCIENCE & ENGINEERING)

DC 101 ENGINEERING MATHEMATICS – I
- Differential Calculus
- Integral Calculus
- Linear Algebra
- Differential Equations
- Algebra
- Trigonometry
- Coordinate Geometry

DC 102 FUNDAMENTALS OF ELECTRICAL AND ELECTRONICS
- Electromagnetism
- DC Circuits and AC Circuits
- DC Motor
- Transformer and Induction Motor
- Basic Semiconductor and PN Junctions
- Semiconductor Diodes
- Diode Applications
- Bipolar Junction Transistor
- BJT Biasing
- Amplifiers and Oscillators

DC 103 COMPUTER FUNDAMENTALS & C PROGRAMMING
- Computer Basics
- Data Representation
- Input / Output Units
- Computer Languages
- Operating Systems
- Microcomputers
- Computer Networks
- Constants, Variables and Data Types
- Operators and Expressions
- Managing Input and Output Operations
- Decision Making and Branching
- Decision Making and Looping
- Arrays
- User – Defined Functions
- Pointers
- File Management

DC 104 DATA STRUCTURES
- Advanced C Concepts
- Recursion
- Structures, Union and Files
- Arrays, Searching and Sorting
- Stacks and Queues
- Liked Lists
- Trees
- Graphs

DC 141 C& DATA STRUCTURES LAB

DC 105 ENGINEERING MATHEMATICS – II
- Differential Calculus
- Integral Calculus
- Complex Numbers
- Vector Algebra
- Linear Differential Equations of Higher order
- Infinite Series
- Laplace Transforms

DC 106 OBJECT ORIENTED PROGRAMMING WITH C++
- Object-Oriented Programming Concepts
- Language Constructs
- Advanced Constructs
- Classes in C++
- Member Functions
- Operator Overloading
- Constructors and Destructors
- Inheritance
- Multiple Inheritance
- Polymorphism

- Handling Exceptions
- Templates
- C++ I/O

DC 107 COMPUTER ORGANIZATION

- Basic Structure of Computers
- Machine Instructions and Programs
- Input/Output Organization
- Memory System
- Arithmetic
- Basic Processing Unit

DC 108 LOGIC DESIGN

- Introductory Concepts
- Number Systems and Codes
- Describing Logic Circuits
- Combinational Logic Circuits
- Flip-Flops and Applications
- Digital Arithmetic Operations and Circuits
- MSI Logic Circuits
- Flip-Flops and Applications
- Counters and Registers
- Synchronous Counter Design
- Memory Devices

DC 142 OOPS LAB

DC 109 ANALYSIS & DESIGN OF INFORMATION SYSTEMS

- The Context of Systems Analysis & Design Methods
- Information System Building Blocks
- Information Systems Development
- Systems Analysis
- Modeling System Requirements with Use Cases
- Data Modeling and Analysis
- Object-Oriented Analysis and Modeling Using the UML
- Systems Design
- User-Interface Design
- Object-Oriented Design and Modeling Using the UML
- Systems Construction and Implementation
- Systems Operations and Support

DC 110 OPERATING SYSTEMS & SYSTEMS SOFTWARE

- Evolution of OS Functions
- Processes
- Scheduling
- Deadlocks
- Process Synchronization
- File Systems
- Memory Management
- Language Processors
- Data Structures for Language Processing
- Scanning and Parsing
- Macros and Macro Processors
- Linkers
- Assemblers
- Compilers and Interpreters

DC 111 MICORPROCESSORS & MICROCONTROLLERS

- Introduction to Microprocessors
- Assembly Language Programs
- Interrupts in 8085
- Programs Using Interface Modules
- Intel 8259A- Programmable Interrupt Controller
- Intel 8253 – Programmable Interval Timer
- 8051 Microcontroller

DC 112 DATABASE MANAGEMENT SYSTEMS

- Databases and Database Users
- Database System - Concepts and Architecture
- Data Modeling Using the Entity-Relationship Model

- The Enhanced Entity-Relationship (EER) Model
- The Relational Data Model and Relational Database Constraints
- The Relational Algebra and Relational Calculus
- Relational Database Design By ER - to - Relational Mapping
- SQL-99: Schema Definition, Constraints, Queries and Views
- Relational Database Design
- Transaction Processing Concepts

DC 113 JAVA & WEB PROGRAMMING

- Java Evolution
- Overview of Java Language
- Constants, Variables, and Data Types
- Operators and Expressions
- Decision Making and Branching
- Decision Making and Looping
- Classes, Objects and Methods
- Arrays, Strings and Vectors
- Interfaces: Multiple Inheritance
- Packages: Putting Classes Together
- Multithreaded Programming
- Managing Errors and Exceptions
- Managing Input/Output Files in Java
- Web Basics and Overview
- Creating Web Pages: XHTML
- Advanced XHTML
- Design Basics
- Information Architecture and Page Layout
- CSS, Forms and Form Processing
- Client-Side Scripting: Javascript

DC 143 JAVA & WEB PROGRAMMING LAB

DC 114 DATA COMMUNICATION & NETWORKS

- Data Communications, Data Networking, and the Internet
- Data Transmission
- Transmission Media
- Protocol Architecture, TCP/IP, and Internet-Based Applications
- Signal Encoding Techniques
- Digital Data Communication Techniques
- Data Link Control Protocols
- Multiplexing
- Circuit Switching and Packet Switching
- Routing in Switched Networks
- Congestion Control in Data Networks
- Local Area Network Overview
- High-Speed LANs
- Wireless LANs
- Internetwork Protocols
- Internetwork Operation
- Transport Protocols

DC 115 SOFTWARE ENGINEERING

- Socio-Technical Systems
- Software Processes
- Project Management
- Software Requirements
- Requirements Engineering Processes
- System Models
- Rapid Software Development
- Formal Specification
- Architectural Design
- Distributed Systems Architectures
- Objected-Oriented Design
- Software Reuse
- Component-Based Software Engineering

- User Interface Design
- Verification and Validation
- Software Testing
- Quality Management
- Configuration Management

ELECTIVE - I

ELECTIVE - II

DC 144 DBMS LAB

DC 135 PROJECT WORK:

DC 136 SEMINAR

DC 116 COMPUTER GRAPHICS & VISUALIZATION

- A Survey of Computer Graphics
- Overview of Graphics Systems
- Graphics Output Primitives
- Attributes of Graphics Primitives
- Geometric Transformations
- Viewing
- Visible-Surface Detection Methods
- Illumination Models and Surface-Rendering Methods
- Interactive Input Methods and Graphical User Interfaces
- Computer Animation

DC 117 C# & .NET

- Introducing C# and the .Net Platform
- The Philosophy of .Net
- Building C# Applications
- Core C# Programming Constructs
- Defining Encapsulated Class Types
- Understanding Inheritance and Polymorphism
- Understanding Structured Exception Handling
- Understanding Object Lifetime
- Working with Interfaces

DC 118 INTERNET APPLICATIONS

- Hypertext Markup Language
- More HTML
- Cascading Stylesheets
- An Introduction to Javascript
- Objects in Javascript
- Dynamic HTML with Javascript
- Programming in PERL 5
- CGI Scripting
- Building Web Applications with PERL
- An Introduction to PHP
- Building Web Applications with PHP
- XML: Defining Data for Web Applications

DC 119 CLOUD COMPUTING

- Cloud Computing Basics
- Your Organization and Cloud Computing
- The Business Case for Going to the Cloud
- Cloud Computing Technology
- Cloud Computing at Work
- Migrating to the Cloud
- Best Practices and the Future of Cloud Computing

DC 120 SOFTWARE TESTING

- Introduction
- Testing and Levels
- Transaction Flow Testing
- Data Flow Testing
- Domain Testing
- Paths, Path Products
- Logic Based Testing
- Testing of Object-Oriented Systems

DC 121 EMBEDDED SYSTEMS

- Introduction to Embedded Systems
- Custom Single Purpose Processors: Hardware
- General Purpose Processors: Software
- Standard Single-Purpose Processors: Peripherals
- Memory
- Interfacing
- Introduction to Real Time Operating Systems
- Case Studies of Programming with RTOS

DC 122 MOBILE APPLICATION DEVELOPMENT

- Introduction to Android
- Activities and Intents
- Introducing Android User Inferface
- Designing User Interface Using Views
- Displaying Pictures and Menus with Views
- Data Persistence
- Content Providers
- Messaging and Networking
- Location Based Services
- Android Services
- Hardware Sensors

DC 123 NETWORK MANAGEMENT

- Data Communications and Network Management Overview
- SNMP and Network Management Basic Foundations: Standards, Models and Language
- SNMPv1 Network Management: Organization and Information Models
- SNMPv1 Network Management: Communication and Functional Models
- SNMP Management: RMON
- Network Management Tools, System and Engineering
- Network Management Applications
- Broadband Network Management

DC 137 (ORAL) DC 138 (WRITTEN) COMMUNICATION SKILLS AND TECHNICAL WRITING

- Communication: Its Types and Significance
- Grammar
- Syntax
- Reading Skills
- Writing Skills
- Listening Skills
- Speaking Skills
- Technical Report and Scientific Report
- Campus Recruitment, Interview and Group Discussion
- Meeting Negotiations, Phone and Mobile Phone Skills

Appendix 'E'

DETAILED SYLLABUS

Introduction

Most of the Student Members of the IETE are working engineers/ technicians/science graduates and under graduates. Thus, due to occupational reasons and other factors these students are deprived of a formal education and therefore have to learn the subjects through self-study only.

Review of Syllabus

2. IETE periodically reviews the syllabi of DIPIETE and the aim of these reviews is not only to renovate and modernize the contents but also to make them contemporary. The syllabi for both Electronics & Telecommunications (ET) and Computer Science & Engineering (CS) streams have been reviewed recently.

3. Keeping the above aspects in view and based on feed backs/suggestions received from the students, this syllabus has been formulated to meet the following criteria:-

- The Syllabus should cater to the technological advancements.
- The textbooks should be available and affordable to the students.
- In the absence of a formal coaching to the students, there should be a reasonable correlation between the topics in a subject and the textbooks.

Salient Features

4. Some salient features of the syllabus are:-

- Each subject has a code preceding it (Viz DE101 and DC101 are codes for Mathematics I in ET & CS streams respectively).
- In order to guide the student and to enable him/her to prepare well for an examination, each subject is divided into 8 units and each unit has the course contents to be covered in 7 or 8 hours.
- The textbooks have been numbered in Roman Numerical (viz I, II, III)
- The chapters and sections are mentioned inside the bracket e.g. I (2.1) would indicates chapter 2 and section 1 of textbook I.

Scheme of the Examination

5. For all theory subjects the Question Paper contains

- 10 objective questions for 20 marks covering the complete syllabus
- 8 questions are from each unit and each question carries 16 marks.

6. Regular feed back from the students, academicians, corporate members and professionals is requested to keep this syllabus updated, so that our students keep abreast of latest technological changes. Though every effort has been made to identify standard and best textbooks for each subject, we welcome suggestions on availability of better and cheaper textbooks.

DE 101 ENGINEERING MATHEMATICS – I

UNIT I

DIFFERENTIAL CALCULUS 08 hrs

Limits; Left hand and Right hand Limits; Continuity of functions; Evaluation of simple limits; Differentiability of a Function; Geometrical Meaning of derivative; Standard Results; Logarithmic Differentiation; Differentiation of Implicit function; Parametric Equations; Successive differentiation; Calculation of n^{th} derivative of standard functions; Leibnitz theorem for the n^{th} derivative of the product of two functions; Applications of differentiation –Increasing and Decreasing functions; Maxima and Minima.

I (1.6, 1.8, 1.9, 1.10, 2.3, 2.25, 2.26, 2.27, 2.30, 2.31, 2.37, 4.1, 4.2)

UNIT II

INTEGRAL CALCULUS 07 hrs

Introduction; Definitions; Hyperbolic functions; Standard results – Indefinite Integrals; Integration by the Method of Substitution; Standard formula; Integration by parts; Integration by Partial Fraction Method; Integration of Irrational Functions; Integration of Trignometric functions; Definite Integrals - Introduction; Theorems on Definite Integrals.

I (21.1, 21.2, 21.4, 21.5, 22.1, 22.2, 23.1, 24.1, to 24.7, 25. 1 to 25.6, 26.1 to 26.3, 28.1, 28.2)

UNIT III

MATRICES 08 hrs

Definition of Matrices**;** various types of Matrices, Addition of Matrices; Properties of Matrix addition; subtraction of Matrices, sclar Multiple of a Matrix; Multiplication of Matrices; Adjoint of square Matrix; Inverse of a Matrix; Elementary Transformations; To compute the inverse of a Matrix using Gauss Jordan Method; Normal form, Rank of a Matrix, Types of Linear equations; Consistency of system of Linear equations; Linear Dependence and Independence of Vectors

I (19.1 TO 19.23)

UNIT IV

DIFFERENTIAL EQUATIONS 07 hrs

Definition of Differential Equation; Order and Degree of a Differential Equation; Formation of Differential Equation; Solution of First order and First Degree Differential Equation; Solution by the Method of Variable Separable; Homogeneous Differential Equation; Reducible to Homogeneous Differential Equation; Linear Differential Equation of 1^{st} Order; Equations Reducible to Linear Form; Linear Differential Equation in x; Exact Differential Equation; Equations Reducible to Exact Equations, Application of Differential equation

I (36.1 TO 36.13)

UNIT V

ALGEBRA 07 hrs

Principles of Mathematical Induction; Permutation and Combinations; Binomial Theorem (for positive integral index); Arithmetic Progressions; Geometric Progressions.

II (Unit II Chapters 14, 18, 19, 20, 21, 22)

UNIT VI

TRIGONOMETRY 07 hrs

Introduction; Measurement of Angles; Trigonometric ratios; Trigonometric functions; Trigonometric functions of Sum and Difference of two angles; Transformation Formulae;

Trigonometric functions of Multiple and sub-multiple angles; Conditional Identities and Equations; Graphs of Trignometric Functions; Trignometric Equations; Relations between the Sides and the Trignometric Ratios of the Angles of a Triangle.

II (Unit I Chapters 4, 5, 6, 7, 8, 9, 10, 11, 12)

UNIT VII

CO-ORDINATE GEOMETRY 08 hrs

Introduction, Distance formula, Area of a Triangle, Condition for collinearity of three points, Section formulae, Centroid of a triangle, Incentre of a triangle, Straight lines, Parallel and Perpenidcular lines, Angle between two lines, Condition for lines to be Parallel and Perpenidcular, Intersection of lines.

II (Chapter 24 &25; 24.1 to 24.7, 25.1 to 25.9, 25.17 to 25.20)

UNIT VIII

CO-ORDINATE GEOMETRY (CONTINUED) 08 hrs

Conic sections: Introduction, Circles, Concetric Circles, Parabola, Equation of a Parabola in the general form, Ellipse, Equation of an Ellipse in the general and standard form, Hyperbola, Equation of Hyperbola in its general and standard form.

II (Chapter 26;26.1 to 26.5,26.7,26.9,26.10 to 26.13,26.15 to 26.17,26.22 to 26.24)

Text Books:

I. Engineering Mathematics, H. K. Dass, S, Chand and Company Ltd, New Delhi, 2010.
II. A Text book of Comprehensive Mathematics Class XI, Parmanand Gupta, Laxmi Publications (P) Ltd, New Delhi.

Reference Book:

1. Higher Engineering Mathematics, B. S. Grewal, 41st Edition, Khanna Publishers, Delhi.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 102 FUNDAMENTALS OF ELECTRICAL AND ELECTRONICS

PART A
FUNDAMETALS OF ELECTRICAL ENGINEERING

UNIT I

ELECTROMAGNETISM 07 hrs

Coulomb's Law of Electrostatics; Capacitor Charging and Discharging; Magnetic Field; Force on Current Carrying Conductor in a Magnetic Field; MMF; Magnetic Field Strength; Reluctance; Laws of Magnetic Circuits; Calculation of Ampere-Turns; Magnetization Curve; Comparison of Electric and Magnetic Circuits; Faraday's Law; Statically Induced EMF.

I (2.3, 2.8, 2.9, 3.2, 3.9, 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 5.2, 5.6)

UNIT II

DC CIRCUITS AND AC CIRCUITS 08 hrs

Ohm's Law; Kirchoff's Laws; Superposition Theorem; Thevenin's Theorem; Norton's Theorem; Production of AC Voltage; RMS Value; Phasor Representation; Steady State Analysis of R, L, C, RL, RC, RLC circuits; Power in AC Circuits; Generation of Three

Phase EMF; Phase Sequence; Star and Delta Connection; Relationship Between Line and Phase Quantities; Power in Three Phase System.

I (1.5, 1.6, 1.8, 1.9, 1.10, 6.2, 6.4, 6.9, 6.12, 6.13, 6.14, 7.2, 7.3, 7.4, 7.5, 9.2, 9.3, 9.5, 9.6, 9.7, 9.8, 9.9)

UNIT III

DC MOTOR **08 hrs**

Principle of Operation; Construction; EMF Equation; Types of DC Motor (Shunt and Series Motor); Torque Equation; Motor Characteristic Curves; Necessity of Starter; Speed Control of Shunt Motor-Armature Control and Field Control.

I (17.3, 17.4, 17.6, 17.9, 19.2, 19.4, 19.5, 19.6)

UNIT IV

TRANSFORMER AND INDUCTION MOTOR **07 hrs**

Transformer: Principle of Operation; EMF Equation of Transformer; Three Phase Induction Motor: Construction; Rotating Magnetic Field; Principle of Operation; Slip.

I (14.3, 14.6, 23.2, 23.3, 23.4, 23.8)

PART B: FUNDAMETALS OF ELECTRONICS

UNIT V

BASIC SEMICONDUCTOR AND PN JUNCTION THEORY **04 hrs**

Introduction; Atomic Theory; Conduction in Solids; Conductors, Semiconductors and Insulators; n-type and p-type Semiconductors; The p-n Junction; Biased Junctions.

II (1.1, 1.2, 1.3, 1.4, 1.5, 1.6)

SEMICONDUCTOR DIODES **04 hrs**

Introduction; p-n Junction Diode; Characteristics and Parameters; Diode Approximations; DC Load Line Analysis; Temperature Effects; AC Equivalent Circuits; Zener Diodes.

II (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.9)

UNIT VI

DIODE APPLICATIONS **07 hrs**

Introduction; Half Wave Rectification; Full Wave Rectification; Half Wave Rectifier DC Power Supply; Full Wave Rectifier DC Power Supply; Power Supply Performance; Zener Diode Voltage Regulators; Series Clipping Circuits; Shunt Clipping Circuits; Clamping Circuits; DC Voltage Multiplexers.

II (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10)

UNIT VII

BIPOLAR JUNCTION TRANSISTORS **04 hrs**

Transistor Operation; Transistor Voltages and Currents; Amplification; Common Base Characteristics; Common Emitter and Common Collector Characteristics.

II (4.1, 4.2, 4.3, 4.4, 4.5, 4.6)

BJT BIASING **04 hrs**

DC Load Line and Bias Point Base Bias; Collector to Base Bias; Voltage Divider Bias; Comparison of Basic Bias Circuits; Bias Circuit Design; Thermal Stability of Bias Circuits (Qualitative Discussions Only).

II (5.1, 5.2, 5.3, 5.4, 5.5, 5.7, 5.9)

UNIT VIII

AMPLIFIERS AND OSCILLATORS **07 hrs**

Decibels and Half Power Points; Single Stage CE Amplifier; Capacitor Coupled Two Stage CE Amplifier (Qualitative Discussions Only); Series Voltage Negative Feedback (Qualitative Discussions); Additional Effects of Negative Feedback (Qualitative); The BJT Phase Shift Oscillators; BJT Colpitts and Hartley Oscillator (Qualitative).

II (8.2, 12.1, 12.3, 13.1, 13.7, 16.1, 16.2, 16.3)

Text Books:

I. V.N. Mittle and Arvind Mittal, 'Basic Electrical Engineering', Tata McGraw-Hill Publishing Company Limited, 2nd edition, 2006.
II. Electronic Devices and Circuits, Fourth Edition, David A Bell, PHI (2006).

Reference Books:

1. D.P. Kothari and I.J. Nagrath, 'Basic Electrical Engineering', Tata McGraw-Hill Publishing Company Limited, 2nd edition, 2002.
2. I.J. Nagrath and D.P. Kothari, 'Electric Machines', Tata McGraw-Hill Publishing Company Limited.
3. Electronic Devices and Circuits, I.J. Nagrath, PHI, 2007.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks, selecting atleast **TWO** questions from each part.

DE 103 COMPUTER FUNDAMENTALS & C PROGRAMMING

PART A: COMPUTER FUNDAMENTALS

UNIT I

1.1 COMPUTER BASICS **07 hrs**

Algorithms, A Simple Model of a Computer, Characteristics of Computers, Problem Solving Using Computers

1.2 DATA REPRESENTATION

Representation of Characters in Computers, Representation of Integers, Representation of Fractions, Hexadecimal Representation of Numbers, Decimal to Binary Conversion, Error Detecting Codes

I (1, 2)

UNIT II

1.3 INPUT / OUTPUT UNITS **08 hrs**

Description of Computer Input Units, Other Input Methods, Computer Output Units

1.4 COMPUTER LANGUAGES

Why Programming Language? Assembly Language, Higher Level Programming Languages, Compiling High Level Language Program, Some High Level Languages

1.5 OPERATING SYSTEMS

Why Do We Need an Operating System? Personal Computer Operating System, The Unix Operating System

1.6 I (3, 9, 10.1, 10.5, 10.6)

UNIT III

1.7 MICROCOMPUTERS **07 hrs**

An Ideal Microcomputer, An Actual Microcomputer, Memory Systems for Microcomputers, A Minimum Microcomputer Configuration, Evolution of Microcomputers

1.8 COMPUTER NETWORKS

Need for Computer Communication Networks, Internet and the World Wide Web, Local Area Networks

I (11.1to 11.4, 14.1, 14.2, 14.4)

2 **PART B: C PROGRAMMING**

UNIT IV

2.1 CONSTANTS, VARIABLES AND DATA TYPES **08 hrs**

Introduction, Characters set, C tokens, Keywords and Identifiers, Constants, Variables, Data types, Declaration of variables

2.2 OPERATORS AND EXPRESSIONS

Arithmetic operators, Relational operators, Logical operators, Assignment operators, Increment and Decrement operators, Conditional operator, Bit wise operators, Special operators, Arithmetic expressions, Evaluation of expressions, Precedence of Arithmetic operators, Type conversions in expressions, Operator precedence and associativity

2.3 MANAGING INPUT AND OUTPUT OPERATIONS

Introduction, Reading a character, Writing a character, Formatted Input, Formatted Output

II (2.1 to 2.8, 3.2 to 3.12, 3.14, 3.15, 4)

UNIT V

2.4 DECISION MAKING AND BRANCHING **07 hrs**

Introduction, Decision making with *if* statement, Simple *if* statement, The *if… else* statement, Nesting of *if…. else* statements, The *else….if* ladder, The *switch* statement, The?: operator, The *Goto* statement

2.5 DECISION MAKING AND LOOPING

Introduction, The *while* statement, The *do* statement, The *for* statement, Jumps in Loops.

II (5, 6)

UNIT VI

2.6 ARRAYS **08 hrs**

Introduction, One – dimensional Arrays, Declaration of one – dimensional Arrays, Initialization of one – dimensional Arrays, Two – dimensional Arrays, Initializing two – dimensional Arrays.

2.7 CHARACTER ARRAYS AND STRINGS

Introduction, Declaring and Initializing String Variables, Reading Strings from Terminal, Writing Strings to Screen, Putting Strings together, Comparison of Two Strings, String-handling Functions

II (7.1 to 7.6, 8.1 to 8.4, 8.6, 8.7, 8.8)

UNIT VII

2.8 USER – DEFINED FUNCTIONS **07 hrs**

Introduction, Need for User – defined Functions, A multi – function program, Elements of User defined Functions, Definition of Functions, Return Values and their Types, Function Calls, Function Declaration, Category of Functions, No Arguments and no Return Values, Arguments but no Return Values, Arguments with Return Values, No Argument but Returns a Value, Functions that Return Multiple Values.

II (9.1 to 9.14)

UNIT VIII

2.9 POINTERS **08 hrs**

2.10 Introduction, Understanding Pointers, Accessing the Address of a Variable, Declaring Pointer Variables, Initialization of Pointer Variables, Accessing a Variable through its Pointer, Chain of Pointers, Pointer Expressions, Pointer Increments and Scale Factor, Pointer and Arrays, Pointers and Character Strings, Array of Pointers.

2.11 FILE MANAGEMENT

2.12 Introduction, Defining and Opening a File, Closing a File, Input/Output Operations on Files

2.13 II (11.1 to 11.12, 12.1 to 12.4)

Text Books:

I. Fundamentals of Computers, V. Rajaraman, Fifth Edition, PHI, 2011
II. Programming in ANSI C, E. Balagurusamy, 5th Edition, Tata McGraw Hill, 2011

Reference Book:

1. Computer Science – A Structured Programming Approach Using C, Behrouz A. Forouzan, Richard F. Gilberg, 3rd Edition, CENGAGE Learning, 2007

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks, selecting **TWO** questions from Part A and **THREE** from Part B.

DE 104 ELECTRONIC ENGINEERING MATERIALS

UNIT I

CONDUCTING MATERIALS **08 hrs**

Introduction; Factors Affecting the Resistivity of Electrical Materials; The Electron Gas Model of Metal; Motion of Electron in Electric Field; Equation of Motion of an Electron; Current Carried by Electrons; Mobility; Energy Levels of a Molecule; Fermi Energy; Fermi-Dirac Distribution; Emission of Electrons from Metals-Thermionic, Photoelectric, Field and Secondary Emissions; Contact Potential, Effect of Temperature on Electrical Conductivity of Metals; Superconductivity; Electrical Conducting Materials; Thermo-Electric Effects; Operation of Thermocouple.

I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.14, 3.15)

UNIT II

DIELECTRIC PROPERTIES OF MATERIALS IN STATIC FIELDS **07 hrs**

Introduction, Effect of a Dielectric on the Behavior of a Capacitor; Polarization; Dielectric Constant of Monatomic Gases; Polarization Mechanisms-Electronic, Ionic and Dipolar polarization; Internal Fields in Solids and Liquids-Lorentz field; Clausius-Mosotti Relation; Polarisability Catastrophe.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III

DIELECTRIC MATERIALS IN ALTERNATING FIELDS **08 hrs**

Introduction; Frequency Dependence of Electronic Polarizability; Frequency Dependence of Permittivity; Frequency Dependence of Ionic Polarizability; Dielectric Losses and Loss Tangent; Dipolar Relaxation; Frequency and Temperature Dependence of Dielectric

Constant of Polar Dieletrics; Dielectric Properties of Polymeric Systems; Ionic Conductivity in Insulators; Insulating Materials; Breakdown in Gaseous, Liquid and Solid Dielectric Materials; Important Requirements of Good Insulating Materials; Ferroelectricity; Piezoelectricity.

I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11, 5.12, 5.13)

UNIT IV

MAGNETIC MATERIALS **08 hrs**

Introduction; Classification of Magnetic Materials; Origin of Permanent Magnetic Dipoles-Diamagnetism and Paramagnetism; Ferromagnetism-Origin and Ferromagnetic Domains; Magnetization and Hysteresis Loop; Magnetostriction; Factors Affecting Permeability and Hysteresis Loss; Common Magnetic Materials-Iron and Silicon Iron Alloys; Nickel-Iron Alloys and Permanent Magnet Materials and Design of Permanent Magnets; Anti-Ferromagnetism and Ferrimagnetism; Magnetic Resonance.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11, 6.12, 6.13, 6.14, 6.15, 6.16)

UNIT V

SEMICONDUCTING MATERIALS **08 hrs**

Introduction; Energy Bands in Solids-Energy Bands in Conductors, Semiconductors and Insulators; Types of Semiconductors-Energy Bands for n-type and p-type Semiconductor; Intrinsic Semiconductors; Impurity Type Semiconductor and Interaction of Semiconductor with Time-Dependent Fields; Diffusion and Einstein Relation; Hall-effect-Hall Voltage; Hall Coefficient; Thermal Conductivity of Semiconductors; Electrical Conductivity of Doped Materials; Materials for Fabrication of Semiconductor Devices; Passive Materials Integral to Device-Metals; Capacitance Materials; Junction Coatings.

Device Potting; Packaging; Process Aids; Susceptor Materials; Reactor Envelopes; Plastics and Pump fluids; Solvents and Etchants.

I (7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.7, 7.8, 7.9, 7.10, 7.11, 7.12, 7.13)

UNIT VI

SEMICONDUCTING DEVICES **07 hrs**

Metal-Semiconductor Contacts; P-N Junction; Barrier Capacitance; Breakdown Phenomena in Barrier Layer-Zener and Avalanche Breakdown; Junction Diodes-Zener, Varactor and Tunnel Diodes; Junction Transistor; Thermistors and Varistors; Semiconductor Materials-Silicon and Germanium; Silicon-Germanium Mixed Crystals; Silicon Carbide and Intermetallic Compounds; Silicon Controlled Rectifier-Two Transistor and Electromechanical Analogue.

I (8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8, 8.9)

UNIT VII

MATERIALS FOR ELECTRONIC COMPONENTS **07 hrs**

Resistors-Carbon Composition; Insulated-Moulded; Film type; Cracked Carbon and Alloy Resistors; Metal-Oxide Film; Wire-Wound; High-Value; Non-Linear Resistors; Voltage-Sensitive resistors; Variable Resistors; Capacitors-Paper, Mica, Ceramic, Glass-Dielectric, Vitreous-Enamel, Plastic, Electrolytic, Air-Dielectric and Variable Capacitors; Inductors-Air-Cored Coils; Laminated-Core; Powdered Iron Core and Ferrite-Core Inductors; Relays-Reed; Moving Coil; Induction; Thermal Type Relays; Electronic Valves;Gas-filled and transistor relays; Function of Relays.

I (12.1, 12.2, 12.3, 12.4, 12.5)

UNIT VIII

FABRICATION OF SEMICONDUCTORS **07 hrs**

Fabrication Technology-Czochralski Method, Grown Junction and Alloyed Junction Processes; Diffused Junction Technique; Epitaxial Diffused Junction Diode; Fabrication of Junction Transistor; Field-Effect Devices; Distinguishing Properties from Bipolar Devices; JFET; Drain and Transfer Characteristics of JFET; Operation as far as pinch-off; operation of JFET with high drain voltages.

I (14.1, 14.2, 14.3, 14.4, 14.5, 14.6, 14.7, 14.8, 14.9)

Text Book:

I. Introduction to Electrical Engineering Materials by C.S. Indulkar and S. Thiruvengadam, 6th Edition, Reprint 2012 Edition, S. Chand and Company, New Delhi.

Reference Books:

1. Materials Science and Engineering, V. Raghavan, Prentice-Hall of India, New Delhi, 5th Edition, Thirty ninth Printing, June 2010
2. Electronic Engineering Materials and Devices, John Allison, Tata McGraw Hill, New Delhi (1998)
3. Elements of Materials Science and Engineering, Lawrence H. Van Vlack, Pearson Education (6th Edition)

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 141 C PROGRAMMING LAB

List of Experiments

1. Write a C program to find and output the roots of a given quadratic equation with non-zero coefficients.
2. Write a C program to simulate a simple calculator that performs addition, subtraction, multiplication, and division of integers. Error should be reported, if any attempt is made to divide by zero.
3. Write a C program to generate and print the first*N* Fibonacci numbers.
4. Write a C program to find the GCD and LCM of two given integers, and output the results.
5. Write a C program to reverse a given four-digit number and check whether the number is a palindrome or not.
6. Write a C program to find whether a given integer is prime or not.
7. Write a C program to input *N* real numbers in ascending order into a single dimension array, conduct binary search for a given key number, and report success or failure.
8. Write a C program to sort a given set of *N* student names in alphabetical order.
9. Write a C program to evaluate the polynomial $f(x) = a_4x^4 + a_3x^3 + a_2x^2 + a_1x + a_0$for a given value of x, and the coefficients using Horner's method.
10. Write a C program to read two matrices A (M x N) and B (P x Q), and compute the product of A.B after checking compatibility for multiplication.
11. Write C user defined functions

a. to input *N* integer numbers into a single dimension array
b. to conduct linear search

Using these functions write a C program to accept *N* integer numbers and a given key integer and conduct linear search.

12. Write C user defined functions
    a. to input N integer numbers into single dimension array
    b. to sort the integer numbers in ascending order using bubble sort technique
    c. to print the single dimension array elements

    Using these functions, write a C program to input N integers numbers into a single-dimension array, sort them in ascending order, and print both the given array and the sorted array.
13. Write C user defined functions
    a. To input N real numbers into single dimension array
    b. to compute their mean
    c. to compute their variance
    d. to compute their standard deviation

    Using these functions write a C program to input N real numbers into a single dimension array, compute their mean, variance, and standard deviation.
14. Write a C program to read a matrix A(M x N) and compute the following using user defined functions:
    a. Sum of the elements of the specified row
    b. Sum of the elements of the specified column
    c. Sum of all the elements of the matrix
15. Write a C program using pointers to read in an array of integers and print its elements in reverse order.

Note:

- All the C programs to be executed using Turbo C or similar environment.

DE 105 ENGINEERING MATHEMATICS – II

UNIT I

DIFFERENTIAL CALCULUS **07 hrs**

Mean value theorems and expansion of functions,Taylor's and Maclaurin's expansion of functions,Indeterminate forms.

I (2.2 to 2.6)

UNIT II

INTEGRAL CALCULUS **07 hrs**

Reduction formulae for $\int_0^{\pi/2} \sin^n(x)dx$, $\int_0^{\pi/2} \cos^n(x)dx$, $\int_0^{\pi/2} \sin^m(x)\cos^n(x)dx$,

Problems, Application of Integration –Volume and Surface area of the solid of revolution.

I (7.1, 7.2, 8.1 to 8.6)

UNIT III

COMPLEX NUMBERS **08 hrs**

Introduction; Geometric representation of complex number (Argand diagram); Modulus and Argument of Complex number; conjugate of a Complex number; Addition; Subtraction of Complex numbers; Multiplication and Division of Complex numbers; Exponential and Circular functions of Complex variables; DeMovire's Theorem; Phasor; R and A.C Circuits; L and A.C Circuits; C and A.C. Circuits; R-C and A-C circuits Impedance; R-L in Parallel Circuit.

II (Chapter 28: 28.1 to 28.16)

UNIT IV

VECTOR ALGEBRA **07 hrs**

Introduction to Vectors; Addition and Subtraction of Vectors; Properties of Addition of vectors; Rectangular resolution of a Vector; Position Vector of a point; Ratio formula; Product of two Vectors; Scalar or Dot product of two Vectors; Geometrical interpretation; Work done as a scalar product; Vector product or cross product; Geometrical interpretation; Moment of a force; Angular velocity; Scalar triple product; Geometrical interpretation; Vector triple product.

II (20.1to20.9,20.8,21.1,21.2,21.3,21.5,21.6,22.1,22.8,22.9,22.10,23.1,23.2,23.3)

UNIT V

LINEAR DIFFERENTIAL EQUATION OF HIGHER ORDER **07 hrs**

Introduction; General form; complete solution as C.F+P.I; Method of finding complimentary function, Inverse operator $\frac{1}{f(D)}$, Method of finding particular integral for the functions e^{ax} ; $\sin(ax+b)$; $\cos(ax+b)$; x^m,

Application of Linear Differential equation Electrical Circuits

II (45.1 to 45.8, 46.1)

UNIT VI

INFINITE SERIES **08 hrs**

Introduction to Sequences,Series,Tests for Convergence,Comparsion test,D'Alembert's Ratio test,Rabee's test,Cachy's root test,Alternating series,Absolute convergence

I (1.1, 1.8 to1.12, 1.19, 1.20)

UNIT VII

LAPLACE TRANSFORMS **08 hrs**

Definition, Examples of Laplace Transforms, Properties of Laplace Transforms, Limiting theorems.

I (20.1, 20.2, 20.3)

UNIT VIII

INVERSE LAPLACE TRANSFORMS **08 hrs**

Definition; Standard results; Properties of Inverse Laplace transforms, Problems, Convolution Theorem (only statements and problems); Application of Laplace transform to solve Linear differential problems.

I (21.1,21.2,21.3,21.6,22.1,22.2)

Text Books:

I. Engineering Mathematics – Babu Ram, Pearson Education Limited, 2012.

II. Applied Mathematics for Polytechnic, H.K.Dass, 10th Edition, 2012, CBS Publishers & Distributors, New Delhi

Reference Book:

1. A Text book of engineering Mathematics – N.P. Bali and Manish Goyal , 8th Edition 2011, Laxmi Publication(P) Ltd.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 106 ANALOG ELECTRONICS

UNIT I

INTEGRATED CIRCUIT FABRICATION 07 hrs

Introduction; Classification; IC Chip Size and Circuit Complexity; Fundamentals of Monolithic IC Technology; Basic Planar Processes; Fabrication of a Typical Circuit; Active and Passive Components of IC's; Fabrication of FET; Thin and Thick Film Technology; Technology Trends.

II (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 1.10)

UNIT II

AC ANALYSIS OF BJT CIRCUITS 07 hrs

Coupling and Bypassing Capacitors; AC Load Lines; Transistor Models and Parameters; Common Emitter Circuit Analysis; CE Circuit with un-bypassed Emitter Resistor; Common Collector Circuit Analysis; Common Base Circuit Analysis; Comparison of CE; CC and CB Circuits.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8)

UNIT III

FIELD EFFECT TRANSISTORS 07 hrs

Junction Field Effect Transistor; JFET Characteristics; JFET Data Sheet and Parameters; FET Amplification and Switching; MOSFETS.

I (9.1, 9.2, 9.3, 9.4, 9.5)

UNIT IV

POWER AMPLIFIERS 04 hrs

Transformer Coupled Class-A Amplifier; Transformer Coupled Class-B Amplifier and Class AB Amplifiers; Transformer Coupled Amplifier Design; Capacitor-coupled and Direct-coupled Output Stages.

I (19.1, 19.2, 19.3, 19.4)

OPTOELECTRONIC DEVICES 04 hrs

Light Units; Light Emitting Diodes; Seven Segment Displays; Photo-Diodes and Solar Cells; Photo Transistors; Opto-couplers.

I (21.1, 21.2, 21.3, 21.5, 21.6, 21.7)

UNIT V

OPERATIONAL AMPLIFIER 03 hrs

Basic Information of Operational Amplifier; The Ideal Operational Amplifier; Operational Amplifier Internal Circuit; Differential Amplifier; Transfer Characteristics.

II (2.1, 2.2, 2.3, 2.4, 2.4.1, 2.4.2)

OPERATIONAL AMPLIFIER CHARACTERISTICS **04 hrs**

Introduction; DC Characteristics; AC Characteristics; Frequency Response; Stability of Op-Amp (Qualitative Analysis); Slew Rate; Analysis of Data Sheet of an Op-Amp.

II (3.1, 3.2, 3.3, 3.3.1, 3.3.2, 3.3.4, 3.4)

UNIT VI

OPERATIONAL AMPLIFIER APPLICATIONS **08 hrs**

Introduction; Basic Op-Amp Applications; Instrumentation Amplifier; AC Amplifier; V to I and I to V Converters; Op-Amp Circuits using Diodes; Sample and Hold Circuits; Differentiator; Integrator.

II (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.10, 4.11)

UNIT VII

COMPARATORS AND WAVEFORM GENERATORS **04 hrs**

Introduction; Comparator; Regenerative Comparator (Schmitt Trigger); Square Wave Generator (Astable Multivibrator); Monostable Multivibrator; Triangular Wave Generator; Sine Wave Generators.

II (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7)

555 TIMER **04 hrs**

Introduction; Description of Functional Diagram; Monostable Operation; Astable Operation.

II (8.1, 8.2, 8.3, 8.4)

UNIT VIII

VOLTAGE REGULATORS; DAC AND ADC **08 hrs**

Introduction; Series Op-Amp regulator; IC Voltage Regulator; 723 General Purpose Regulator.

Basic DAC Techniques; Weighted Resistor DAC; R-2R Ladder DAC.

A-D Converters; The Parallel Comparator(FLASH) ADC; The Counter-type ADC; Successive approximation-type ADC; Dual-Slope ADC;

II (6.1, 6.2, 6.3, 6.4, 10.1, 10.2, 10.2.1, 10.2.2, 10.3, 10.3.1, 10.3.2, 10.3.4, 10.3.6)

Text Books:

I. Electronic Devices and Circuits, Fifth Edition, David A Bell, OXFORD UNIVERSITY PRESS, Thirteenth impression 2010.
II. Linear Integrated Circuits, 4th Reprint 2011 Edition, D. Roy Choudhury, Shail B. Jain, New Age International Publishers.

Reference Books:

1. Electronic Devices and Circuits, I.J. Nagrath, PHI, 2007.
2. Operational Amplifiers and Linear IC's, Second Edition, David A Bell, PHI.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks

DE 107 NETWORKS AND TRANSMISSION LINES

UNIT I

LAPLACE TRANSFORMATION 08 hrs

Advantages of Laplace Transformation; Laplace Transformation; Basic Theorems; Laplace Transform of Important Functions; Inver Laplace Transformation; Transform Impedance of Network Elements; Common Singularity Functions; Laplace Transform of Singularity Functions; Shifting Theorems; Laplace Transform of Shifted Functions; Square Pulse and Triangular Waveforms; Initial and Final Value Theorems; Impulse Response; Convolution Theorem;

I (18.1 to 18.14)

UNIT II

NETWORK THEOREMS 07 hrs

Superposition Theorem; Thevenin's and Norton's Theorem; Reciprocity Theorem; Compensation Theorem; Maximum Power Transfer Theorem; Bartlett's Bisection Theorem; π-T Equivalent Theorem; Foster's Reactance Theorem; Millman Theorem; Principle of Duality. Tellengen's Theorem;

I (13.1 to 13.15)

UNIT III

NETWORK PARAMETERS 08 hrs

Characterization in terms of z, y, h and ABCD parameters; Equivalent Circuits; Relationships between two-port Parameters; Use of Matrices for Networks; Interconnection of Two-port Networks; Application to the Analysis of Typical Two-port Networks; Condition of Reciprocity and Symmetry in Two-port parameter representation.

I (14.1 to 14.6, 14.8)

UNIT IV

RESONANCE CIRCUITS 08 hrs

Power Factor; Q of Inductor and Capacitor; Series Resonance; Characteristics Curves of Series R-L-C Circuit; Voltage across Capacitor and Inductor at Series Resonance Circuit; Parallel Resonance; Characteristic Curves of a Parallel R-L-C Resonance Circuit; Current Through Inductor and Capacitor of Parallel RLC Resonance Circuit; Bandwidth and Selectivity;

I (19.1 to 19.9)

UNIT V

TRANSMISSION LINES 07 hrs

Fundamental Quantities; Primary Constants of Transmission Lines; Loop Inductance; Shunt Capacitance; Loop Resistance; Skin Effect; Transmission Line Equations; Determination of Constants A and B; Infinite Line; Infinite Line is equivalent to a finite line terminated in Z_o; Secondary Constants of Transmission Line; Characteristic Impedance; Propagation Constant; Attenuation and Phase Constants; Wavelength; Velocity of Propagation; and Group Velocity; Computation of Primary Constants; Computation of Secondary Constants; Computation of Sending End and Receiving End parameters.

I (1.1 to 1.18)

UNIT VI

OPEN AND SHORT CIRCUITED LINES 04 hrs

Reflected and Incident Waves; Standing Waves in Open and Short Circuited Lines; Input Impedance of Open and Short Circuited Lines; Secondary Line Constants in terms of Z_{oc} and Z_{sc}; Transmission Lines as Circuit Elements.

2.13.1.1.1.1 **LINE WITH ANY TERMINATION** **04 hrs**

General Equation; Input Impedance; Input Impedance of the line in terms of Exponential Form; Input Impedance of a loss lessline; Reflection; Reflection Coefficient; Reflection Loss and Reflection Factor; Standing Wave Ratio; Input Impedance in terms of Reflection Coefficients; Reflection Loss due to Mismatching; Power Delivered to the Load; Efficiency of Transmission;

I (2.1 to 2.5, 3.1 to 3.12)

UNIT VII

2.13.1.1.1.1.1 **ULTRA HIGH FREQUENCY LINES** **07 hrs**

Characteristic Impedance; Standing Wave Ratio; Relation Between VSWR and Reflection Coefficient; Location of Voltage Maxima and Minima; Impedance Circle Diagram; Smith Chart; Properties of Smith Chart; Application of Smith Chart; Impedance Matching Devices; The Quarterwave Transformer; Balun; Stub Matching; Single Stub Matching; Determination of I_s and I_t in terms of Reflection Coefficient K; Determination of I_s and I_t by Smith Chart; Double Stub Matching; Determination of I_{s1} and I_{s2} by Smith Chart.

I (6.1 to 6.17)

UNIT VIII

FILTERS AND ATTENUATORS **04 hrs**

The Decibel and Neper; Ladder Network as Filters; Characteristics of Filter;Uses of Filters; Type of Filters Characteristics of The Filter; Constant k Filters; Phase-shift and attenuation of Constant k Filters; m-derived Filters; Composite Filter; Termination Half-sections, Band-Pass Filters; Band-Stop Filter.

ATTENUATORS **04 hrs**

Symmetrical Attenuators; Symmetrical T-Attenuators; Symmetrical-π Attenuators, Symmetrical Bridged T Attenuators; Symmetrical lattice Attenuators; Asymmetrical Attenuators; Asymmetrical- T Attenuator; Asymmetrical-L Attenuator; Asymmetrical-π Attenuator; Minimum Loss Attenuator; Attenuators for variable Load; Balanced and Unbalanced Attenuators.

I (15.17 to 15.29, 17.1 to 17.12)

Text Book:

I. Transmission Lines and Networks; Umesh Sinha, 8th Edition; Reprint 2004, Satya Prakashan, Incorporating Tech India Publications, New Delhi

Reference Book:

1. Networks, Lines and Fields; John D Ryder**;** Prentice Hall of India.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 108 LOGIC DESIGN

UNIT I

INTRODUCTORY CONCEPTS 03 hrs

Numerical Representations; Digital and Analog Systems; Digital Number Systems; Representing Binary Quantities; Digital Circuits / Logic Circuits; Parallel and Serial Transmission; Memory, Digital Computers.

I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8)

NUMBER SYSTEMS AND CODES 04 hrs

Introduction; Binary to Decimal Conversions; Decimal to Binary Conversions; Octal Number System; Hexadecimal Number System; BCD Code,Gray Code; Putting it all together; The Byte; Nibble and Word; Alphanumeric Codes;

I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9)

UNIT II

DESCRIBING LOGIC CIRCUITS 04 hrs

Introduction; Boolean Constants and Variables; Truth Tables: OR, AND, NOT Operations; Describing Logic Circuits Algebraically; Evaluating Logic Circuit Outputs; Implementing Circuits from Boolean Expressions; NOR and NAND Gates; Boolean Theorems; De-Morgan's Theorems; Universality of NAND and NOR Gates.

I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, 3.12)

COMBINATIONAL LOGIC CIRCUITS 04 hrs

Sum of Product Form; Simplifying Logic Circuits; Algebraic Simplification; Designing Combinational Logic Circuits; Karnaugh Map Method (3 and 4 Variables); Exclusive OR and Exclusive NOR Circuits; Parity Generator and Checker;.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III

DIGITAL ARITHMETIC OPERATIONS AND CIRCUITS 08 hrs

Introduction; Binary Addition; Representing Signed Numbers; Addition in 2's Complement System; Subtraction in 2's Complement System; Multiplication and Division of Binary Numbers; BCD Addition; Hexadecimal Arithmetic; Arithmetic Circuits; Parallel Binary Adder; Design of a Full Adder; Complete Parallel Adder with Registers; Carry Propagation; Integrated Circuit Parallel Adder; 2's Complement System; BCD Adder; ALU Integrated Circuits.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11, 6.12, 6.13, 6.14, 6.15, 6.16, 6.17)

UNIT IV

MSI LOGIC CIRCUITS 07 hrs

Introduction; Decoders; BCD to 7-Segment Decoder / Drivers; Liquid Crystal Displays; Encoders; Multiplexers; Multiplexer Applications; De-Multiplexers; Magnitude Comparator; Code Converters.

I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7, 9.8, 9.9)

UNIT V

FLIP-FLOPS AND APPLICATIONS 08 hrs

Introduction; NAND Gate Latch; NOR Gate Latch; Clocked Signals and Clocked Flip-Flops; Clocked SR Flip-Flop; Clocked JK Flip-Flop; Clocked D Flip-Flop; D Latch; Asynchronous Inputs; IEEE / ANSI Symbols; Flip-Flop Timing Considerations; Potential Timing Problem in Flip-Flop Circuits; Master Slave Flip-Flops; Flip-Flop Applications; Flip-

Flop Synchronization; Data Storage and Transfer; Serial Data Transfer: Shift Registers; Frequency Division and Counting; Schmitt Trigger Devices; Analyzing Sequential Circuits.

I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11, 5.12, 5.13, 5.14, 5.16, 5.17, 5.18, 5.19,5.20, 5.21)

UNIT VI

COUNTERS AND REGISTERS **08 hrs**

Introduction; Asynchronous (Ripple) Counters; Counters with Mod Numbers < 2^N; IC Asynchronous Counters; Asynchronous Down Counters; Propagation Delay in Ripple Counters; Synchronous (Parallel) Counters; Synchronous Down and Up / Down Counters; Presettable Counter; Decoding a Counter; Decoding Glitches; Cascading BCD Counters,Analyzing synchronous counter.

I (7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.7, 7.8, 7.11, 7.12, 7.13)

UNIT VII

SYNCHRONOUS COUNTER DESIGN **07 hrs**

Synchronous Counter Design;State machines, Integrated Circuit Registers; Parallel In / Parallel Out Register; Serial In / Serial Out Register; Parallel In / Serial Out Register; Serial In / Parallel Out Register; Shift Register Counters.

I (7.14, 7.15, 7.16, 7.17, 7.18, 7.19, 7.21)

UNIT VIII

MEMORY DEVICES **07 hrs**

Memory Terminology; General Memory Operation; CPU Memory Connections; Read Only Memories; ROM Architecture; ROM Timing; Types of ROM's; Flash Memory; ROM Applications; Semiconductor RAM; RAM Architecture; SRAM; DRAM; DRAM Structure and Operation.

I (11.1, 11.2, 11.3, 11.4, 11.5, 11.6, 11.7, 11.8, 11.9, 11.10, 11.11, 11.12, 11.13, 11.14)

Text Book:

I. Digital Systems – Principles and Applications, Ronald J Tocci, Neal S. Wildmer, Gregory L. Moss, Tenth Edition, Pearson Education, Copyright 2009.

Reference Books:

1. Digital Fundamentals, Thomas L. Floyd and R. P. Jain, Eighth Edition, Pearson Education Publisher, 2005
2. Digital Electronics and Microprocessors – Problems and Solutions, R. P. Jain, 2007, Tata-McGraw Hill

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 142 ANALOG ELECTRONICS LAB

List of Experiments:

1. **Characteristics of Semiconductor Diode and Zener Diode:** Determination of forward and reverse resistance from VI characteristics.
2. **Static Characteristics of BJT under CE Mode:** Determination of h-parameters h_{ie} from input characteristics and h_{fe} and h_{oe} from output characteristics.
3. **Static Characteristics of JFET:** Determination of r_d from drain characteristics and g_m from mutual characteristics and hence obtain amplification factor.
4. **Characteristics of UJT:** Determination of intrinsic standoff ratio η from emitter characteristics.
5. **Resonant Circuits:** Characteristics of Series and Parallel Circuits, Determination of quality factor and bandwidth.
6. **Bridge Rectifier with and without C-Filter:** Display of output waveforms and Determination of ripple factor, efficiency and regulation for different values of load current.
7. **Diode Clipping Circuits:** Design and display the transfer characteristics of single ended and double ended shunt type clipping circuits.
8. **RC Coupled Single-stage BJT Amplifier:** Determination of lower and upper cutoff frequencies, mid band voltage gain, gain bandwidth product from the frequency response.
9. **Emitter Follower:** Determination of mid band voltage gain, input and output impedances at mid frequency range.
10. **Class-B Complementary Symmetry Power Amplifier:** Display of input and output waveforms and Determination of the conversion efficiency and optimum load.
11. **BJT Colpitt's Oscillator:** Design and test the performance for a given frequency.
12. **Study of Basic Op-Amp Circuits:** Design and verification of inverting amplifier, non-inverting amplifier, voltage follower, integrator, differentiator and inverting adder circuits.
13. **Schmitt Trigger:** Design, testing, and display of waveforms.
14. **Op-Amp Wein Bridge Oscillator:** Design and test the performance for the given frequency.
15. **Study of 555 Timer:** Design and test the performance of Astable multivibrator circuit for the given frequency.
16. **Study of Voltage Regulator:** Design and study of IC7805 voltage regulator, calculation of line and load regulation.

Note: Experiments are to be conducted in the hardware lab as well as using the software PSPICE 9.1 version and above downloadable at http://pspice.en.softonic.com

DE 109 ELECTRONIC INSTRUMENTATION AND MEASUREMENTS

UNIT I

MEASUREMENT FUNDAMENTALS **08 hrs**

Significance of Measurements; Methods of Measurements; Instruments and Measurement Systems; Mechanical, Electrical and Electronic Instruments; Classification of Instruments.

Characteristics of Instruments; Static Calibration; Static Characteristics; Errors in Measurement; True value; Static Error; Static Correction; Scale Range and Scale Span; Error Calibration; Accuracy and Precision; Indication of Precision; Linearity; Hysteresis; Threshold; Dead Time and Dead Zone; Resolution.

Types of Errors; Gross Errors; Systematic Errors; Random Errors.

Units, Systems, Dimensions and Standards – Units; Absolute Units; Fundamental and Derived Units; Dimensions; Dimensions of Mechanical Quantities; Dimensional Equations; Relationship between Electrostatic and Electromagnetic System of Units; SI Units; Base Units of SI; Standards and their Classification.

I (1.2 to 1.6, 2.2 to 2.9, 2.13,2.14, 2.18 to 2.23, 3.5 to 3.8, 5.2 to 5.6, 5.9, 5.10, 5.13, 5.14, 5.20)

UNIT II

MEASUREMENT OF RESISTANCE, INDUCTANCE AND CAPACITANCE **08 hrs**

Measurement Resistance-Classification of resistances; Measurement of Medium Resistances-Wheatstone Bridge; Sensitivity of Wheatstone Bridge; Measurement of Low Resistance-Kelvin Double Bridge; Measurement of High resistance-Difficulties; Earth Resistance Measurement using Megger.

Measurement of Inductance- sources& detectors ,General Form of an AC Bridge; Measurement of Self Inductance Using Anderson Bridge; Measurement of Capacitance Using Schering Bridge; High Voltage Schering Bridge.

I (14.1, 14.2, 14.2.3, 14.2.4, 14.3.2, 14.4, 14.4.1, 14.5, 16.2, 16.4, 16.5.4, 16.6.2, 16.6.3)

UNIT III

INSTRUMENTS TO MEASURE CURRENT AND VOLTAGES **07 hrs**

Measurement of current by DC Ammeter; Multi range Ammeters; RF Ammeters; Limitations of Thermocouple; Effect of Frequency on Calibration; Measurement of Very Large Currents by Thermocouple.

Measurement of voltage by DC Voltmeter; DC Voltmeter; Multi range voltmeter; Solid State Voltmeter; AC Voltmeter using Rectifier, Half-Wave and Full Wave Rectifiers;

Average and Peak Responding Voltmeter; True RMS Voltmeter; Multimeter; Digital Multimeters.

II (3.2, 3.6, 3.7, 3.8, 3.9, 4.2, 4.3, 4.4, 4.9, 4.12 to 4.14, 4.16 to 4.18, 4.25, 6.2)

UNIT IV

DIGITAL MEASURING INSTRUMENTS **07 hrs**

Digital Voltmeter-Dual Slope Integrating Type DVM; Integrated Type DVM; Continuous Balanced DVM, successive approximation DVM; 3½ Digit; Digital Meter for Measuring Frequency and Time; Counter-Universal, Decade, Electronic; Digital Tachometer; Digital pH Meter; Digital Phase Meter; Digital Capacitance Meter; Q-Meter

II (5.3, 5.4, 5.5, 5.7, 5.8, 6.3 to 6.10, 6.12, 6.13, 10.7)

UNIT V

SIGNAL GENERATORS AND OSCILLOSCOPE **08 hrs**

Introduction; Basic Standard Signal Generator; Standard Signal Generator; Modern Laboratory Signal Generator; AF Sine and Square Wave Generator; Function Generator; Square and Pulse Generator; Standard Specifications of a Signal Generator.

Oscilloscope-Basic Principle; CRT Features; Block diagram; Simple CRO; Vertical Amplifier; Deflecting system; Triggered CRO; Trigger Pulse Circuits; Storage and Sampling Oscilloscope, lissajous methods.

II (8.1, 8.4 to 8.9, 8.20, 7.2 to 7.9, 7.17, 7.18, 7.20)

UNIT VI

SIGNAL ANALYSIS INSTRUMENTS AND R.F POWER MEASUREMENT TECHNIQUES **08 hrs**

Wave Analyzers-Basic; Frequency Selective; Heterodyne Wave Analyzers; Harmonic Distortion and Spectrum Analyzer.

Bolometer Method of Power Measurement; Bolometer Element and Mount; Measurement of Power by Means of Bolometer Bridge; Measurement of Large Amount of RF Power.

II (9.3, 9.4, 9.5, 9.6, 20.3 to 20.7, 20.10)

UNIT VII

RECORDERS **07 hrs**

Objective and Requirement of Recording Data; Recorder Selection for Particular Applications; Recorders-Strip Chart; Galvanometer Type; Null Type; Circular Chart Type; X-Y; Magnetic; Potentiometric Recorders; Recorder Specifications.

II (12.2 to 12.7, 12.10 to 12.13)

UNIT VIII

TRANSDUCERS AND DATA ACQUISITION SYSTEM **07 hrs**

Electrical transducer; Selecting a Transducer; Resistive transducer; Resistive Position Transducer; Strain Gauges; Resistance Thermometer; Thermistor; Inductive Transducer, Differential Output Transducers; LVDT; Pressure Inductive; Capacitive Transducers; Load Cell;

Data Acquisition System-Objective of Data Acquisition System; Signal Conditioning of the Inputs; Single and Multi Channel Data Acquisition System.

II (13.2 to 13.14, 13.20, 17.1 to 17.5)

Text Books:

I. A Course in Electrical and Electronic Measurements and Instrumentation, A.K Sawhney, Dhanpat Rai & Co,New Delhi, 19th Revised Edition 2011(Reprint 2012).
II. Electronic Instrumentation, H.S Kalsi, Tata McGraw Hill, 3rd Edition(fourth reprint 2012).

Reference Books:

1. Electronic Instrumentation and Measurement Techniques, W.D. Cooper and A. D. Helfrick, Prentice Hall of India Pvt. Ltd., New Delhi
2. Electronic Instrumentation and Measurements, David A. Bell, Second Edition, PHI, 2007.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 110 POWER ELECTRONICS

UNIT I

POWER ELECTRONICS 03 hrs

Introduction; What is Power Electronics?; Why Power Electronics?; Power Semiconductor Switches; Power Losses in Real Switches; Types of Power Electronics Circuits; Applications of Power Electronics.

I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7)

POWER DIODES 04 hrs

Introduction; The PN Junction Diode; The Voltage-Current Characteristic of a Diode; The Ideal Diode; The Schottky Diode; Diode Circuit Analysis; Diode Losses; Principal Ratings for Diodes; Diode Protection; Testing a Diode; Series and Parallel Operation of Diodes.

I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11)

UNIT II

POWER TRANSISTORS 07 hrs

Introduction; Power Bipolar Junction Transistors (BJTs); Power Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs); Insulated-Gate Bipolar Transistors (IGBTs); Unijunction Transistors (UJT).

I (3.1, 3.2, 3.3, 3.4, 3.5)

UNIT III

THYRISTOR DEVICES 08 hrs

Introduction; The Silicon Controlled Rectifier (SCR); SCR Characteristic Curves; Testing SCRs; SCR Ratings; Junction Temperature Rating; Increasing SCR Ratings; Series and Parallel SCR Connections; Power Loss; SCR Protection; Gate Circuit Protection; SCR Gate-Triggering Circuits; Triggering SCRs in Series and in Parallel; SCR Turn-Off (Commutation) Circuits; Other types of Thyristors.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10, 4.11, 4.12, 4.13, 4.14, 4.15)

UNIT IV

SINGLE-PHASE CONTROLLED RECTIFIERS 07 hrs

Introduction; Half-Wave Controlled Rectifiers; Full-Wave Controlled Center-Tap Rectifiers; Full-Wave Controlled Bridge Rectifiers; Half-Controlled or Semi-Controlled Bridge Rectifiers; Dual Converters.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6)

UNIT V

THREE-PHASE CONTROLLED RECTIFIERS 08 hrs

Introduction; Half-Wave (Three-Pulse) Controlled Rectifiers; Full-Wave (Six-Pulse) Controlled Bridge Rectifier; Full-Wave Half-Controlled Bridge Rectifiers with FWD.

I (8.1, 8.2, 8.3, 8.4)

UNIT VI

DC CHOPPERS 07 hrs

Introduction; The Principles of Basic DC Choppers; Step-Down (Buck) Choppers; Step-Up (Boost) Choppers; Buck-Boost Choppers.

I (9.1, 9.2, 9.3, 9.4, 9.5)

UNIT VII

INVERTERS **08 hrs**

Introduction; The Basic Inverter; Voltage Source Inverters (VSI); Pulse-Width Modulation (PWM); Pulse-Width Modulated (PWM) Inverters; Other Basic Types of Single-Phase Inverters; The Ideal Current Source Inverter (CSI).

I (10.1, 10.2, 10.3, 10.5, 10.6, 10.7, 10.9)

UNIT VIII

AC VOLTAGE CONTROLLER **05 hrs**

Introduction; AC Power Control; Integral Cycle Control; AC Phase Control; Cycloconverters.

I (11.1, 11.2, 11.3, 11.4, 11.7)

STATIC SWITCHES

03 hrs

Introduction; Comparison of Static and Mechanical Switches; Static AC Switches; Three-Phase Static Switches; Hybrid Switches; The Solid State Relay (SSR); Static Tap-Changing Control; The Static VAR Controller (SVC).

(12.1, 12.2, 12.3, 12.4, 12.5, 12.6, 12.7, 12.8)

Text Book:

I. Power Electronics for Technology, Ashfaq Ahmed, Purdue University - Calumet, Pearson Education.

Reference Books:

1. Power Electronics – Circuits, Devices and Applications, Third Edition, Muhammad H. Rashid, Pearson Education / Prentice Hall of India Pvt. Ltd.
2. Power Electronics, Third Edition, P.S.Bimbra, Khanna Publishers, New Delhi.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 111 MICROPROCESSORS & MICROCONTROLLERS

UNIT I

INTRODUCTION TO MICROPROCESSORS **08 hrs**

Evolution of Microprocessors, Fundamentals of a Computer, Number Representation – Unsigned binary integers, Signed binary integers; Fundamentals of Microprocessor – description of 8085 pins, Programmer's view of 8085, Registers A, B, C, D, E, H and L
First Assembly Language Program; Instruction set of 8085 – Data transfer group, Arithmetic group, Logical group, NOP and Stack group of instructions

I (1, 2, 3.1, 3.2, 4.2, 4.3, 4.4, 4.5, 5, 6, 7, 8, 9)

UNIT - II

INTRODUCTION TO MICROPROCESSORS (CONTD) **08 hrs**

Instruction set of 8085 continued – Branch group, Chip select logic, Addressing of I/O ports, Architecture of 8085 – Details of 8085 architecture

I (10, 11, 12, 13.1)

UNIT III

ASSEMBLY LANGUAGE PROGRAMS **07 hrs**

Exchange 10 bytes, Add 2 multibyte numbers, Add 2 multibyte BCD numbers, Block movement without overlap, Monitor routines, Multiply two numbers
Linear search, Find the smallest number
I (14.1 to 14.4, 14.6.1, 16.1, 16.2)

UNIT IV

INTERRUPTS IN 8085 **07 hrs**

Data transfer schemes, 8085 interrupts, EI and DI instructions, INTR and INTA* pins, RST 5.5, RST 6.5, RST 7.5, and TRAP pins, SIM and RIM instructions
I (18.1 to 18.7, 18.9)

UNIT V

PROGRAMS USING INTERFACE MODULES **07 hrs**

8255 Programmable peripheral interface chip, Description of 8255, Operational modes, Control port of 8255, Logic controller interface, Evaluation of Boolean expression, Decimal counter, Intel 8279 Keyboard and display controller.
I (20.1, 20.2, 20.3, 21.1 – 21.1.1, 21.1.3, 22.6.1)

UNIT VI

2.14.1 INTEL 8259A- PROGRAMMABLE INTERRUPT CONTROLLER **08 hrs**

Need for interrupt controller, Overview of 8259, Pins of 8259, Registers of 8259
Intel 8257 – Programmable DMA controller, Concept of DMA, Need for DMA, Description of 8257, Pins of 8257.
I (23.1 to 23.4, 24.1, 24.2, 24.3, 24.5)

UNIT VII

INTEL 8253 – PROGRAMMABLE INTERVAL TIMER **08 hrs**

Need for programmable interval timer, Description of 8253, Programming the 8253, Mode 0 operation, Intel 8251A – Universal synchronous asynchronous receiver transmitter, Need for USART, Asynchronous transmission, Asynchronous reception, Synchronous transmission, Synchronous reception, Pin description of 8251.
I (25.1 to 25.4, 26.1 to 26.6)

UNIT VIII

8051 MICROCONTROLLER **07 hrs**

Main features, Functional blocks, Program memory structure, Data memory structure, Programmer's view, Addressing modes, Instruction set, Programming examples.
I (29)

Text Book:

I. The 8085 Microprocessor; Architecture, Programming and Interfacing, K. Udaya Kumar and B. S. Umashankar, Pearson Education, 2008

Reference Books:

1. Microprocessor Architecture, Programming and Applications with the 8085, Fifth Edition, R. S. Gaonkar, Penram International Publishing (India), 2011
2. The 8051 Microcontroller and Embedded Systems, Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay, Second Edition, Pearson Education, 2009

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 112 ANALOG COMMUNICATIONS

UNIT I

INTRODUCTION TO COMMUNICATION SYSTEMS 03 hrs

Communications; Communication Systems; Modulation; Bandwidth Requirements.

I (1.1, 1.2, 1.3, 1.4)

NOISE 04 hrs

External Noise; Internal Noise; Noise Calculations; Noise Figure; Noise Temperature.

I (2.1, 2.2, 2.3, 2.4, 2.5)

UNIT II

AMPLITUDE MODULATION 04 hrs

Amplitude Modulation Theory; Generation of AM.

I (3.1, 3.2)

SINGLE-SIDEBAND TECHNIQUES 04 hrs

Evolution and Description of SSB; Suppression of Carrier; Suppression of Unwanted Sideband; Extensions of SSB.

I (4.1, 4.2, 4.3, 4.4)

UNIT III

FREQUENCY MODULATION 07 hrs

Theory of Frequency and Phase Modulation; Noise and Frequency Modulation; Generation of Frequency Modulation.

I (5.1, 5.2, 5.3)

UNIT IV

RADIO RECEIVERS 08 hrs

Receiver Types; AM Receivers; FM Receivers; Single and Independent Sideband Receivers.

I (6.1, 6.2, 6.4, 6.5)

UNIT V

RADIATION AND PROPAGATION OF WAVES 03 hrs

Electromagnetic Radiation; Propagation of Waves.

I (8.1, 8.2)

WAVEGUIDES, RESONATORS AND COMPONENTS 05 hrs

Rectangular Waveguides; Circular and Other Waveguides; Waveguide Coupling, Matching and Attenuation; Cavity resonators.

I (10.1, 10.2, 10.3, 10.4)

UNIT VI

ANTENNAS 08 hrs

Basic Considerations; Wire Radiators in Space; Terms and Definitions; Effects of Ground on Antennas; Antenna Coupling at Medium Frequencies; Directional High-Frequency Antennas; UHF and Microwave Antennas; Wideband and Special Purpose Antennas.

I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6, 9.7, 9.8)

UNIT VII

PULSE COMMUNICATIONS 07 hrs

Information Theory; Pulse Modulation; Pulse Systems.

I (13.1, 13.2, 13.3)

UNIT VIII

BROADBAND AND COMMUNICATIONS SYSTEMS **07hrs**

Multiplexing; Short and Medium-Haul Systems; Long-Haul Systems; Elements of Long-Distance Telephony.

I (15.1, 15.2, 15.3, 15.4)

Text Book

I. Electronic Communication Systems, George Kennedy and Bernard Davis, Fourth Edition, (1999) Tata McGraw Hill Publishing Company Ltd.

Reference Books

1. Communication Systems, 4rd Edition, Simon Haykin, John Wiley & Sons.
2. Telecommunications Principles Circuits Systems and Experiments, S. Ramabhadran, Khanna Publishers, Sixth Edition.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 113 TELECOMMUNICATION SWITCHING SYSTEMS

UNIT I

SWITCHING SYSTEMS **08 hrs**

Evolution of Telecommunications; Network Structures; Network Services; Terminology; Regulation; Standards; The ISO Reference Model for Open Systems Interconnections; Basics of a Switching System; Functions of a Switching System; Message Switching; Circuit Switching; Crossbar Switching-Principle of crossbar switching, crossbar switch configurations, Crosspoint technology, Crossbar Exchange Organization; A General Trunking; Electronic Switching; Reed Electronic Systems; Digital Switching Systems.

I (1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 3.2, 3.3, 3.5, 3.10, 3.11, 3.12, 3.13); II (1.1, 1.3, 3.3, 3.4, 3.5, 3.6)

UNIT II

TELECOMMUNICATIONS TRAFFIC **08 hrs**

Introduction; The Unit of Traffic; Congestion; Traffic Measurement; A Mathematical Model; Lost-Call Systems-Theory; Traffic Performance; Loss Systems in Tandem; Use of Traffic Tables; Queuing Systems-The Second Erlang Distribution; Probability of Delay; Finite Queue Capacity; Some Other Useful Results; Systems with a Single Server; Queues in Tandem; Delay Tables; Applications of Delay Formulae.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III

SWITCHING NETWORKS **08 hrs**

Introduction; Single Stage Networks; Gradings-Principle; Design of Progressive Gradings; Other Forms of Grading; Traffic Capacity of Gradings; Application of Gradings; Link Systems-General, Two Stage Networks; Three Stage Networks; Four Stage Networks; Discussion; Grades of Service of Link Systems.

I (5.1, 5.2, 5.3, 5.4, 5.5)

UNIT IV

TIME DIVISION SWITCHING **07 hrs**

Basic Time Division Space Switching; Basic Time Division Time Switching; Time Multiplexed Space Switching; Time Multiplexed Time Switching; Combination Switching; Three Stage Combination Switching.

II (6.1, 6.2, 6.3, 6.4, 6.5, 6.6)

UNIT V

CONTROL OF SWITCHING SYSTEMS **07 hrs**

Introduction; Call Processing Functions-Sequence of Operations; Signal Exchanges; State Transition Diagrams; Common Control; Reliability; Availability and Security; Stored Program Control.

I (7.1, 7.2, 7.3, 7.4, 7.5)

UNIT VI

SIGNALLING **08 hrs**

Introduction; Customer Line Signaling; Audio Frequency Junctions and Trunk Circuits; FDM Carrier Systems-Outband Signaling; Inband (VF) Signaling; PCM Signaling; Inter Register Signaling; Common Channel Signaling Principles-General Signaling Networks; CCITT Signaling System Number 6; CCITT Signaling System Number 7; The High Level Data Link Control Protocol; Signal Units; The Signaling Information Field.

I (8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8, 8.9)

UNIT VII

PACKET SWITCHING **07 hrs**

Introduction; Statistical Multiplexing; Local Area and Wide Area Networks-Bus Networks; Ring Networks; Comparison of Bus and Ring Networks; Optical Fiber Networks; Large Scale Networks-General; Datagrams and Virtual Circuits; Routing; Flow Control; Standards; Frame Relay; Broadband Networks-General; The Asynchronous Transfer Mode; ATM Switches.

I (9.1, 9.2, 9.3, 9.4, 9.5)

UNIT VIII

NETWORKS **07 hrs**

Introduction; Analog Networks; Integrated Digital Networks; Integrated Services Digital Networks; Cellular Radio Networks; Intelligent Networks; Private Networks; Charging; Routing-General, Automatic Alternative Routing.

I (10.1, 10.2, 10.3, 10.4, 10.5, 10.6, 10.7, 10.9, 10.10)

Text Books:

I. Telecommunications Switching, Traffic and Networks, J.E.Flood, Pearson Education, Fourth Impression-2008.
II. Telecommunication Switching Systems and Networks, Thiagarajan Viswanathan, Prentice Hall of India Pvt. Ltd, Thirty-fifth Printing, August 2011.

Reference Book:

1. Digital Telephony, John C Bellamy, John Wiley International Student Edition.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 143 LOGIC DESIGN LAB

List of Experiments

1. **Study of Logic Gates:** Truth-table verification of OR, AND, NOT, XOR, NAND and NOR gates; Realization of OR, AND, NOT and XOR functions using universal gates.
2. **Implement Circuits using basic gates for the given Boolean expression.**
3. **Half Adder / Full Adder:** Realization using basic and XOR gates.
4. **Half Subtractor / Full Subtractor:** Realization using NAND gates.
5. **Parallel Adder / Subtractor:** Perform adder and subtractor operation using IC7483 chip.
6. **4-Bit Binary-to-Gray & Gray-to-Binary Code Converter:** Realization using XOR gates.
7. **4-Bit and 8-Bit Comparator:** Implementation using IC7485 magnitude comparator chips.
8. **Multiplexer:** Truth-table verification and realization of Half adder and Full adder using IC74153 chip.
9. **Demultiplexer:** Truth-table verification and realization of Half subtractor and Full subtractor using IC74139 chip.
10. **LED Display:** Use of BCD to 7 segment decoder / driver chip to drive LED display.
11. **Flip Flops:** Truth-table verification of JK Master Slave FF, T-type and D-type FF using IC7476 chip.
12. **Asynchronous Counter:** Realization of 4-bit up counter and Mod-N counter using IC7493 chip.
13. **Synchronous Counter:** Realization of 4-bit up/down counter and Mod-N counter using IC74192 chip.
14. **Shift Register:** Study of shift right, SIPO, SISO, PIPO and PISO operations using IC7495 chip.
15. **Ring counter and Twisted Ring Counter**: Realization using IC7495 chip.
16. **RAM:** Study of RAM (2K x 8 RAM) operation.

Note:

- All the experiments can be performed using IC Trainer Kits.
- Experiments are to be conducted in the hardware lab as well as using the software PSPICE 9.1 version and above downloadable at http://pspice.en.softonic.com

DE 114 DIGITAL COMMUNICATIONS

UNIT I

INTRODUCTION **02 hrs**

Sources and Signals; Basic Signal Processing Operations in Digital Communication; Channels For Digital Communications.

I (1.1, 1.2, 1.3)

FUNDAMENTAL LIMITS ON PERFORMANCE **05 hrs**

Uncertainty, Information and Entropy; Source Coding Theorem; Huffman Coding; Discrete Memoryless Channels; Mutual Information; Channel Capacity; Channel Coding theorem.

I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6, 2.7)

UNIT II

SAMPLING PROCESS **07 hrs**

Sampling Theorem; Quadrature Sampling of BP Signal; Reconstruction of a Message Process from its Samples; Signal Distortion in Sampling; Practical Aspects of Sampling and Signal Recovery; Pulse Amplitude Modulation; Time Division Multiplexing.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7)

UNIT III

WAVEFORM CODING TECHNIQUES **08 hrs**

Pulse Code Modulation; Channel Noise and Error Probability; Quantization Noise and Signal to Noise Ratio; Robust Quantization; Differential PCM; Delta Modulation.

I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6)

UNIT IV

BASE-BAND SHAPING FOR DATA TRANSMISSION **08 hrs**

Discrete PAM Signals; Power Spectra of Discrete PAM Signals; Inter Symbol Interference; Nyquist's Criterion for Distortionless Base-Band Binary Transmission; Correlative Coding; Eye Pattern, Base-Band M-ary PAM Systems; Adaptive Equalization for Data Transmission.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6)

UNIT V

DIGITAL MODULATION TECHNIQUES **08 hrs**

Digital Modulation Formats; Coherent Binary Modulation Techniques; Coherent Quadrature Modulation Techniques; Non-Coherent Binary Modulation Techniques; Comparison of Binary and Quaternary Modulation Techniques; M-ary Modulation Techniques; Effect of Inter Symbol Interference; Synchronization.

I (7.1, 7.2, 7.3, 7.4, 7.5, 7.10, 7.12)

UNIT VI

DETECTION AND ESTIMATION **07 hrs**

Gram-Schmidt Orthogonalization Procedure; Geometric Interpretation of Signals; Response of Bank of Correlators to Noisy Input; Detection of Known Signals in Noise; Probability of Error; Correlation Receiver; Matched Filter Receiver; Detection of Signals with Unknown Phase in Noise.

I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9)

UNIT VII

SPREAD SPECTRUM MODULATION **08 hrs**

Pseudo Noise Sequences; Notion of Spread Spectrum; Direct Sequence Spread Coherent Binary PSK; Signal Space Dimensionality and Processing Gain; Probability of Error; Frequency Hop Spread Spectrum.

I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6)

UNIT VIII

APPLICATIONS **07 hrs**

Applications of Waveform Coding Techniques; Applications of Digital Modulation Techniques; Applications of Spread Spectrum Modulation.

I (5.8, 7.13, 9.7)

Text book:

I. Digital Communications, Wiley Student Edition, Simon Haykin, , reprint 2012

Reference books:

1. Digital and Analog Communication Systems, K. Sam Shanmugham, John Wiley.
2. An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 115 EMBEDDED SYSTEMS

UNIT I

INTRODUCTION TO EMBEDDED SYSTEMS 07 hrs

Embedded Systems Overview; Design Challenge-Optimizing Design Metrics: Common Design Matrics, The time to Market Design Matric, The NRE and Unit Cost Design Metrics, The performance Design Metric; Processor Technology: GPPs, SPPs, ASIPs; IC Technology: Full Custom, Semicustom, PLD; Design Technology: Compilation, Libraries, Test; Trade-Offs: Design Productivity Gap.

I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6)

UNIT II

CUSTOM SINGLE PURPOSE PROCESSORS: HARDWARE 07 hrs

Introduction; Combinational Logic: Transistors and Logic Gates, Basic Combinational Logic Design, RT Level Combinational Components; Sequential Logic: Flip-Flops, RT Level Sequential Components, Sequential Logic design; Custom Single Purpose Processor Design; RT-Level Custom Single Purpose Processor Design; Optimizing Custom Single Purpose Processors: Optimizing the Original Program, FSMD, Datapath, FSM.

I (2.1, 2.2, 2.3, 2.4, 2.5, 2.6)

UNIT III

GENERAL PURPOSE PROCESSORS: SOFTWARE 08 hrs

Introduction; Basic Architecture: Datapath, Control Unit, Memory; Operation: Instruction Execution, Pipelining, Superscalar and VLIW Architectures; Programmer's View; Development Environment: Design Flow and Tools, Example(ISS for a simple processor), Testing and Debugging; ASIPs: Microcontrollers, DSPs ; Selecting a Microprocessor; General Purpose Processor Design

I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8)

UNIT IV

STANDARD SINGLE-PURPOSE PROCESSORS: PERIPHERALS 08 hrs

Introduction; Timers, Counters and Watchdog Timers: Examples of Reaction Timer and ATM Timeout Using a WDT; UART; Pulse Width Modulators: Overview, Controlling a DC Motor Using a PWM; LCD Controllers; Keypad Controllers; Stepper Motor Controllers: Overview, Examples; Analog to Digital Converters: Successive Approximation; Real Time Clocks.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9)

UNIT V

MEMORY 08hrs

Introduction; Memory Write Ability and Storage Permanence: Trade-offs; Common Memory Types: ROMs, RAMs; Composing Memory; Memory Hierarchy and Cache: Cache Mapping Techniques, Replacement Policy, Write Techniques, Impact on System Performance; Advanced RAM: The Basic DRAM, FPM DRAM, EDO DRAM, ES DRAM, RDRAM, MMU.

I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6)

UNIT VI

INTERFACING **08 hrs**

Introduction; Communication Basics; Microprocessor Interfacing: I/O Addressing; Microprocessor Interfacing: Interrupts; Microprocessor Interfacing: Direct Memory Access; Arbitration; Multilevel Bus Architecture; Advance Communication Principles; Serial Protocols; Parallel Protocols; Wireless Protocols.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7, 6.8, 6.9, 6.10, 6.11)

UNIT VII

INTRODUCTION TO REAL TIME OPERATING SYSTEMS **07hrs**

Tasks and Task States: The Scheduler, A Simple Example ; Tasks and Data: Shared-Data Problems, Reentrancy ; Semaphores and Shared Data: RTOS Semaphores, Initializing Semaphores, Reentrancy and Semaphores, Multiple Semaphores, Semaphores as a Signaling Device, Semaphore Problems, Ways to Protect Shared Data .

II (6.1, 6.2, 6.3)

UNIT VIII

CASE STUDIES OF PROGRAMMING WITH RTOS **07hrs**

Case Study of Coding for An Automatic Chocolate Vending Machine; Case Study of Coding for Sending Application Layer Byte Streams on TCP/IP Network; Case Study of An Embedded System for An Adaptive Cruise Control System in a Car.

III (11.1, 11.3, 12.3)

Text Books:

I. Embedded System Design, A Unified Hardware/Software Introduction, Frank Vahid / Tony Givargis, 2009 reprint, John Wiley Student Edition.
II. An Embedded Software Primer, David E. Simon, Tenth Impression 2011, Pearson Education.
III. Embedded Systems, Raj Kamal, Ninth reprint 2011, Tata-McGrawHill Publications.

Reference Book:

1. Embedded Microcomputer Systems, Jonathan W. Valvano, Fourth Indian reprint 2009, 2nd Edition, Thomson or Cengage Learning.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 144 ANALOG & DIGITAL COMMUNICATIONS LAB

List of Experiments

1. **Passive Attenuators:** T and π type – Design and study of attenuators for the given attenuation, source and load impedances.
2. **1st Order Active Filters:** Low pass and High pass – Design for a given cutoff frequency, passband gain and to obtain frequency response curve.
3. **Class C Tuned Amplifier:** Design for a particular tuned frequency, plot of Efficiency Vs Load and to obtain optimum load.
4. **Collector Amplitude Modulation:** Display of AM output, calculation of modulation index.
5. **AM Detector using Envelope Detector:** To study the variation of output signal amplitude and AVC output with variations in AF input.
6. **DSBSC generation using Diodes:** Study of output waveforms for variations in the input.
7. **FM Modulation:** Study and display of waveforms.
8. **FM Detection:** Study and display of waveforms.
9. **PAM:** Generation and demodulation – Observe input and output waveforms.
10. **PWM:** Generation for the given analog frequency and study of PWM output.
11. **OPAMP preemphasis and deemphasis:** Design for a given time constant and plot of Gain Vs Frequency.
12. **Transistor Mixer:** Demonstration of mixing action of RF and oscillator frequency to produce IF, to obtain conversion trans-conductance of the mixer.
13. **Verification of sampling theorem** using natural / flat top sampling.
14. **Generation and Detection of ASK:** Study and display of waveforms.
15. **Generation and Detection of PSK:** Study and display of waveforms.
16. **TDM:** Study of TDM and recovery of two band limited signals.

Note: Experiments are to be conducted in the hardware lab as well as using the software PSPICE 9.1 version and above downloadable at http://pspice.en.softonic.com

DE 116 WIRELESS & MOBILE SYSTEMS

UNIT I

INTRODUCTION 04 hrs

History of Cellular Systems; Characteristics of Cellular Systems; Fundamentals of Cellular Systems; Cellular System Infrastructure; Satellite Systems; Network Protocols; Ad Hoc and Sensor Networks; Wireless MANs, LANs and PANs.

I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8)

CHANNEL CODING AND ERROR CONTROL 04 hrs

Introduction; Linear Block Codes; Cyclic Codes; Cyclic Redundancy Check; Convolutional Codes; Interleaver.

I (4.1, 4.2, 4.3, 4.4, 4.5, 4.6)

UNIT II

MOBILE RADIO PROPAGATION 04 hrs

Introduction; Types of Radio Waves; Propagation Mechanisms; Free-Space Propagation; Land Propagation; Path Loss; Slow Fading; Fast Fading; Doppler Effect; Delay Spread; Intersymbol Interference; Coherence Bandwidth; Cochannel Interference.

I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, 3.12, 3.13)

CELLULAR CONCEPT 04 hrs

Introduction; Cell Area; Signal Strength and Cell Parameters; Capacity of a Cell; Frequency Reuse; How to form a Cluster; Cochannel Interference; Cell Splitting; Cell Sectoring.

I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9)

UNIT III

MULTIPLE RADIO ACCESS 03 hrs

Introduction; Multiple Radio Access Protocols; Contention-Based Protocols.

I (6.1, 6.2, 6.3)

MULTIPLE DIVISION TECHNIQUES FOR TRAFFIC CHANNELS 04 hrs

Introduction; Concepts and Models for Multiple Divisions; Modulation Techniques.

I (7.1, 7.2, 7.3)

UNIT IV

TRAFFIC CHANNEL ALLOCATION 03 hrs

Introduction; Static Allocation versus Dynamic Allocation; Fixed Channel Allocation (FCA); Dynamic Channel Allocation (DCA); Allocation in Specialized System Structure.

I (8.1, 8.2, 8.3, 8.4, 8.6)

MOBILE COMMUNICATION SYSTEMS 04 hrs

Introduction; Cellular System Infrastructure; Registration; Handoff Parameters and Underlying Support; Roaming Support; Multicasting.

I (10.1, 10.2, 10.3, 10.4, 10.5, 10.6)

UNIT V

EXISTING WIRELESS SYSTEMS 08 hrs

Introduction; AMPS; IS-41; GSM; PCS; IS-95; IMT-2000.

I (11.1, 11.2, 11.3, 11.4, 11.5, 11.6, 11.7)

UNIT VI

SATELLITE SYSTEMS 04 hrs

Introduction; Types of Satellite Systems; Characteristics of Satellite Systems; Satellite System Infrastructure; Call Setup; Global Positioning System.

I (12.1, 12.2, 12.3, 12.4, 12.5, 12.6)

AD HOC NETWORKS **04 hrs**

Introduction; Characteristics of MANETs; Applications; Routing; Table-Driven Routing Protocols; Source-Initiated On-Demand Routing.

I (13.1, 13.2, 13.3, 13.4, 13.5, 13.6)

UNIT VII

SENSOR NETWORKS **04 hrs**

Introduction; Wireless Sensor Networks; Fixed Wireless Sensor Networks.

I (14.1, 14.2, 14.3)

RECENT ADVANCES **03 hrs**

Introduction; Ultra-Wideband Technology; RFID; Cognitive radio; Directional and Smart Antennas.

I (16.1, 16.3, 16.5, 16.6, 16.11)

UNIT VIII

WIRELESS LANs, MANs and PANs **07 hrs**

Introduction; Wireless Local Area Networks (WLANs); Enhancement for IEEE 802.11 WLANs, Wireless Metropolitan Area Networks (MANs); Wireless Personal Area Networks (WPANs); Zigbee.

I (15.1, 15.2, 15.3, 15.4, 15.6, 15.7)

Text Book:

I. Introduction to Wireless and Mobile Systems, Third Edition (2011), Dharma Prakash Agrawal and Qing-An Zeng, CENGAGE Learning.

Reference Books:

1. Wireless Communications-Principles and Practice, Second Edition (2010), Theodore S. Rappaport, Pearson Education India.
2. Modern Wireless Communications , Simon Haykin and Michael Moher, Pearson Education, Low Price Edition.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 117 TELEVISION ENGINEERING AND BROADCASTING

UNIT I

ELEMENTS OF TELEVISION SYSTEM, ANALYSIS, SYNTHESIS OF TELEVISION PICTURES AND COMPOSITE VIDEO SIGNAL **08 hrs**

Picture and Sound Transmission and Reception; Synchronization; Receiver Controls and Color Television; Structure; Image Continuity; Number of Scanning Lines; Flicker; Fine Structure; Tonal Gradation; Video Signal Dimensions; Horizontal Sync Details; Vertical Sync Details; Scanning Sequence Details; Functions of Vertical Pulse Train; Sync Details of the 525 Line System.

I (1.1 to 1.7, 2.1 to 2.6, 3.1 to 3.6)

UNIT II

SIGNAL TRANSMISSION AND CHANNEL BANDWIDTH **07 hrs**

Amplitude Modulation; Channel Bandwidth; Vestigial Sideband Transmission; Transmission Efficiency; Complete Channel Bandwidth; Reception of Vestigial Sideband Signals; Frequency Modulation; FM Channel Bandwidth; Channel Bandwidth for Colour Television; Allocation of Frequency Bands for Television Signal Transmission.

I (4.1 to 4.11)

UNIT III

TELEVISION PICTURE TUBES AND CAMERA TUBES

Television Picture Tube: **04 hrs**

Monochrome Picture Tubes; Beam Deflection; Screen Phosphor; Face Plate; Picture Tube Characteristics; Picture Tube Circuit Controls.

Television Camera Tubes: **03 hrs**

Basic Principle; Image Orthicon; Vidicon; Plumbicon; Silicon Diode Array Vidicon; Solid State Image Sensors.

I (5.1 to 5.6, 6.1 to 6.6)

UNIT IV

BASIC TELEVISION BROADCASTING AND RECEPTION

Basic Television Broadcasting: **05 hrs**

Television Studio; Television Cameras; Programme Control Room; Video Switcher; Synchronizing System; Master Control Room (MCR); Generation of AM; TV Transmitters; Positive and Negative Modulation; Sound Signal Transmission; Merits of FM; Generation of FM; Stabilized Reactance Modulator; Generation of FM from PM; FM Sound Signal.

Television Receiver:

03 hrs

Types of TV Receivers; Receiver Sections; Vestigial Sideband Correction; Choice of IF; Picture Tube Circuitry and Controls; Sound Signal Separation; Sound Section; Sync Processing and AFC Circuit; Vertical and Horizontal Deflection Circuits.

I (7.1 to 7.15, 8.1 to 8.10)

UNIT V

VIDEO SECTION

Video Section Fundamentals: **04 hrs**

Picture Reproduction; Video Amplifier Requirements; Transistor Video Amplifier Video Driver; Contrast Control Methods; Screen Size and Video Amplifier Bandwidth.

Video Detector **03 hrs**

Video Signal Detection; Basic Video Detector; IF Filter; Video Detector Requirements; Functions of the Composite Video Signal.

I (11.1, 11.2, 11.3, 11.6, 11.7, 12.1, 12.2, 13.4, 13.9, 13.10)

UNIT VI

SOUND SECTION **04 hrs**

Sound Signal Separation, Sound Take-off Circuits; Inter-carrier Sound IF Amplifier; AM Limiting; FM Detection; FM Sound Detectors; Sound Section ICs; Audio Output Stage.

VERTICAL AND HORIZONTAL DEFLECTION CIRCUITS **04 hrs**

Miller Deflection Circuit; IC for Vertical System; Horizontal Amplifier Configurations; Horizontal Amplifier Controls; Transistor Horizontal Output Circuits; Horizontal Combination IC-CA.920.

I (21.1 to 21.8, 19.7, 19.8, 20.3, 20.6, 20.10, 20.12)

UNIT VII

COLOUR TELEVISION

Essentials of Colour Television: 04 hrs

Colour Reception; Three Colour Theory; Luminance, Hue and Saturation; Colour TV Camera, Colour TV Display tubes; Delta-Gun Colour Picture Tube; Precision-in-line (P.I.L.) Colour Picture Tube; Deflection Unit; Trinton Colour Picture Tube.

Colour Signal Transmission and Reception: 04 hrs

Colour Signal Transmission; Bandwidth; Modulation of Colour Difference Signals; Formation of Chrominance Signal; NTSC Colour TV System and Receiver; PAL Colour TV System; SECAM System.

I (25.3, 25. 4, 25. 25.5, 25.6, 25.10, 25.11, 25.13, 25.14, 25.17, 26.1, 26.2, 26.3, 26.5 to 26.7, 26.9, 26.15)

UNIT VIII

TELEVISION APPLICATIONS 07 hrs

Television Broadcasting; Cable Television; Closed Circuit Television (CCTV); Theatre Television; Picture Phone and Facsimile; Video Tape Recording (VTR); Television via Satellite and TV Games.

I (10.1 to 10.8)

Text Book:

I. Monochrome And Colour Television, Second Revised Edition, R.R.Gulati, New Age International Publishers, Reprint-2011.

Reference Books:

1. Modern Television Practice, Principles, Technology and Servicing, Second Edition, R.R.Gulati, New Age International Publishers, Reprint-2004.
2. Television and Video Engineering, A.M. Dhake, Second Edition, 2003, Tata-McGraw Hill.
3. Colour Television- Theory and Practice, S.P. Bali, TMH Publisher, 1994.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 118 DATA COMMUNICATION & NETWORKS

UNIT I

DATA COMMUNICATIONS, DATA NETWORKING, AND THE INTERNET 04 hrs

Data Communications and Networking for Today's Enterprise; A Communications Model; Data Communications; Networks; The Internet.

I (1.1, 1.2, 1.3, 1.4, 1.5)

DATA TRANSMISSION 04 hrs

Concepts and Terminology; Analog and Digital Data Transmission; Channel Capacity.

I (3.1, 3.2, 3.4)

UNIT II

TRANSMISSION MEDIA 03 hrs

Guided Transmission Media; Wireless Transmission.

I (4.1, 4.2)

PROTOCOL ARCHITECTURE, TCP/IP, AND INTERNET-BASED APPLICATIONS 04 hrs
The Need for a Protocol Architecture; The TCP/IP Protocol Architecture; The OSI Model; Standardization within a Protocol Architecture.
I (2.1, 2.2, 2.3, 2.4)

UNIT III

SIGNAL ENCODING TECHNIQUES 05 hrs
Digital Data, Digital Signals; Digital Data, Analog Signals; Analog Data, Digital Signals; Analog Data, Analog Signals.
I (5.1, 5.2, 5.3, 5.4)

DIGITAL DATA COMMUNICATION TECHNIQUES 03 hrs
Types of Errors; Error Detection; Line Configurations.
I (6.2, 6.3, 6.5)

UNIT IV

DATA LINK CONTROL PROTOCOLS 03 hrs
Flow Control; Error Control; High-Level Data Link Control (HDLC).
I (7.1, 7.2, 7.3)

MULTIPLEXING 04 hrs
Frequency-Division Multiplexing; Synchronous Time-Division Multiplexing; Statistical Time-Division Multiplexing.
I (8.1, 8.2, 8.3)

UNIT V

CIRCUIT SWITCHING AND PACKET SWITCHING 02 hrs
Switched Communications Networks; Circuit Switching Networks; Packet-Switching Principles.
I (10.1, 10.2, 10.5)

ROUTING IN SWITCHED NETWORKS 03 hrs
Routing in Packet-Switching Networks; Least-Cost Algorithms.
I (12.1, 12.3)

CONGESTION CONTROL IN DATA NETWORKS 02 hrs
Effects of Congestion; Congestion Controls.
I (13.1, 13.2)

UNIT VI

LOCAL AREA NETWORK OVERVIEW 04 hrs
Background; Topologies and Transmission Media; LAN Protocol Architecture; Bridges.
I (15.1, 15.2, 15.3, 15.4)

HIGH-SPEED LANs 02 hrs
The Emergence of High-Speed LANs; Ethernet.
I (16.1, 16.2)

WIRELESS LANs 02 hrs
Overview; Wireless LAN Technology.
I (17.1, 17.2)

UNIT VII

INTERNETWORK PROTOCOLS 08 hrs
Basic Protocol Functions; Principles of Internetworking; Internet Protocol Operation; Internet Protocol; IPv6.
I (18.1, 18.2, 18.3, 18.4, 18.5)

UNIT VIII

TRANSPORT PROTOCOLS **03hrs**

TCP; UDP

I (20.2, 20.4)

INTERNET APPLICATIONS **04 hrs**

Electronic Mail: SMTP and MIME; Network Management: SNMP; Internet Directory Service: DNS.

I (22.1, 22.2, 23.1)

Text Book:

I. Data and Computer Communications, Eight Edition, William Stallings, Pearson Education Low Price Edition.

Reference Book:

1. Data Communications and Computer Networks (2012), C.Murali, Reed Elsevier India Private limited (Fillip Learning, Bangalore).

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 119 ADVANCED COMMUNICATION SYSTEMS

UNIT I

OPTICAL FIBER TRANSMISSION MEDIA **08 hrs**

Introduction; History of optical fiber communications; Optical Fibers versus Metallic Cable Facilities; Electromagnetic Spectrum; Block Diagram of an Optical Fiber Communications System; Optical Fiber Types; Light Propagation; Optical Fiber Configurations; Losses in Optical Fiber Cables; Light Sources; Optical Sources; Light Detectors; LASERs; Optical Fiber System Link Budget.

I (13.1 to 13.15)

UNIT II

CELLULAR TELEPHONE CONCEPTS **07 hrs**

Introduction; Mobile Telephone Service; Evolution of Cellular Telephone; Cellular Telephone; Frequency Reuse; Interference; Cell Splitting, Sectoring, Segmentation and Dualization; Cellular System Topology; Roaming and Handoffs.

I (19.1 to 19.9)

UNIT III

CELLULAR TELEPHONE SYSTEMS **08 hrs**

Introduction; First-Generation Analog Cellular Telephone; Personal Communications System; Second-Generation Cellular Telephone Systems; N-amps; Digital Cellular Telephone; Interim Standard 95 (IS-95); North American Cellular and PCS Summary.

I (20.1 to 20.8)

UNIT IV

INTRODUCTION TO DATA COMMUNICATIONS AND NETWORKING **07 hrs**

Introduction; history of data communications; Data Communications Network Architecture, Protocols and Standards; Standards Organizations for Data Communication; Layered Network Architecture; Open Systems Interconnection; Data Communications Circuits; Serial and Parallel Data Transmission.

I (21.1 to 21.8)

UNIT V

FUNDAMENTAL CONCEPTS OF DATA COMMUNICATIONS 08 hrs

Introduction; Data Communication Codes; Bar Codes; Error Control; Error Detection; Error Correction; Character Synchronization; Data Communications Hardware; Data Communication Circuits; Line Control Unit; Serial Interfaces.

I (22.1 to 22.11)

UNIT VI

DATA-LINK PROTOCOLS AND DATA COMMUNICATIONS NETWORKS 08 hrs

Introduction; Data-Link Protocol Functions; Character- and Bit-oriented Data-Link Protocols; Asynchronous Data-Link Protocols; Synchronous Data-Link Protocols; Synchronous Data-Link Control; High-level Data-Link Control; Public Switched Data Networks; CCITT X.25 user-to-network Interface Protocol; Integrated Services Digital Network; Asynchronous Transfer Mode; Local Area Networks; Ethernet.

I (23.1 to 23.13)

UNIT VII

SATELLITE COMMUNICATIONS 07 hrs

Introduction; History of Satellites; Kepler's Laws; Satellite Orbits; Geosynchronous Satellites; Antenna Look Angles; Satellite Antenna Radiation Patterns: Footprints; Satellite System Link Models; Satellite System Parameters.

I (25.1 to 25.10)

UNIT VIII

SATELLITE MULTIPLE ACCESSING ARRANGEMENTS 07 hrs

Introduction; FDM/FM Satellite Systems; Multiple Accessing; Channel Capacity; Satellite Radio Navigation.

I (26.1 to 26.5)

Text Book:

I. Electronic Communications Systems, Fifth Edition, Wayne Tomasi, Pearsopn Education Publisher, Second Impression-2004.

Reference Books:

1. Digital Communication Techniques, Signaling and Detection, M.K. Simon, S.M. Hinedi and W.C. Lindsay, PHI, 1995.
2. Modern Digital and Analog Communication System, B.P. Lathi, 1998, 3rd Edition, Oxford University Press.
3. Satellite Communications, Dennis Roddy, Fourth edition, 2006, TMH Publisher.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 120 CONTROL ENGINEERING

UNIT I

MODELING OF SYSTEMS **07 hrs**

The Control System; Servomechanisms; The Control Problem; Introduction to Mathematical Models; Differential Equations of Physical Systems; Transfer Functions; Illustrative Examples.

I (1.1, 1.2, 1.6, 2.1, 2.2, 2.4, 2.7)

UNIT II

BLOCK DIAGRAMS AND SIGNAL FLOW GRAPHS **07 hrs**

Block Diagram Algebra; Signal Flow Graphs; Illustrative Examples.

I (2.5, 2.6, 2.7)

UNIT III

FEEDBACK CHARACTERISTICS OF CONTROL SYSTEMS **03 hrs**

Feedback and Non-Feedback Systems; Reduction of Parameter Variations by Use of Feedback; Control Over System Dynamics by Use of Feedback; Control of the Effects of Disturbance Signals by Use of Feedback; Illustrative Examples.

I (3.1, 3.2, 3.3, 3.4, 3.7)

CONTROL SYSTEMS AND COMPONENTS **04 hrs**

Introduction; Controller Components; Stepper Motors; Hydraulic Systems.

I (4.1, 4.3, 4.4, 4.5)

UNIT IV

TIME RESPONSE ANALYSIS **04 hrs**

Introduction; Standard Test Signals; Time Response of First and Second-Order Systems; Steady-State Errors and Error Constants; Effect of Adding a Zero to a System; Design Specifications of Second-Order Systems; Illustrative Examples; State Variable Analysis-Laplace Transform Technique.

I (5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.7, 5.10, 5.12)

CONCEPTS OF STABILITY **04 hrs**

Concept of Stability; Necessary Conditions for stability; Hurwitz Stability Criteria; Routh Stability Criteria; Relative Stability Analysis; Stability of Systems Modeled in State Variable Form.

I (6.1, 6.2, 6.3, 6.4, 6.5, 6.7)

UNIT V

ROOT LOCUS TECHNIQUE **07 hrs**

Introduction; Root Locus Concepts; Construction of ROOT LOCI; Sensitivity of Roots of Characteristic Equation.

I (7.1, 7.2, 7.3, 7.6)

UNIT VI

FREQUENCY DOMAIN ANALYSIS **08 hrs**

Introduction; Correlation Between Time and Frequency Response; Polar Plots; Bode Plots; All-Pass And Minimum-Phase Systems; Experimental Determination of Transfer Functions;

I (8.1, 8.2, 8.3, 8.4, 8.5, 8.6)

UNIT VII

STABILITY IN FREQUENCY DOMAIN **08 hrs**

Introduction; Mathematical Preliminaries; Nyquist Stability Criterion; Assessment of Relative Stability; Closed Loop Frequency Response; Sensitivity Analysis in Frequency Domain.

I (9.1, 9.2, 9.3, 9.4, 9.5, 9.6)

UNIT VIII

COMPENSATION **08 hrs**

The Design Problem; Preliminary Considerations of Classical Design; Realization Of Basic Compensators; Cascade Compensation in Time and Frequency Domains; Tuning of PID Controllers; Feedback Compensation.

I (10.1, 10.2, 10.3, 10.4, 10.5, 10.6, 10.7)

Text Book:

I. Control Systems Engineering, Fifth Edition, Reprint 2011, I.J. Nagrath and M. Gopal, New Age International Pvt. Ltd.

Reference Books:

1. Modern Control Engineering, D. Roy Choudhury, Prentice Hall India Pvt Ltd (2006)
2. Modern Control Engineering, K. Ogata, Pearson Education/Prentice-Hall of India Pvt. Ltd.
3. Schaum's Outline of Theory and Problems of Feedback and Control Systems, Second Edition (2007), J. J. DiStefano, III, A.R. Stubberud and I. J. Williams, Tata McGraw-Hill Publishing Company Ltd.
4. Modern Control Systems, Tenth Edition (2007), Richard. C. Dorf and Robert. H. Bishop, Pearson Education.
5. Automatic Control Systems, B.C. Kuo, Prentice-Hall of India Pvt. Ltd.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

DE 121 VERILOG HDL AND VLSI DESIGN

PART A: VERILOG HDL

UNIT I

OVERVIEW OF DIGITAL DESIGN WITH VERILOG HDL **08 hrs**

Evolution of Computer Aided Digital Design, Emergence of HDLs, Typical Design Flow, Hierarchical modeling Concepts, Modules and Ports.

I (1.1 to 4.3)

UNIT II

GATE LEVEL AND DATAFLOW MODELING **08 hrs**

Gate Types, Gate delays, Continuous Assignments, Delays, Expressions, Operators and Operands, Operator Types, Examples.

I (5.1 to 6.5.3)

UNIT III

BEHAVIORAL MODELING **07 hrs**

Structured procedures, Procedural Assignments, Timing controls, Conditional statements, Multi way Branching, Loops

I (7.1 to 7.6)

UNIT IV

TASKS AND FUNCTIONS **07 hrs**

Differences between Tasks and Functions, Tasks, Functions

I (8.1 to 8.3)

PART B: VLSI DESIGN

UNIT V

A REVIEW OF MICROELECTRONICS AND AN INTRODUCTION TO MOS TECHNOLOGY **07 hrs**

Introduction to Integrated Circuit Technology; The Integrated Circuit (IC) Era; Metal-Oxide-Semiconductor (MOS) and Related VLSI Technology; Basic MOS Transistors; Enhancement Mode Transistor Action; Depletion Mode Transistor Action; nMOS Fabrication; CMOS Fabrication

II (1.1 to 1.8)

3 **UNIT VI**

BASIC ELECTRICAL PROPERTIES OF MOS CIRCUITS **08 hrs**

Drain-to-source current I_{ds} versus Voltage V_{ds} Relationships; Aspects of MOS Transistor Threshold Voltage V_t;The Pass Transistor;The nMOS Inverter; Determination of Pull-up to Pull-down Ratio for an nMOS Inverter Driven by Another nMOS Inverter; Alternative Forms of Pull-up; The CMOS Inverter

II (2.1 to 2.10)

UNIT VII

MOS CIRCUIT DESIGN PROCESSES **07 hrs**

MOS Layer; Stick Diagrams; Design Rules and Layout; 2μm Double Metal, Double Poly.

I (3.1 to 3.4)

SCALING OF MOS CIRCUITS

Scaling Models and Scaling Factors; Scaling Factors for Device Parameters; Some Discussion on Scaling and Limitations of Scaling.

II (5.1 to 5.3)

UNIT VIII

PRACTICAL ASPECTS AND TESTABILITY **08 hrs**

Real World of VLSI Design; Design Styles and Philosophy; The Interface with the Fabrication House; CAD Tools for Design and Simulation; Aspects of Design Tools; Test and Testability.

II (10.8 to 10.13)

Text Books:

I. Verilog HDL- A Guide to Digital Design and Synthesis, Samir Palnitkar, Pearson Education, Second Edition, 2012.
II. Basic VLSI Design, Douglas A. Pucknell and Kamran Eshraghian, PHI, 3rd Edition, 2007

Reference Books:

1. CMOS Digital Integrated Circuits: Analysis and Design, Sung Mo Kang, Yusuf Leblebcci, TMH, 3rd Edition, 2002.
2. Principles of CMOS VLSI Design: A Systems Perspective, Neil Weste, Kamran Eshraghian, Pearson Education, 2nd Edition, 1994.
3. Verilog HDL primer, J.Bhasker, BS publication, 2001
4. Fundamentals of Digital Logic with Verilog Design, Stephen Brown, Zvonko Vranesic, Tata McGraw Hill, 2003.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks, selecting at least **TWO** questions from each Part.

DE 122 OBJECT ORIENTED PROGRAMMING WITH C++

UNIT I

OBJECT-ORIENTED PROGRAMMING CONCEPTS **08 hrs**

Software Evolution, Procedure-oriented Programming, Object-oriented Programming, Object-oriented Languages

LANGUAGE CONSTRUCTS

Introduction, Hello World Program, C++ Program Structure, Accepting User Input, Identifiers, Literals, Keywords, Data Types, Operators in C++, Program Statements

I (1, 2)

UNIT II

ADVANCED CONSTRUCTS **07 hrs**

Arrays, Multidimensional Arrays, Pointers, Structures

I (3)

UNIT III

CLASSES IN C++ **08 hrs**

Introduction, Data Type – Class, Declaring and Using Classes, Dynamic Objects, Defining Member Functions, Static Data Members and Functions

MEMBER FUNCTIONS

Passing Parameters, Constant Parameters, Default Parameters, Friend Functions

I (4, 5)

UNIT IV

OPERATOR OVERLOADING **07 hrs**

Adding 'Meaning' to Operators, Syntax for Operator Overloading, Overloading Arithmetic Operators, Overloading Complex Operators, What cannot be Overloaded?

CONSTRUCTORS AND DESTRUCTORS

Defining Constructor, Multiple Constructors, Using Parameterized Constructors in Dynamic Objects, Constructors with Default Arguments, Default Constructor, Copy Constructor, Class Destructor

I (6, 7)

UNIT V

INHERITANCE **08 hrs**

What is Inheritance, Single Inheritance, Access Modifiers, Multiple Level Inheritance, Public / Non-public Derivations, Types of Inheritance, Calling Sequence for Constructors and Destructors.

MULTIPLE INHERITANCE
Multiple Inheritance – An Illustration, Constructor Calling Sequence, Destructor Calling Sequence, Parameter Passing to Base Class Constructors, Access Modifiers, Protected Inheritance, Virtual Classes
I (8, 9)

UNIT VI

POLYMORPHISM **08 hrs**
The Meaning of Polymorphism, Types of Polymorphism, Static Polymorphism, Dynamic Polymorphism, Virtual Functions
HANDLING EXCEPTIONS
Exceptional conditions, The Try/Catch/Throw Constructs, Throwing Exceptions, Rethrowing Exceptions
I (10) (Mentioned topics in 11)

UNIT VII

TEMPLATES **07 hrs**
Need for Templates, Types of Templates, Function Templates, Class Templates, User-defined Data Types as Parameters
I (12)

UNIT VIII

C++ I/O **07 hrs**
The C++ I/O Systems, Streams, File I/O, Random Access Files
I (13)

Text Book:
I. Object-oriented Programming with C++, Poornachandra Sarang, PHI, 2004

Reference Book:
1. Big C++, Cay Horstmann, Timothy A. Budd, Wiley India, 2005

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks.

4 **DE 123 JAVA & WEB PROGRAMMING**

PART A: JAVA

4.1 UNIT I

JAVA EVOLUTION **07 hrs**
Java History, Java Features, How Java Differs from C and C++, Java and Internet, Java and World Wide Web, Web Browsers, Hardware and Software Requirements, Java Support Systems, Java Environment

4.1.1.1 **OVERVIEW OF JAVA LANGUAGE**
Introduction, Simple Java Program, More of Java, An Application with Two Classes, Java Program Structure, Java Tokens, Java Statements, Implementing a Java Program, Java Virtual Machine, Command Line Arguments, Programming Style.

4.1.1.2 **I (2, 3)**

4.1.2 UNIT II

4.1.3 CONSTANTS, VARIABLES AND DATA TYPES 08 hrs

Introduction, Constants, Variables, Data Types, Declaration of Variables, Giving Values to Variables, Scope of Variables, Symbolic Constants, Type Casting, Getting Values of Variables, Standard Default Values.

4.1.3.1 **OPERATORS AND EXPRESSIONS**

Introduction, Arithmetic Operators, Relational Operators, Logical Operators, Assignment Operators, Increment and Decrement Operators, Conditional Operator, Bitwise Operators, Special Operators, Arithmetic Expressions, Evaluation of Expressions, Precedence of Arithmetic Operators, Type Conversion in Expressions, Operator Precedence and Associativity, Mathematical Functions.

DECISION MAKING AND BRANCHING

Introduction, Decision Making with If Statement, Simple If Statement, The If…Else Statement, Nesting of If…Else Statements, The Else If Ladder, The Switch Statement, The ?: Operator.

DECISION MAKING AND LOOPING

Introduction, The While Statement, The do Statement, The for Statement, Jumps in Loops, Labeled Loops

4.1.3.2 **I (4, 5, 6, 7)**

4.1.3.3 UNIT III

4.1.3.3.1 CLASSES, OBJECTS AND METHODS 07 hrs

Introduction, Defining a Class, Fields Declaration, Methods Declaration, Creating Objects, Accessing Class Members, Constructors, Methods Overloading, Static Members, Nesting of Methods, Inheritance: Extending a Class, Overriding Methods, Final Variables and Methods, Final Classes, Finalizer Methods, Abstract Methods and Classes, Methods with Varargs, Visibility Control.

4.1.3.3.2 **ARRAYS, STRINGS AND VECTORS**

Introduction, One-dimensional Arrays, Creating an Array, Two-dimensional Arrays, Strings, Vectors, Wrapper Classes, Enumerated Types, Annotations.

I (8, 9)

4.1.4 UNIT IV

4.1.4.1.1 **INTERFACES: MULTIPLE INHERITANCE 08 hrs**

Introduction, Defining Interfaces, Extending Interfaces, Implementing Interfaces, Accessing Interface Variables.

PACKAGES: PUTTING CLASSES TOGETHER

Introduction, Java API Packages, Using System Packages, Naming Conventions, Creating Packages, Accessing a Package, Using a Package, Adding a Class to a Package, Hiding Classes, Static Import

MULTITHREADED PROGRAMMING

Introduction, Creating Threads, Extending the Thread Class, Stopping and Blocking a Thread, Life Cycle of a Thread, Using Thread Methods, Thread Exceptions, Thread Priority, Synchronization, Implementing the 'Runnable' Interface

4.1.4.1.2 **I (10, 11, 12)**

4.1.5 UNIT V

MANAGING ERRORS AND EXCEPTIONS 07 hrs

Introduction, Types of Errors, Exceptions, Syntax of Exception Handling Code, Multiple Catch Statements, Using Finally Statement, Throwing Our Own Exceptions, Using Exceptions for Debugging.

MANAGING INPUT/OUTPUT FILES IN JAVA

Introduction, Concept of Streams, Stream Classes, Byte Stream Classes, Character Stream Classes, Using Streams, Other Useful I/O Classes, Using the File Class, Input/Output Exceptions, Creation of Files, Reading/Writing Characters, Reading/Writing Bytes, Handling Primitive Data Types.

4.1.5.1.1 **I (13), (16.1 to 16.13)**

PART B: WEB PROGRAMMING

UNIT VI

WEB BASICS AND OVERVIEW **08 hrs**

The Web, Content Types, Putting Information on the Web, What is HTML?, Web Hosting, Domain Registration, What are Name Servers, Looking up Host Information, The Web Development Process, Dynamic Generation of Web Pages, HTTP Briefly.

CREATING WEB PAGES: XHTML

HTML Basics, Creating Your First Web Page, Elements & Entities, A Brief History of HTML, XHTML Syntax, Core Attributes, Heading and Paragraphs, White Spaces and Line Wrapping, Inline Elements, Controlling Presentation Styles, Length Units, Colours, Text Fonts, Lists, List Styles, Hyperlinks, Images, Positioning Inline Images, Image Maps, Editing HTML.

II (1.4 to 1.14, 2)

UNIT VII

ADVANCED XHTML **08 hrs**

Character Encoding, Special Symbols and HTML Entities, Tables, Cell Content Alignment, Displaying Tables, Formatting Tables, Positioning Tables, Table Width and Height, Grouping Rows and Columns, Forwarding Pages, Frames, Server-side Includes, Internationalization, Common Page errors, Page Checking and Validation.

DESIGN BASICS

What is Design?, Design and Perception, Elements of Design, Unity and Variety, Emphasis, Focal Point, and Hierarchy, Contrast, Visual Balance.

INFORMATION ARCHITECTURE AND PAGE LAYOUT

Layout Overview, Web Site Architectures, Information Architecture, Client Identity, Organizational Framework, Layout Grids, Web Page Layout Grids, Designing Layout Grid Systems.

II (3.1 to 3.9, 3.15, 3.18 to 3.22, 4.1, 4.2, 4.4 to 4.8, 5.1, 5.2, 5.3, 5.5, 5.6, 5.12, 5.13, 5.14)

UNIT VIII

4.1.5.1.1.1 **CSS, FORMS AND FORM PROCESSING** **07 hrs**

What is CSS?, Overall Styling of a Page, What is a Form?, Form Basics, Text Input, User Selections, Submit Buttons, File Uploading, Other Input Elements, HTTP Basics, HTTP Message Format, CGI Overview, Outline of a CGI Program, Getting Started with CGI Programming, Deploying CGI Programs.

CLIENT-SIDE SCRIPTING: JAVASCRIPT

Getting Started, Embedding JavaScript in a Web Page, JavaScript Objects, Windows, Form Checking, Events and Event Objects, Testing and Debugging.

II (6.1, 6.2, 8.1, 8.3 to 8.8, 8.11 to 8.16, 9.1, 9.2, 9.11, 9.12, 9.15, 9.17, 9.19)

Text Books:

I. Programming with Java – A Primer, E. Balagurusamy, Third Edition, TMH, 2007.
II. An Introduction to Web Design + Programming, Paul S. Wang and Sanda S. Katila, Thomson Course Technology, India Edition, 2008.

Note: Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 16 marks, selecting **THREE** questions from Part A and **TWO** from Part B.

DE 138 (WRITTEN) COMMUNICATION SKILLS AND TECHNICAL WRITING

UNIT I

COMMUNICATION: ITS TYPES AND SIGNIFICANCE **06 hrs**

What is Communication; Process of Communication; Types of communication; The Media of Communication; Barriers in Communication; Effective Communication.

I (1.1, 1.2, 1.3, 1.4, 1.5, 1.6)

UNIT II

GRAMMAR **07 hrs**

Synonyms; Antonyms; Words used as different parts of Speech; Spotting errors; Concord; Principle of proximity between subject and verb.

I (4.1, 4.2, 4.3, 4.6, 4.7, 4.8)

UNIT III

SYNTAX **06 hrs**

Sentence Structure; Combination of Sentences; Transformation of Sentences; Verb Patterns in English.

I (5.1, 5.2, 5.3, 5.4)

UNIT IV

READING SKILLS **07 hrs**

The Purpose of Reading; The Process of Reading; How to get Concentration in Reading; Reading Strategies; Reading Comprehension; Preparing outlines.

I (2.1, 2.2, 2.3, 2.5, 2.6, 2.11)

UNIT V

WRITING SKILLS **07 hrs**

Effective Writing; Job Application, Bio-data, Personal Resume and Curriculum Vitae; Agenda and Minutes of a Meeting; Back office job for organizing a conference/seminar; Writing Styles; Scientific and Technical Writing; Writing paragraphs; Writing Essays.

I (3.1, 3.2, 3.3, 3.4, 3.5, 3.6, 3.9, 3.11)

UNIT VI

5 **LISTENING SKILLS** **04 hrs**

5.1 The Process of listening; Two Styles of Communication; Soft Skills; Feedback Skills; Essentials of Good Communications; Types of Listening; Barriers to Listening; Note taking and Note making.

I (8.1, 8.2, 8.3, 8.4, 8.6, 8.7 8.8, 8.9)

SPEAKING SKILLS **03 hrs**

Skills of Effective Speaking; the Components of an Effective Talk; Tone of Voice; Body Language; Timing and Duration of Speech; Audio-Visual Aids in Speech.

I (9.1, 9.2, 9.4, 9.5, 9.6, 9.7)

UNIT VII

TECHNICAL REPORT AND SCIENTIFIC REPORT 06 hrs

Writing a good report; Types of Report; Structure of Reports; Collecting Data; Visual Aids; Tips for Writing Reports.

I (15.1, 15.2, 15.3, 15.4, 15.8, 15.9)

UNIT VIII

CAMPUS RECRUITMENT, INTERVIEW AND GROUP DISCUSSION 03 hrs

Main Features of Campus Recruitment; Tips for giving an Interview; Body language for Interviews; Group Discussion.

I (10.1, 10.2, 10.3, 10.4)

MEETINGS NEGOTIATIONS PHONE AND MOBILE PHONE SKILLS 03 hrs

Conducting Meetings, Skills for Participating in a Meeting; Attending Telephonic Calls.

I (11.1, 11.2, 11.5)

Text Book:

I. The Functional Aspects of Communication Skills, Prajapati Prasad, S. K. Kataria & Sons, New Delhi, Fifth Edition, July 2011-12

Reference Books:

1. Business Communication, Sinha K. K, S. Chand, New Delhi.
2. Business Communication, Asha Kaul, Prentice Hall of India.
3. Business Correspondence and Report Writing: A Practical Approach to Business and Technical Communication, Sharma, R.C. and Krishna Mohan, Tata McGraw-Hill.
4. A New Approach to English Grammar for High Schools, Madan Sabina, Spectrum Books, New Delhi.

NOTE: Examination procedure.

(a) Theory: Consists of written examination for 80 marks.

(b) Students have to answer **FIVE** full questions out of **EIGHT** questions to be set from each unit carrying 12 marks.

DE 137 (ORAL)

Oral Test: Consists of an Oral Test to test the Communication Skills which includes an oral presentation on any subject, of the choice of students (e.g. About IETE, General Knowledge topics etc.). This presentation need not be on technical subject. This test carries **20** marks.

GENERAL GUIDELINES for DIPIETE Project work and Seminar

PROJECT WORK

Eligibility

For eligibility students may refer to the website **www.iete.org**

The project will consist of hardware/software, design/development, experimental / theoretical work of a contemporary topic or a combination of these. There will be no joint project work.

The students may work for the project in any industry, in any educational institution or in R&D laboratory. The student will be required to have a project guide from one of these places who can supervise and guide. In case of difficulties, the students may contact the local centre.

Pass marks for the project will be 5 GPA. Students not getting 5 GPA marks will be required to re-register for the project following the usual procedure. The students will have the option of taking up a new project or continue with the earlier project.

DE 135 Project work

Eligible students are required to forward their applications for registration of Project Work to the respective IETE Centres/Sub Centres where the examinations are conducted. The applications should include the synopsis of the Project Work, guide's bio-data and his willingness letter to guide the student, along with requisite project fees.

Project guide

Project guide can be chosen from any one of the following categories

(a) An academic person with a Master's qualification in Engineering having atleast 5 years of experience
(b) A person working in industry/institution with a Bachelor's degree in Engineering having atleast 10 years of experience
(c) IETE corporate member with 10 years of experience

DE 135 Project work

Execution of the Project Approved and Submission of Project Reports

A student is expected to put in at least 6 hours/week spread over a period of 12 weeks for the project after the same has been approved.

Two bound copies of the project report are required to be submitted by the student (one copy for Evaluation board & one copy for IETE HQ record) to their respective local Centres who will intimate the date, time and venue for appearing before the Evaluation Board & presentation of the Project Work by the student.

Evaluation Board

The Regional Evaluation Board already set up for scrutinizing of the proposals will also form the Evaluation Board for assessment of the final Project Reports with one of the member acting as Chairman of the Evaluation Board. **IETE Centre will only act as facilitator and are not to be associated with the Examination Work**.

Evaluation is for 200 Marks (8 Credits)

The following points are required to be checked by the Evaluation Board at the time of assessment of the Project Reports.

(a) **Time Limit;** The Project Report is required to be completed within a period of one year.
(b) **Project Report;** The Project Report should contain the following certificate from the guide:

CERTIFICATE

This is to certify that this is a bonafide record of the Project Work done satisfactorily at _____ by Mr/Ms. _____ in partial fulfillment of his/her AMIETE Examination. This report has not been submitted for any other examination and does not form part of any other course undergone by the candidate.

(Signature, Name, Designation
and Address of the Guide with the seal of
the Organization/Institution/Laboratory)

Project Fee

Project Fee of Rs.1200/- is required to be submitted by the student while forwarding his/her application for the project work. The DD of requisite amount is to be drawn in favour of the IETE Centre.

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DE 136 SEMINAR

Eligibility:
For eligibility students may refer to the website **www.iete.org**

Registration:
Eligible students are required to submit their applications for the registration of seminar to the respective Centres/Sub-Centres where the examinations are conducted with a brief write up of the topic selected for approval. Seminar topic should be selected from the emerging technologies in ET,CST only. Students who have undergone industrial training may make their presentation of their training report.

Scrutiny/Approval of Seminar proposals:
The members of Regional Evaluation Board will approve the topic of seminar. The students should make presentation on approved topics only.

Seminar Fees:
Each student is required to pay Rs.600/- Seminar fee to the respective IETE Centre/Sub-Centre.

Examination/Evaluation:
The IETE Centre / Sub-Centre will fix up a suitable date immediately after the main examination for the conduct of Seminar. The students should make Power Point presentation on the approved topic. In addition, they have to submit a complete report on the Seminar topic presented.

Evaluation is for 100 Marks (4 Credits)

Appendix 'F'

[TO BE PUBLISHED IN PART-1 SECTION -I OF GAZATTE OF INDIA]

Government of India
Ministry of Human Resource Development
Department of Secondary & Higher Education
****

Shastri Bhavan, New Delhi,
the 16th January, 2006

NOTIFICATION

No.F.24 - 7 /2002 - TS.III. On the recommendations of the High Level Committee for recognition, Government of India have decided to recognize the Diploma in Computer Science & Engineering, DIPIETE (Computer Science & Engineering) conducted by the Institution of Electronics & Telecommunication Engineers, New Delhi, till further orders for the purpose of employment to the posts and services under the Central Government in the appropriate field.

The recognition will be effective from the year 2002, till further orders.

(Ravi Mathur)
Joint Secretary to the Government of India
Tel: 2338 1097

To

The Manager,
Government of India Press,
Faridabad.

Contd./-

NITI\C:\Ghildiyal\HIGH LEVEL COMMITTEE

Appendix 'G'

GOVERNMENT OF KARNATAKA

No. BTE 36 ERS (2) 92

Office of the Secretary,
Board of Technical Examinations,
Bangalore-1,
Dated 22.12.1992.

To

The Secretary,
Institute of Electronic & Telecommunication,
No.2, Institutional Area,
Lodi Road,
NEW DELHI.

Sir,

Sub:- Recognisation by Government of India of Diploma Level Examination in Electronic conducted by your Institution.

Ref:- 1. Notification 38 (F.18-9/89 TD-V dt.5.8.92 of Govt. of India, Ministry of Human Resource Development, New Delhi.

2. G.O.No. GAD 35 SRR 64 dt.20th April 1965 of Govt. of Karnataka.

I wish to inform you that the Diploma in Electronic conducted by your institution has been recognised by Government of India (vide ref. 1). Hence, the Diploma in Electronic conducted by your institution stands automatically recognised by Government of Karnataka as per Karnataka Government Order cited under reference(2)

Yours faithfully,

SECRETARY,
BOARD OF TECHNICAL EXAMINATIO
BANGALORE.

GOVERNMENT OF RAJASTHAN

BOARD OF TECHNICAL EDUCATION,RAJ.JODHPUR

NO.F5(7-11)A/Gen/BTE/99/ 7957 Dated: 30/10/99

Asstt. Secretary(ACAD)
The Institution of Electronics
and Tele communication Engineers,
Institutional Area, Lodi Road,
New Delhi-110003

Sub:Recognition of Diploma I.E.T.E
Ref:IETE/769/Exam/99 Dt.16.6.98

Sir,

It is to inform you that Govt. of Rajasthan Department of Technical Education as per there order No P.1(10) T.E./92 dated 13.10.99(Copy enclosed) has recognised this Diploma in electronics and Telecumminaction awarded by your as equivalent to 3 years Diploma course awarded by this Board.

Yours Faithfully

(M.D. Bhargava 30.10.99

Dy. Director(conf.)

Encls:As above

WEST BENGAL STATE COUNCIL OF TECHNICAL EDUCATION

(A Statutory Body Under West Bengal Act XXI of 1995)

No. 1063-SC(T)E Date 10th Oct., 2002.

From : The Secretary,
W.B.State Council of Tech.Education.

To : The Director, Academic
The Institution of Electronics & Tele-Communication Engineers (Calcutta Centre),
Salt Lake Electronics Complex,
EP Block, Plot No.JI-7,Sector-V,
Kolkata- 700091.

Sub :- Recognition of Diploma IETE(Diploma Level)in the field of Electronics & Tele-Communication Engg.

Ref :- Your letter No.IETE/Cal/Recog-SCTE/2001/2002.

It appears that the Diploma level examination in Electronics conducted by the Institution of Electronics & Tele-Communication Engineers is recognised by the MHRD, Government of India for the purpose of employment of posts and services under the Central Government in the appropriate field.

In this connection it is intimated that according to existing procedure any course recognised by Government of India in the Ministry of Human Resource Development is also recognised by All State Governments/Union Teretories and as such no further recognition notification is required to be issued from this end.

10/10/2002

(R. C. BHATTACHARYA)
Secretary,
W.B.State Council of Tech. Education.

प्रेषक,

तकनीकी शिक्षा आयुक्त एवं विशेष सचिव,
हरियाणा सरकार, तकनीकी शिक्षा विभाग,
चण्डीगढ ।

सेवा में,

प्रधान सचिव,,
इलैक्ट्रोनिक्स एवं टैलीकम्यूनिकेशन इंजीनियर संस्थान,
2, इंस्टीच्यूशनल ऐरिया, लोदी रोड़,
नई दिल्ली 110 003

यादी कमांक 95 /शैक्षिक,
दिनांक : 18-2-03

विषय : **Regarding – Recognition of Diploma by Haryana Govt.**

उपरोक्त विषय पर आपके यादी कमांक : आई.ई. टी.ई.769/2002/दिनांक 11.12.02 के संदर्भ में ।

2. इस सम्बन्ध में सूचित किया जाता है कि जो डिप्लोमा/डिग्रीयां भारत सरकार तथा अखिल भारतीय तकनीकी शिक्षा परिषद द्वारा मान्यता प्राप्त है वही डिप्लोमे हरियाणा राज्य द्वारा भी मान्यता प्राप्त हैं ।

उप – निदेशक,
कृते:तकनीकी शिक्षा आयुक्त एवं
विशेष सचिव, हरियाणा सरकार,
तकनीकी शिक्षा विभाग, चण्डीगढ
7/2/03

ફોન : (૦૭૯) ૬૩૦૧૧૪૭
ટેલિફોન : ૬૩૦૧૩૪૧-૬૩૦૦૩૪૨-૪૩,
૬૩૦૦૧૨૬ અને ૬૩૦૦૬૬૪
ટેલિગ્રામ : યુનિગુજરાત

FAX : (079) 6301654
Telc. { Phone : 6301341-6300342-43, 6300126 & 6300664
grams. UNIGUJARAT

ગુજરાત યુનિવર્સિટી
GUJARAT UNIVERSITY

ગુજરાત યુનિવર્સિટી કાર્યાલય,
પોસ્ટ બોક્સ નં. ૪૦૧૦,
નવરંગપુરા, અમદાવાદ-૩૮૦ ૦૦૯.

OFFICE OF THE GUJARAT UNIVERSITY
POST BOX No 4010,
NAVRANGPURA,
AHMEDABAD-380 009 (INDIA)

No. Exam/3A/Eli/ 6370 /2002 Date : 12/9/2002

To,

The Chair Person,
I.E.T.C. 4 - IETE
206, Umiya Shopping Centre
Satelite Road,
Ahmedabad-380 015

Sub:- Recognition of AMIETE/DIPIETE Course.

Madam,

With reference to your letter No.IETE/Ch/2/2001 dated 6/12/2001 on the subject mentioned above, I am to inform you that on the recommendation of the Standing Committee on equivalence of examination of the University held on 26/8/2002, It has been resolved that the examinations of AMIETE/DIPIETE are recognized as equivalent to B.E./DIPLOMA examination by this University.

Thanking you,

Yours faithfully,

for Registrar

UNIVERSITY OF CALICUT

(Abstract)

Recognition of Diploma in Electronics and Telecommunication Engineering regular Diploma awarded by Institution of Electronics and Telecommunication Engineers, New Delhi as equivalent to 3 years Diploma awarded by State Board of Technical Education – Granted – Orders issued.

GENERAL AND ACADEMIC BRANCH – I 'A' SECTION

No.GAI/A1/6988/05 Dated, Calicut University P.O, 12.08.2009.

Read: 1. Minutes of the meeting of Board of Studies in Electrical, Electronics and Communication Engineering, Instrumentation and Control Engineering Applied Electronics and Instrumentation Engineering (UG) held on 30-03-2006, item No.4.

2. Minutes of the meeting of Faculty of Engineering held on 06-06-2006 item No.5.

3. Minutes of the meeting of Academic Council held on 05-04-08 item No.B-5.

ORDER

The meeting of the Board of Studies in Electrical, Electronics and Communication Engineering, Instrumentation and Control Engineering Applied Electronics and Instrumentation Engineering (UG) held on 30-03-2006, vide paper read first, considered the recognition of Diploma in Electronics and Telecommunication Engineering (regular Diploma) awarded by the Institution of Electronics and Telecommunication Engineers, New Delhi, and decided to recognise the same as equivalent to 3 years diploma awarded by State Board of Technical Education.

The meeting of Faculty of Engineering held on 06.06.2006 and the Academic Council held on 05.04.2008 as paper read 2nd and 3rd above, approved the decision of the Board of Studies.

Sanction has therefore been accorded to recognise the regular Diploma in Electronics and Telecommunication Engineering awarded by the Institution of Electronics and Telecommunication Engineers, New Delhi as equivalent to 3 years Diploma awarded by State Board of Technical Education.

Orders are issued accordingly.

Sd/-
DEPUTY REGISTRAR (G&A–I)
For REGISTRAR

To

K.M. Ajas
Karimbil Manalath (H),
Mundathicode (PO),
Trichur – 680595.

Copy to:
1. The Assistant Secretary (Acad)
   Institute of Electronics & Telecommunication Engineers,
   New Delhi.
2. The Controller of Examinations
3. Director, Technical Education, Government of Kerala
4. Entrance Commissioner, Trivandrum.
5. E.R.D.I.
6. GAI/'E' Section
7. PS to VC/PA to PVC/PA to Registrar
8. SF/DF/FC

Forwarded / By Order

SECTION OFFICER

From

The Director,
Technical Education, U.T.
Chandigarh.

To

The Secretary,
Institution of Electronics &
Telecommunication Engineers,
2, Institutional Area Lodi Road,
New Delhi-110003

Memo. No. F. 213/EA(P&EC)-92/1896
dated, Chandigarh, the 16/12/92

Subject: Recognition of Diploma Level Examination in Electronics and Telecommunication conducted by the Institution of Electronics and Telecommunication Engineers, New Delhi.

Reference your letter no. IETEI/769/Exam/92/ dated 23.10.92, on the subject noted above.

In this connection, it is intimated that the notification regarding recognition of diploma course cited as subject accorded/received from the Govt.of India, Ministry of Human Resource Development, New Delhi is applicable to all state Govt./ Union Territories as such no further recognition notification is required to be issued by this Directorate.

15/12

Director Technical Education,
Union Territory, Chandigarh.

1 DEC 1992

Government of India
Ministry of Human Resource Development
Department of Education

Copy of MHRD Letter No.F.24-7/2002-TS.III Dated 10th January, 2006.

To,

The Secretary General,
Institution of Electronics & Telecommunication Engineers,
Delton House, Lodhi Road,
New Delhi

Subject:- Permanent recognition to the Diploma in Electronics and Telecommunication Engineering (DIPIETE-ETE) run by the Institution of Electronics and Telecommunication Engineers, New Delhi

Sir,

I am directed to inform that the issue of permanent recognition was discussed by the High Level Committee in its 9th meeting held on 16.11.2005. While giving the approval to the permanent recognition to the course namely, Diploma in Electronics and Telecommunication Engineering run by IETE, the Committee took the policy decision as under.

"Henceforth, the recognition to the courses, granted by the High Level Committee shall be permanent till it is withdrawn either due to deficiencies identified by AICTE or the genuine complaints received against the Institutions".

The Institution is required to put all the details about their educational activities on the website of the All India Council for Technical Education in the format prescribed for the purpose. AICTE can conduct a random review of the courses run by the Institutes to ascertain the standard and level.

Yours faithfully,

Sd/-
(Dr. G.L. Jambhulkar)
Deputy Educational Advisor

Extract of Notification dated 16 Jan 2006

Extract of Notification No. F.24-7/2002 - TS.III. On the recommendations of the High Level Committee for recognition, Government of India have decided to recognize the Diploma in Computer Science & Engineering, DIPIETE (Computer Science & Engineering) conducted by the Institution of Electronics & Telecommunication Engineers, New Delhi, till further orders for the purpose of employment to the posts and services under the Central Government in the appropriate field.

The recognition will be effective from the year 2002, till further orders.

Present Status of Recognition of IETE Courses by MHRD

Current status in respect of IETE writ petition No. W.P.(C.) N. 3239/2013 & CM Appl. 6125/2013 in respect of recognition of its Courses by MHRD.

The above writ petition filed by IETE HQ in Delhi High Court on 13 May 2013 came up for 5th hearing on 09 Jan 2014.

The Hon'ble High Court directed the parties to complete the pleadings before the Joint Registrar on 23 Apr 2014 before the next date of hearing. The Joint Registrar is directed to list these matters before the Court after completion of the pleadings. **Interim Order will continue (Stay)**.

Issued by
Secretary General
For and on behalf of The Institution of Electronics and Telecommunication Engineers (IETE)

Status in respect of recognitions granted for the examinations conducted by IETE.

A writ petition was filed by the Institution in Delhi High Court on 13 May 2013 for quashing the orders of MHRD dated 10 July 2012 and 06 Dec 2012 withdrawing the recognition in perpetuity for equivalence in Central Govt jobs after 31 May 2013. The writ petition came up for hearing on 17 May, 21 May and 23 May 2013.

The Hon'ble High Court, Delhi is pleased to stay the orders of the Ministry of Human Resource Development dated 06 Dec. 2012 with respect to the dead line of 31 May 2013 till the next date of hearing i.e. 06 Aug 2013. However, the admissions, which are made, will be subject to final orders, which will be passed in the writ petition.

The matter came up for further hearing before the Delhi High Court on 06 Aug 2013.

On the last date of hearing of our Writ Petition in Hon. High Court Delhi, following order has been issued

(i) The case listed for next hearing on 9th January 2014.

(ii) The OM dated 6/12/2012 with respect to the dead line of

31/05/2013 qua the petitioners shall remain stayed till further of the Court.

The above statement does not affect students who have passed & enrolled for IETE courses before 31st May 2013.

The last date of hearing of our case regarding recognitions of our courses from MHRD was 9th Jan 2014 in Hon'ble High Court of Delhi. The Hon'ble High Court has decided the interim orders to continue.

Issued by

Secretary General
The Institution of Electronics and Telecommunication Engineers (IETE)

Status in respect of recognitions granted for the examinations conducted by IETE.

A writ petition was filed by the Institution in Delhi High Court on 13 May 2013 for quashing the orders of MHRD dated 10 July 2012 and 06 Dec 2012 withdrawing the recognition in perpetuity for equivalence in Central Govt jobs after 31 May 2013. The writ petition came up for hearing on 17 May, 21 May and 23 May 2013.

The Hon'ble Delhi Court is pleased to stay the orders of the Ministry of Human Resource Development dated 06 Dec. 2012 with respect to the dead line of 31 May 2013 till the next date of hearing i.e. 06 Aug. 2013. However, the admissions, which are made, will be subject to final orders, which will be passed in the writ petition.

The matter has now been fixed for further hearing before the Delhi High Court on 06 Aug. 2013.

Issued by

Secretary General
The Institution of Electronics and Telecommunication Engineers (IETE)

Last Date for Enrolment for June exam is 28 February and for December exam is 31 August. Please submit your application preferably 15 days before these dates.

Form IETE-2

THE INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS (IETE)

2, Institutional Area, Lodhi Road, New Delhi-110 003
Phone: 011-43538858/41/55/56
Email: membership@iete.org

Signature of the candidate

A B
Size of photograph 3.5x3.5cm exact.
*Paste within the box ABCD.
*To be attested by the gazette Officer/ Corporate Member of IETE
C D

To,
The Secretary General, IETE
2, Institutional Area,
Lodhi Road, New Delhi-110 003

Sir

1. I wish to enroll myself as a Student Member of (Please tick √ the course opted by you carefully out of the following)

   AMIETE : Computer Science & Engineering (CS) ☐
   (Deegree level)

2. Name _____
   (In Capital Letters) (Name should be written as per High School Certificate)

3. Date of Birth _____ 4. Father's/Husband Name _____

5. Correspondence Address _____ 6. Permanent Address _____
   (In Capital Letter) (In Capital Letter)
   _____ _____
   _____ Dist _____ _____ Dist _____
   State _____ PIN _____ State _____ PIN _____

7. Phone No. (O)_____ (R)_____ Mobile _____

   Fax _____ Email _____

FOR OFFICE USE ONLY

1. Accepted
2. Withheld/ Rejected with reason
3. Remarks

Mem No. SG-

Student Member (AM) ET/CS/IT

Signature _____

8. Educational Qualifications

(Attach attested copies of certificates Age/ Qualification/ Training/ Study etc.)

Examination Passed	Subjects	Board/ University	Year of Passing	Initial of Proposer(s)
Class 10 with General Science and Maths				
10+2/ Intermediate (Physics and Maths)				
Diploma				
B.Sc / M.Sc/ BE / B.Tech				

9. I enclose herewith Bank Draft No ……..Dated ……..for Rs.6000/- Drawn on …… in favour of IETE, New Delhi.(Please see Sl No.10 of Instructions to applicants)

If you are using downloaded form, Please Send a **Photograph (3.5x3.5cms) and Separate Bank Drafts** in the name of IETE, Delhi.
*Rs.350/- - Cost of Regulation. Detailed Syllabus and Postage
*Rs.6000/- - Enrollment Fee

10. Certificate Practical Experience/Training/Study to be filled in by the Head of Dept/ Institution/ Organization (See Bylaw 17 Refer para 2, on page No 4 of the Regulation of DipIETE Examination) or (See Bylaw 15 / Bylaw 16 on page no.4 of the Regulation & Syllabi of AMIETE Examination). I/ We certify that …….. has been studying / working/ engaged ……(Write the field of his working/ study) since …….

Seal of Dept/ Org.

Signature & Date……..…….
Name ……..……
Designation …….

11. *PROPOSAR'S RECOMMENDATION (TO BE FILLED BY A CORPORATE MEMBER OF IETE ONLY) Having satisfied myself in respect of the applicant's qualification and experience, I recommend him/ her to the Council as being in every way a fit and proper person to be admitted as a STUDENT MEMBER of the Institution, in accordance with Byelaw 17 (for DipIETE) or Bylaw 15 / Bylaw 16 (for AMIETE).

Mem. No……. Signature & Date……..

Name of the Proposer……

DECLARATION BY THE CANDIDATE

I declare that the information given in this form is accurate to the best of my knowledge. Obligation duly signed is given on the Card enclosed.

Name of the Candidate…… Signature of the Candidate……
Date ……

IMPORTANT

1. The institution of Electronics & Telecommunication Engineers (IETE) neither recognizes nor accepts affiliations of any Private Coaching Institute/ College.
2. Membership form IETE-2 forms part of the Regulation & Syllabi of DIPIETE/AMIETE Examination
3. * In Case candidate is finding difficulty in getting his application proposed, he may send his application to HQ, IETE directly for necessary assistance.
4. Student member are advised to ensure that they do not accept the membership form (IETE-2) without the copy of the Regulation and syllabi of DIPIETE/ AMIETE Examination.
5. Fees once paid will neither be adjusted nor be refunded under any circumstances.

INSTRUCTIONS TO APPLICANTS (To be retained by the student)

(To be read in conjunction with Regulations & Syllabi for AMIETE Examination)

1. a) There are two streams available to a candidate for enrolment in DipIETE viz. Electronics & Telecommunication Engineering and Computer Science & Engineering. Applicant is required to write his enrolment option in Column 1.

b) There are three streams available to a candidate for enrolment in AMIETE viz. Electronics & Telecommunication Engineering, Computer Science & Engineering and Information Technology. Applicant is required to write his enrolment option in Column 1.

2. Applicants are advised to submit their forms duly filled in direct to the IETE HQ. IETE neither recognizes nor accepts affiliation of any private coaching institution. Col 10 if filled and certified by these institutions will not be accepted. Incomplete application form will be rejected.
3. One shall be allowed to appear in the DipIETE/ AMIETE Examination only after one's enrolment as a Student member with the Institution. Only those Student members who get enrolled on or before 28th February and 31st August will be allowed to appear in the next DipIETE/ AMIETE Examination, held in June and December respectively. Processing of application takes minimum 15 days, therefore to get enrolled, the application completed in all respect must reach IETE HQ well before 14th February for June examination and 14th August for December Examination. Time period for LAB practice examination is counted from the date of enrollment, therefore, students are advised not to wait for last dates but get enrolled as early as possible.
4. Candidates are advised to submit all documents such as Membership Form, Identity Card, IETE Membership Card, self addressed envelope duly filled in, Qualification Certificates, Mark Sheet, Date of Birth Certificate and Experience Certificate (attested copies are required to be submitted) along with, the declaration on the reverse of the Membership Card duly signed by the candidate to IETE HQ only.
5. Membership No. will be allotted by IETE HQ Office. Candidates are advised to leave these columns blank. Membership No will be mentioned while corresponding with IETE HQ.
6. Candidates are advised to paste their stamp size photograph and fill in other columns of the Identity Card and IETE Membership Card. The photographs pasted (not stapled) on the application and Membership Card should be attested by either a Corporate member of the Institution or a Gazetted Officer, with his membership No./ Stamp affixed on it. They must write their complete address with Pin Code No.
7. Membership number, Identity card, receipt of amount paid and examination form will be sent to the applicant within 8-10 weeks of receipt of the application in IETE HQ.
8. FEE FOR ENROLMENT

	Members in India (Rs)	Members Abroad (US $)
Admission Fee	200.00	40.00
Application Fee	200.00	40.00
Building-cum-Library Fee	1300.00	260.00
Composite Subscription (for 5 years)	2500.00	360.00
Lab Infrastructure Fee	600.00	100.00
Development Fee	500.00	100.00
Establishment Fee	700.00	100.00
Total	6000.00	1000.00
Enrolment Form submission Fee	250.00	

9. Once the candidate is enrolled, the enrolment fee will not be refunded under any circumstances.
10. All remittances shall be made by crossed Bank Draft, drawn in favour of "Secretary General, IETE, New Delhi".MONEY ORDER, CHEQUES, IPO or CASH WILL NOT BE ACCEPTED.

11. Any change in the mailing address should be notified immediately. This will help the Office to keep its database up-to-date, and mail important Circulars/Notices/Letters and Journals of Education at the correspondence address.
12. The IETE neither recognizes nor accepts affiliations of any private coaching institution.
13. The student membership will be valid for 10 consecutive examinations from the date of enrollment. Thereafter, the student members not completing their DIPIETE/ AMIETE Examination are to seek re-enrollment by remitting applicable amount before or immediately after the expiry of the membership period to continue their membership to enable them to appear in the remaining papers and complete DipIETE/ AMIETE. Any examination chance not availed by a student due to whatsoever reason will be counted within 10 examinations. No Notice for renewal of membership will be sent.
14. A student is required to complete DipIETE/ AMIETE Examination within 2 enrollment periods from the date of initial enrollment. The student will, therefore, be permitted to seek only one renewal of membership. Renewal is to be applied for before or immediately after the expiry of initial enrollment with continuity of enrollment maintained by the student. Missed chances will be counted towards total number of examinations and no relaxation in this regard will be permissible. If the request for renewal is made after the stipulated period of two enrollments, admission will be treated as a fresh enrollment and no benefit in terms of exemptions in respect of subject(s) passed or exempted during the earlier enrolment will be granted. Students must renew their membership in time. Otherwise they will not be allowed to appear in the DipIETE/ AMIETE examination.
15. All Legal cases concerning IETE HQ shall lie within jurisdiction of Delhi courts only.
16. Every Student member successfully completing Sections A&B subjects including lab examinations with project work, seminar and a course in Communication Skills & Technical Writing of AMIETE Examination as per regulations prescribed by the Council from time to time shall be eligible to become a Associate Member (AMIETE). On payment of requisite fee for membership, he/she will be awarded a certificate of having passed the AMIETE examination of the institution and shall then be eligible for transfer to the class of AMIETE. To pass AMIETE Examination, a student is required to score a minimum grade of “D” having a grade point of 4 for each subject and having an aggregate of 5 CGPA. However for Project, Seminar and lab examinations he/she should get a minimum grade of “C” having a grade point of 5.
17. First examination application form as per the stream opted by the student will be dispatched to him/her along with the identity card at the time of enrolment.

The Institution of Electronics and Telecommunication Engineers
2, Institutional area, Lodhi Road, New Delhi-110 003.

EXEMPTION APPLICATION FORM

Dear Sir/Madam,

1. I student membership No……Name……..of stream…….request you to grant me exemption based on my qualification in the following subject.

	Sub Code	Subject	Qualification based on which exemption asked from Univ./Institution should be mentioned correctly
(a)			
(b)			
(c)			
(d)			

(For more subjects, use photo copy of this from)

2. A DD of Rs…….bearing machine no…….……of …..……..…is enclosed herewith as exemption fee.

3. I am enclosing following documents (Photo-copies duly attested)

   (a) Final/Provisional certificate.
   (b) Marksheets of all semesters.
   (c) Copy of the syllabus of the course.(Marked on it subject code for which exemption of the subject is applied.
   (d) Any other document.

4. Email address :……..

5. Phone No……..

(Signature of Student)

Note :
1. Fee for exemption for AMIETE is Rs 800/- where as for DipIETE, it is Rs 700/-
2. This application is not to be clubbed with exam form.
3. Relevant sufficient syllabus matching upto 80% mentioning the Textbooks & Reference Books should be enclosed.