ROLL NO. _____

Code: CT76 Subject: MICROELECTRONICS AND VLSI DESIGN

ALCCS – NEW SCHEME

Time: 3 Hours **FEBRUARY 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Describe the VLSI design levels.

b. Why NMOS technology is preferred more than PMOS technology? What are the different operating regions of an MOS transistor?

c. List the different IC Technologies and Basic Fabrication Steps.

d. Explain different Wafer Exposure Systems in Lithography.

e. What are VHDL primary constructs and describe them briefly?

f. Draw and explain scan based techniques of an edge triggered D flip-flop.

g. Define FSM? Explain Moore FSM with neat sketch of its life cycle. **(7×4)**

Q.2 a. Explain Deal Grove's model mathematically and derive expression for long time oxidation and short oxidation. **(10)**

b. Compare thermal diffusion and ion-implantation. Explain Self Diffusion and Inter Diffusion process. **(8)**

Q.3 a. Derive general expression of the threshold voltage for MOS structure. **(8)**

b. Explain all critical design parameters should be considered in an inverter design. **(10)**

Q.4 a. Draw the block diagram of a general two-stage op-amp and explain the working operation of each block. **(10)**

b. Draw the BJT differential amplifier and explain its large signal analysis. **(8)**

Q.5 a. Design a 2-to-1 multiplexer and XOR gate using transmission gates. **(8)**

b. Design a Resistive Load Complex gate and CMOS Complex gate for following expression **(10)**

$$Z = \overline{A(D + E) + BC}$$

Q.6 a. Draw the schematic of 6T SRAM cell and explain its Read & Write operations. **(8)**

b. List and explain Standard VHDL data types & Extended VHDL data types. Also explain the difference between data flow model and behavioral model. **(10)**

Q.7 Explain the importance of scaling of MOS transistor dimensions. Explain the types of scaling and show the effects of parameters in full scaling. **(18)**