ROLL NO. _____

Code: CT12 Subject: COMPUTER ARCHITECTURE

ALCCS – NEW SCHEME

Time: 3 Hours **FEBRUARY 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. What are the objectives of computer architecture?

b. Draw a circuit diagram of 3×8 decoder using 2×4 decoder.

c. State the major characteristics of RISC.

d. State how different policies of writing into cache are implemented.

e. Distinguish between horizontal and vertical microinstruction.

f. What do you mean by Maskable and Non-maskable interrupt?

g. What are the requirements of Superscalar Processors? **(7×4)**

Q.2 a. Design a combinational circuit whose input is a four bit number and whose output is the 2's complement of the number. **(6)**

b. Multiply the following pairs of signed 2's complement numbers using Booth's algorithm:
Multiplicand = 110011 and Multiplier = 101100 **(6)**

c. A digital computer has a common bus system of 16 registers of 32 bits each. The bus is constructed with multiplexers.
(i) How many selection inputs are there in each multiplexer?
(ii) What size of multiplexers is needed?
(iii) How many multiplexers are there in the bus? **(2×3)**

Q.3 a. Explain the process called subroutine nesting. **(6)**

b. The content of the top of memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What is the content of PC, SP and top of stack:
(i) Before the call instruction is fetched from memory.
(ii) After the call instruction is executed.
(iii) After the return from subroutine. **(3×2)**

c. Explain the use of following registers:
(i) PC
(ii) MAR
(iii) IR
(iv) MDR **(6)**

Q.4 a. The 8-bit registers A, B, C & D are loaded with the value $(F2)_H$, $(FF)_H$, $(B9)_H$ and $(EA)_H$ respectively. Determine the register content after the execution of the following sequence of micro-operations sequentially.
(i) A←A + B, C←C + shl(D)
(ii) C←C ^ D, B←B + 1
(iii) A←A – C
(iv) A←shr(B) ⊕ cir(D) **(10)**

b. With the help of neat block diagram explain the function of a Microprogram Sequencer. **(8)**

Q.5 a. What is Associative Memory? With the help of block diagram explain its hardware organization and its working. **(7)**

b. A block-set-associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 each consisting of 128 words.
(i) How many bits are there in main memory address?
(ii) How many bits are there in each of the TAG, SET and WORD fields? **(6)**

c. What is Cache memory? How is the performance of Cache memory measured? **(5)**

Q.6 a. What are the main advantages of using Input / Output interface? Why interfacing is used in digital computers? **(9)**

b. What do you mean by initialization of DMA controller? With the help of block diagram, explain DMA transfer. **(9)**

Q.7 a. Consider the multiplication of two 40 X 40 matrices using a vector processor.
(i) How many product terms are there in each inner product and how many inner products must be evaluated?
(ii) How many multiply-add operations are needed to calculate the product matrix? **(6)**

b. Give Flynn's classification of parallel computer architecture. With the help of diagram discuss each class in brief. Also give Feng's classification of Parallel Computer Architecture. **(2+6+4)**