ROLL NO. _____

Code: CS12 **Subject: COMPUTER ARCHITECTURE**

ALCCS – OLD SCHEME

Time: 3 Hours **FEBRUARY 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Define 'speed up' of a K-stage linear pipeline processor.

b. What is locality of reference? Where this concept is used?

c. Explain the term physical address and virtual address.

d. What is cycle stealing DMA transfer?

e. Define the terms: Seek time and Latency time of a hard disk.

f. What is "throughput" of a computer system? How are they measured?

g. What are the implications of Moore's Law in the development of computer technology? **(7×4)**

Q.2 a. Explain BCD addition and subtraction with suitable example. Also draw the circuit for the same. **(9)**

b. Construct a 16 to 1 line multiplexer with two 8 to 1 line multiplexer and one 2 to 1 line multiplexer. Give the truth table for the same. **(5)**

c. Draw the flowchart for Booth's multiplication process. **(4)**

Q.3 a. What is Assembler? Discuss step by step working of a assembler to generate binary code of a program. **(9)**

b. Give the Register Transfer Level (RTL) statements for Push & Pop operation. Explain how a subroutine is executed. How a subroutine is different from program interrupt? **(9)**

Q.4 a. What is micro-instruction? With suitable block diagram, explain the working of a micro programmed sequencer. **(9)**

b. Discuss the design steps for designing a hardware control unit. What is the advantage of hardware control unit over micro programmed control unit? **(9)**

Q.5 a. Explain instruction cycle. Give the RTL statement for each sub cycle. How the instruction cycle is to accommodate the interrupt from I/O devices? **(9)**

b. Give the classification of instructions of a micro processor. Which types of instructions makes use of flag register? **(9)**

Q.6 a. Explain how cache memory is different from virtual memory. Also discuss various page replacement policies for virtual memory using suitable examples. **(9)**

b. What is software polling and hardware polling? Explain. **(5)**

c. Discuss the features of synchronous and asynchronous data transfer schemes. **(4)**

Q.7 a. With neat flow chart, explain non-restoring division algorithm. **(9)**

b. Design a parallel priority interrupt hardware for a system with eight interrupt sources. **(9)**