ROLL NO. _____

Code: CT12 Subject: COMPUTER ARCHITECTURE

ALCCS – NEW SCHEME

Time: 3 Hours **FEBRUARY 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Give the Truth Table and draw the logic diagram of a full adder.

b. What are zero-address instructions? Explain with the help of an example.

c. Classify micro operations and give an example for each.

d. A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K x 32. Find the following:
(i) Formulate all relevant information required to construct the cache memory.
(ii) What is the size of cache memory?

e. Compare the three modes of data transfer- Programmed I/O, Interrupted Control I/O and DMA.

f. Mention similarities and dissimilarities of RISC and CISC Machines.

g. Perform $(-12)_{10} + (5)_{10}$ using 2's complement form. Use 8-bits to represent numbers in binary. **(7×4)**

Q.2 a. Differentiate between computer organization, computer design and computer architecture. **(6)**

b. Represent decimal number 8620 in
(i) BCD (ii) Excess-3 code
(iii) 2421 code (iv) Binary number **(6)**

c. With the help of examples, differentiate between combinational and sequential circuits. **(6)**

Q.3 a. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? **(3+3)**

b. Explain sequence of steps followed in first pass and second pass assembler. **(6)**

c. Explain floating point representation. Represent the number $(+46.5)_{10}$ as a floating-point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits. **(3+3)**

Q.4 a. Explain the significance of RTL in the implementation of digital systems. **(6)**

b. Compare hardwired and micro programmed control design. Give their respective advantages and disadvantages. Give the formats of horizontal and vertical microinstructions. **(6)**

c. A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.
(i) Formulate a control word for a microoperation.
(ii) Specify the number of bits in each field of the control word and give a general coding scheme.
(iii) Show the control word that specify the microoperation R4 $\leftarrow$ R5 + R6. **(6)**

Q.5 a. Explain multiple-module memory interleaving with a block diagram. **(6)**

b. Explain serial and parallel data communication. **(6)**

c. A Virtual memory has an address space of 8K words, a memory space of 4K words and page sizes of 1K words. The following page reference changes occur during a given time interval.

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (i) FIFO (ii) LRU. **(6)**

Q.6 a. Compare and contrast the superscalar architecture to the VLIW architecture. **(6)**

b. Explain delay in pipeline execution. A non-pipeline system takes 50ns to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10ns. Determine speed-up-ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? **(3+3)**

c. Classify parallel computers and give its comparison. **(6)**

Q.7 a. Write short notes for the following:
(i) Vector computers and array processors
(ii) RS 232C specifications and applications
(iii) Micro Sequencer design **(3 $\times$ 3)**

b. Compare associative, set-associative and direct mapping procedures. **(9)**