ROLL NO. _____

Code: CS12 **Subject: COMPUTER ARCHITECTURE**

ALCCS – OLD SCHEME

Time: 3 Hours **FEBRUARY 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Realise the logic circuit by using NOR gate for the function $F(A, B, C, D) = \sum(0,1,2,5,8,9)$.

b. Explain the working of DMA.

c. Give the micro instruction code format and explain the use of condition field.

d. What is meant by Program Control Instructions? Give an example.

e. State the use of associative memory page table.

f. Discuss in brief serial data transfer.

g. Compare RISC and CISC characteristics. **(7 × 4)**

Q.2 a. With neat block diagram of a bi-directional shift register with parallel load, explain the working of the register. **(9)**

b. Draw the flow chart for three digit decimal addition. Give the block diagram representation of three ways to do the addition. **(9)**

Q.3 a. A two word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction stored at location (W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolised by Z. An index register contains the value X, state how Z is calculated from the other addresses if the addressing mode of the instruction is:

(i) Direct (ii) Indirect
(iii) Relative (iv) Indexed **(9)**

b. With neat flow chart explain the working of an assembler during first pass and second pass. **(9)**

Q.4 a. Give the block diagram of the control unit in basic computer and explain its operations. **(9)**

b. What is microprogram sequencer? Give its block diagram and explain its operation. **(9)**

Q.5 a. Explain Interrupt acknowledgement cycle. Mention various types of interrupts. **(9)**

b. Explain one-address, two address and three address instructions. Give an example for each. **(9)**

Q.6 a. Discuss various methods used for address mapping in virtual memory. **(9)**

b. A virtual memory system has a page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries:

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses in decimal that will cause a page fault if used by CPU. **(5)**

c. Explain page replacement policies used for virtual memory system. **(4)**

Q.7 a. Explain the asynchronous data transfer scheme using strobe control signal. Give its features. **(5)**

b. Give the circuit diagram of 4×4 (FIFO) buffer and explain its working. **(9)**

c. Compare I/O mapped and memory mapped I/O. **(4)**