Code: CT76   Subject: MICROELECTRONICS AND VLSI DESIGN

ALCCS – NEW SCHEME

Time: 3 Hours   **AUGUST 2013**   **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:
- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. Write the advantages of monolithic integration of a large number of functions on a single chip usually provides.

   b. Compare CMOS with BJT.

   c. Explain the purpose of SiO_2 layer formation in MOS transistor and list the different techniques of SiO_2 layer formation.

   d. What are Photo-resists? What are its types and Give examples of each?

   e. What is Channel-length modulation? Why latch-up problem occurs in MOS device?

   f. Define Entity Declaration. Explain different port-modes used in VHDL.

   g. Compare Mealy and Moore FSM's.   **(7×4)**

Q.2 a. How a substrate is prepared for fabricating on IC? Explain CZ process.   **(10)**

   b. Define Diffusion Process. Explain Fick's first diffusion law.   **(8)**

Q.3 a. Calculate the expression for depletion width of an MOS transistor subjected for an external bias.   **(10)**

   b. Explain the effect of V_{SB} voltage on MOS transistor threshold voltage.   **(8)**

Q.4 a. Explain CMOS inverter and give its DC characteristics.   **(10)**

   b. Give a logic circuit example in which stuck-at-'1' fault and stuck-at-'0' fault are distinguishable.   **(8)**

Q.5 a. Design a Full CMOS XOR gate and explain its working operation.   **(8)**

   b. Explain Transmission Gate working operations in different regions.   **(10)**

Q.6 a. Classify Semiconductor Memories according to the type of data storage and type of data access mechanisms. **(10)**

   b. Draw and explain the behavioral model of positive edge triggered T flip-flop. **(8)**

Q.7 a. Explain the capacitances associated with MOSFET. **(10)**

   b. Write short notes on **(8)**

   (i) Scaling of MOS Transistor dimension.
   (ii) Trends in VLSI Technology.