ROLL NO. _____

Code: CT12 Subject: COMPUTER ARCHITECTURE

ALCCS – NEW SCHEME

Time: 3 Hours **AUGUST 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. What do you mean by self complimenting BCD code? Give an example of it.

b. What is macro? How is it different from subroutine?

c. What is stack memory? State its advantages.

d. What is biased exponent? Why is it preferred over normal exponent?

e. What is the use of micro-sequencer?

f. How cache memory helps in improving system performance?

g. Compare DMA based data transfer with program control data transfer. **(7×4)**

Q.2 a. What is cache coherence? How can the problem be resolved with a snoopy cache controller? **(9)**

b. What are the pipeline conflicts? How are they handled? **(9)**

Q.3 a. Discuss RS 232-C standard. State the advantage of USB (Universal Serial Bus) over RS 232-C bus. **(9)**

b. Show the layout of a cache for a CPU that can address $1M \times 16$ of memory. The cache hold $8K \times 16$ of data and have following mapping strategies. Give the number of bits per location and the total number of locations.
(i) Fully associative.
(ii) Directed mapped.
(iii) Four way set-associative. **(9)**

Q.4 a. With a neat block diagram, explain the working principle of a micro-sequencer. State design methods and their limitations. **(9)**

b. Design a common bus system which can implement the following RTL code using tristate buffers. **(9)**

(i) $A \leftarrow H$

(ii) $A \leftarrow H+1, M \leftarrow B$

(iii) $M \leftarrow L-1, A \leftarrow A \wedge B$

(iv) $M \leftarrow \overline{A}+1$

Q.5 a. With flow chart, explain the working of a 2-pass assembler. **(9)**

b. Show the code to perform the computation $X = A + (B * C) + D$ using three, two, one operand instructions. **(9)**

Q.6 a. Design a 4-bit carry look ahead adder and explain how it is faster than 4 bit binary adder. **(9)**

b. Design a BCD subtractor circuit and explain the operation. **(9)**

Q.7 a. Discuss the characteristic features of RISC and CISC processor. State the situations in which RISC and CISC processors are preferable. **(9)**

b. Starting from an initial value of R = 10011101, determine the sequence of binary values in R after logical shift left, followed by a circular shift-right followed by a logical shift right and a circular shift left. **(5)**

c. State the ways to measure the performance of a computer. **(4)**