Q.1

(a) What is on an Integrated Circuit?

Answer:

Actually only two types of things:
– Conducting layers which form the wires on the IC.
• There are many layers of wires (used to have 1 layer of metal, now advanced processes have 4-5 metal layers). Wires have electrical properties like resistance and capacitance.
• (Requires insulators and contacts between layers.)
– Transistors (the free things that fit under the wires).
• There are a few kinds of transistors. These transistors can be thought of as a voltage controlled switch. The voltage on one terminal of the transistor determines whether the other two terminals are connected or not.

(b) Compare CMOS & Bipolar Technologies.

Answer:

CMOS Technology	Bipolar technology
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance (high drive current)
• Scalable threshold voltage	
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load (fan-out limitations)	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low g_m ($g_m \alpha V_{in}$)	• High g_m ($g_m \alpha e^{Vin}$)
	• High f_t at low current
• Bidirectional capability	• Essentially unidirectional
• A near ideal switching device	

(c) What is Body Effect and Channel Length modulation in MOS transistor?

Answer:

The threshold voltage V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

Channel Length Modulation: The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied V_{DS}, increasing V_{DS} causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

(d) What are major uses of SiO2? What are the different formation techniques of SiO2?

Answer:

Major uses of SiO2:
1. Mask against implant or diffusion of dopant into Si
2. Isolation of Devices
3. Gate oxide
4. Inter-Level Dielectric (ILD) in multilevel metallization

Formation Techniques of SiO2:
1. Thermal oxidation
2. Wet anodization
3. Chemical Vapor deposition (CVD)
4. Plasma anodization or oxidation.

(e) What are two components of Power dissipation? Also give some of the important CAD tools.

Answer:

There are two components that establish the amount of power dissipated in a CMOS circuit. These are:

i)Static dissipation due to leakage current or other current drawn continuously from the power supply.
ii) Dynamic dissipation due to
- Switching transient current
- Charging and discharging of load capacitances.

Some of the important CAD tools are:

i) Layout editors
ii) Design Rule checkers (DRC)
iii) Circuit extraction.

(f) Compare Traditional vs. Hardware Description Languages.

Answer:

- Procedural programming languages provide the *how* or recipes
  - for computation
  - for data manipulation
  - for execution on a specific hardware model
- Hardware description languages describe a system
  - Systems can be described from many different points of view
    - Behavior: what does it do?
    - Structure: what is it composed of?
    - Functional properties: how do I interface to it?
    - Physical properties: how fast is it?

(g) What is the test access port and what are the contents of the test architecture?

Answer:

The Test Access Port (TAP) is a definition of the interface that needs to be included in an IC to make it capable of being included in boundary-scan architecture. The port has four or five single bit connections, as follows:

- TCK(The Test Clock Input)
- TMS(The Test Mode Select)
- TDI(The Test Data Input)
- TDO(The Test Data Output)

It also has an optional signal

- TRST*(The Test Reset Signal)

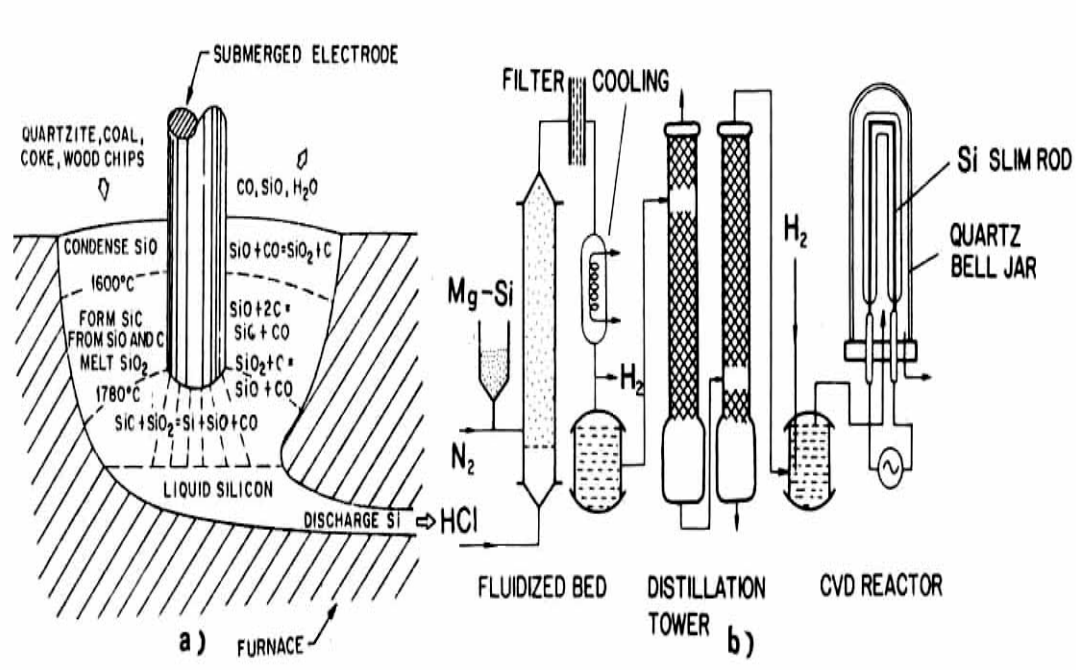
The test architecture consists of:

- The TAP interface pins
- A set of test-data registers
- An instruction register
- A TAP controller

Q.2

a. Explain Purification and Preparation of Electronic Grade Semiconductor.

Answer: MGS⇒ EGS⇒ Si Crystal



(a) Schematic of submerged-electrode arc furnace for production of MGS. Reprinted with permission of the publisher, the Electrochemical Society. (b) Schematic of fluidized bed, distillation tower, and CVD reactor developed by Siemens.

b. Explain diffusion concepts. Define error function solution in an Infinite Medium.

Answer:

• Diffusion is the redistribution of atoms from regions of high concentration of mobile species to regions of low concentration. It occurs at all temperatures, but the diffusivity has an exponential dependence on T.

• Predeposition: doping often proceeds by an initial predep step to introduce the required dose of dopant into the substrate.

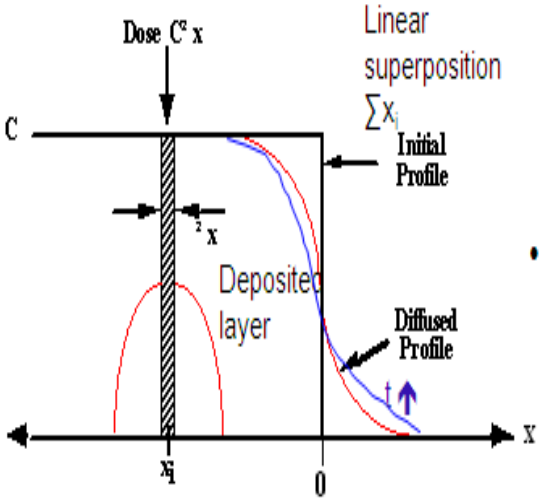
• Drive-In: a subsequent drive-in anneal then redistributes the dopant giving the required x_J and surface concentration.

Error Function Solution in an Infinite Medium

3. Infinite Source (unlimited supply):

$C = 0$ at $t = 0$ for $x > 0$

$C = C$ at $t = 0$ for $x < 0$



• The infinite source is made up of small slices each diffusing as a Gaussian.

$$C(x,t) = \lim_{\Delta x \to 0} \frac{C_s}{2\sqrt{\pi D t}} \sum_{i=1}^{n} \Delta x_i \exp - \frac{(x - x_i)^2}{4Dt}$$

• The solution which satisfies Fick's second law is

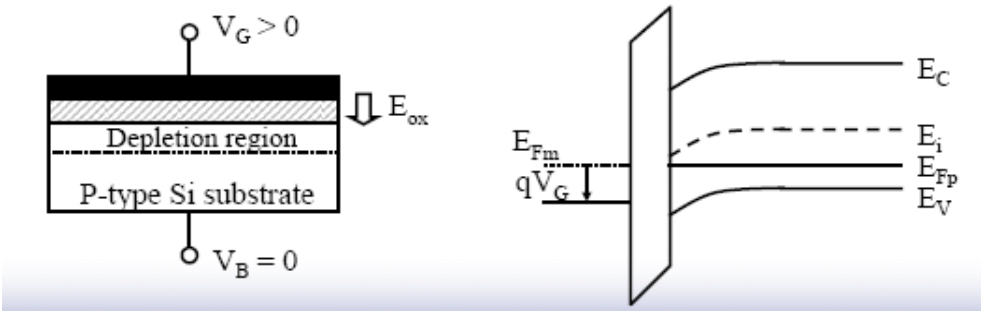
$$C(x,t) = \frac{C}{2}\left[1 - erf\left(\frac{x}{2\sqrt{Dt}}\right)\right] = C_s\left[erfc\left(\frac{x}{2\sqrt{Dt}}\right)\right]$$

$$1 - erf\left(\frac{x}{2\sqrt{Dt}}\right) = erfc\left(\frac{x}{2\sqrt{Dt}}\right)$$ Complementary error function

Q.3

a. Calculate the expression for depletion width of an MOS transistor subjected for an external bias.

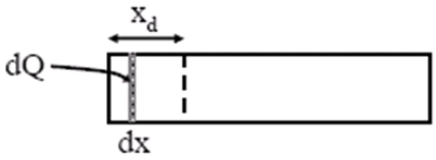
Answer:



(VG > 0) : small positive voltage is applied on gate wrt bulk. Positive voltage pushes holes back to bulk. Near surface hole concentration decreases. Holes leave acceptor ions behind and region near the surface becomes free of mobile carriers. This is called depletion region. Downward band bending takes place because of increase in surface potential.

- Find charge dQ in small slice of depletion area

$$dQ = -qN_A dx$$



- Find change in surface potential to displace dQ by distance x_d (Poisson equation):

$$d\phi = -x\frac{dQ}{\varepsilon_{Si}} \qquad d\phi = xqN_A\frac{dx}{\varepsilon_{Si}}$$

- Integrate perpendicular to surface

$$\int_{\phi_F}^{\phi_S} d\phi_S = \int_0^{x_d} \frac{qN_A x}{2\varepsilon_{Si}} dx$$

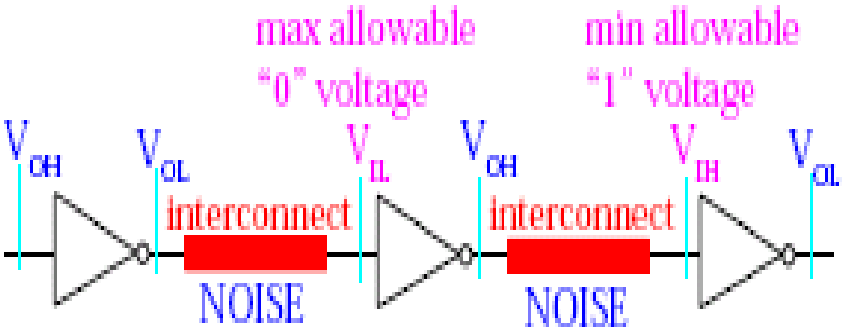
$$\phi_S - \phi_F = \frac{qN_A x_d^2}{2\varepsilon_{Si}}$$

- Result:

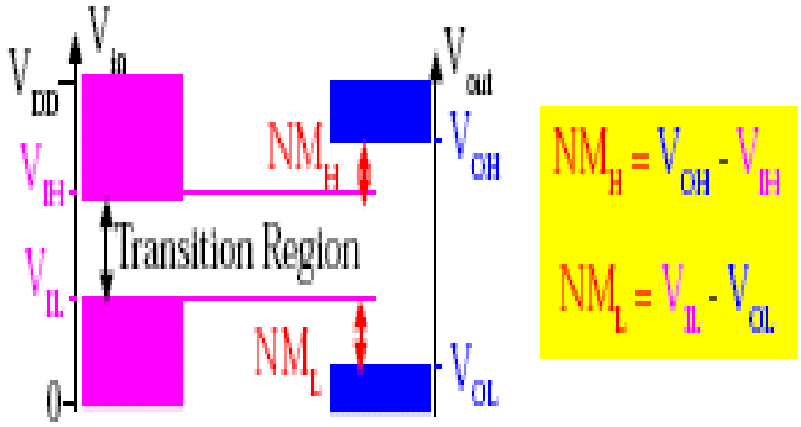
$$x_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_S - \phi_F|}{qN_A}}$$

b. Explain the Noise Immunity and Noise Margins in static CMOS inverter.

Answer:



Output signal is transmitted through interconnect to next inverter.
Interconnects are prone to noise. Suppose output of 1st inverter is perturbed, and its level is higher than VIL than it can not be correctly predicted at output of 2nd inverter.
Thus VIL is max allowable input voltage which is low enough to ensure '1' output.
Similarly VIH is minimum allowable input voltage which is high enough to ensure '0' output.



• Noise tolerance also called Noise Margins and denoted by N_M. Two noise margins will be defined : for low signal level as N_{ML} and high signal level as N_{MH} as

Q.4

a. Draw the block diagram of a general two-stage op-amp and explain the working operation of each block.

Answer:

Block diagram of a general, two-stage op amp:

Differential trans-conductance stage:

Forms the input and sometimes provides the differential-to single ended conversion. This stage improves noise and offset performance.

High gain stage:

Provides the voltage gain required by the op amp together with the input stage.

Output buffer:

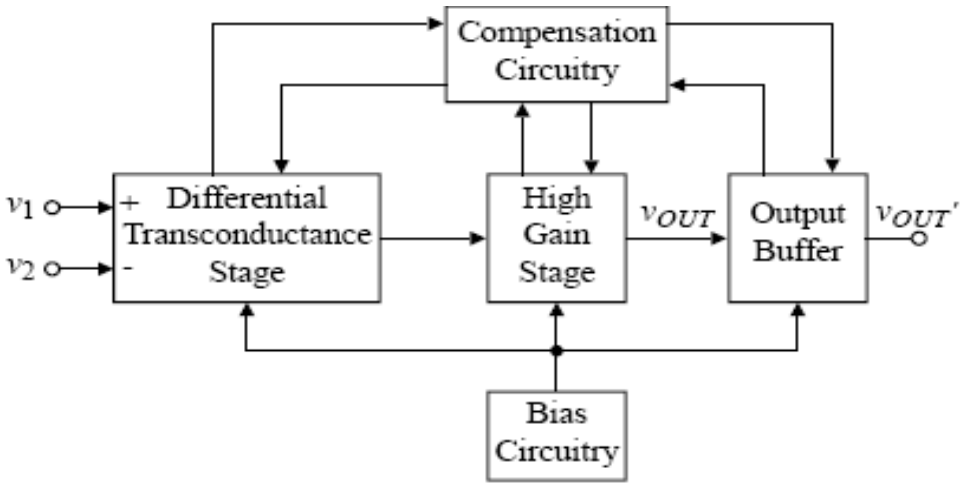
Used if the op amp must drive a low resistance bcoz objective of buffer is to lower the output resistance and maintain large signal swing.

Compensation:

Necessary to keep the op amp stable when resistive negative feedback is applied.

Bias Circuit:

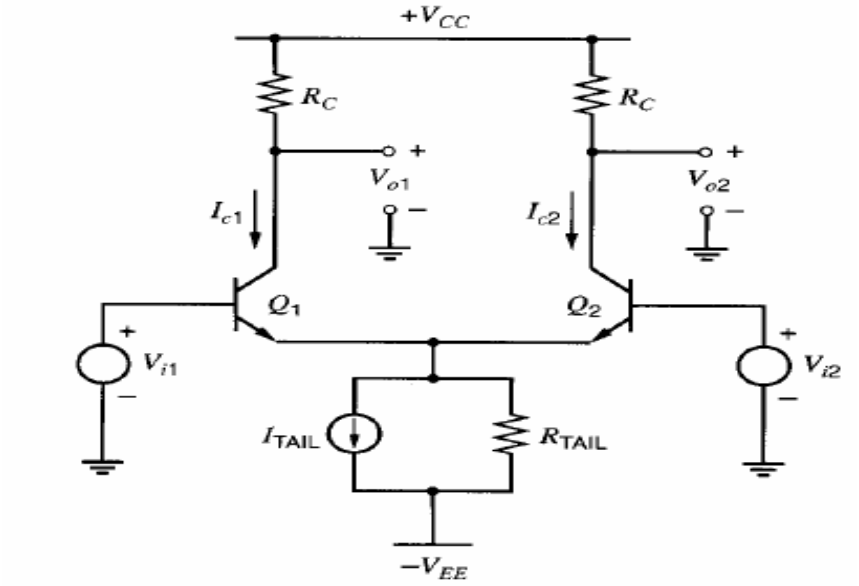
To provide proper operating point.



b. Draw the dc transfer characteristic of an Emitter – Coupled pair of BJT and explain.

Answer:

The biasing circuit in the lead connected to the emitters of Q_1 and Q_2 can be a transistor current source, which is called a tail current source, or a simple resistor.



The large-signal behavior of the emitter-coupled pair is important in part because it illustrates the limited range of input voltages over which the circuit behaves almost linearly.

For simplicity in the analysis, we assume that the output resistance of the tail current source $R_{Tail} \rightarrow \infty$,that the output resistance of each transistor $r_o \rightarrow \infty$ and that the base resistance of each transistor $r_b = 0$.

From KVL around the input loop,

$$V_{i1} - V_{be1} + V_{be2} - V_{i2} = 0$$

Assume the collector resistors are small enough that the transistors do not operate in saturation if $V_{il} \leq V_{cc}$ and $V_{i2} \leq V_{cc}$. If $Vb_{el} >> V_T$ and $V_{be2} >> V_T$, the Ebers-Moll equations show that

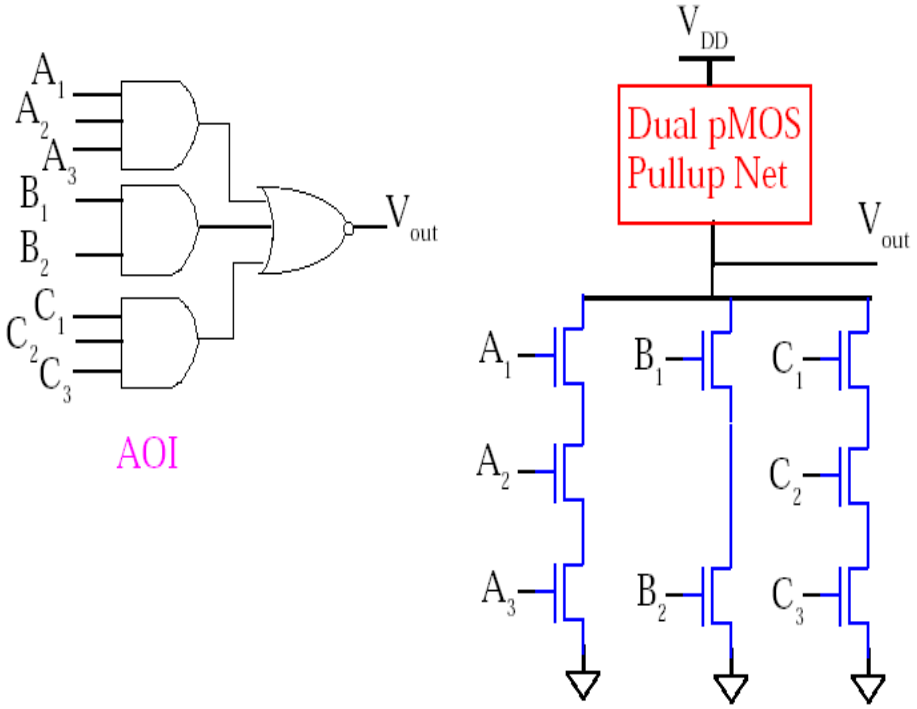
$$V_{be1} = V_T \ln \frac{I_{c1}}{I_{S1}}$$

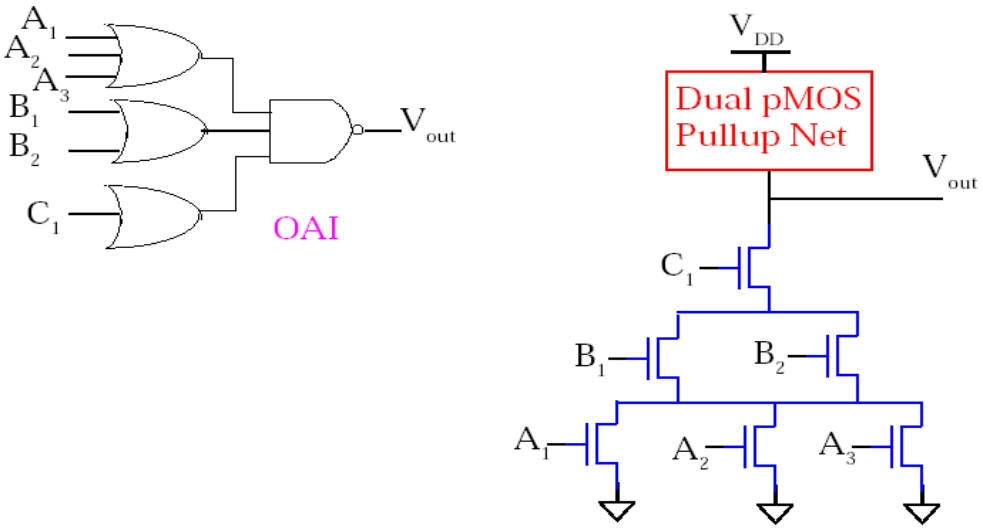
$$V_{be2} = V_T \ln \frac{I_{c2}}{I_{S2}}$$

Q.5

a. Design and Explain AOI and OAI combinational gates with example.

Answer:

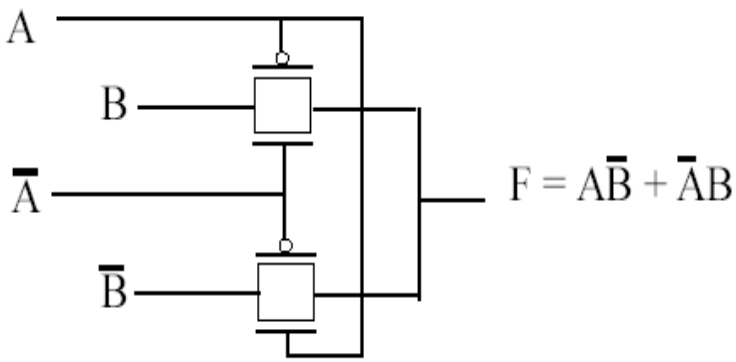




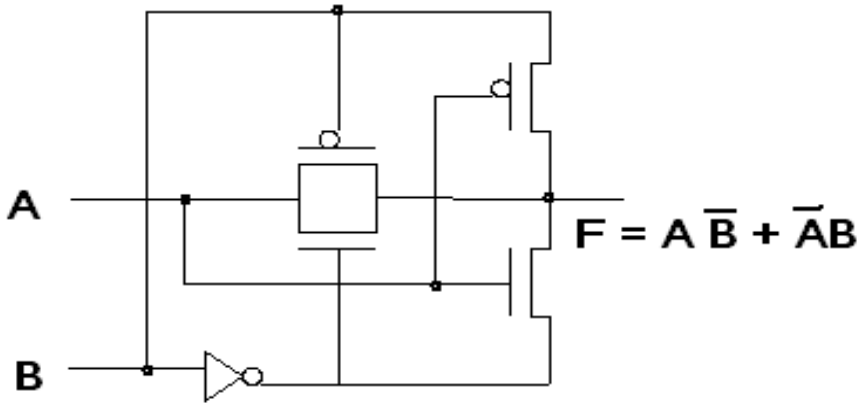
b. Design XOR gate using 8T & 6T Transmission Gate.

Answer:

8-transistor based XOR GATE:



6-transistor based XOR GATE:



Q.6

a. Classify Semiconductor Memories according to the type of data storage and type of data access mechanisms.

Answer:

Semiconductor Memories are classified according to the **type of data storage** and the **type of data access** mechanism into the following two main groups:

• Non-volatile Memory (NVM) also known as Read-Only Memory (ROM) which retains information when the power supply voltage is off. With respect to the data storage mechanism NVM are divided into the following groups:

1. Mask programmed ROM. The required contents of the memory is programmed during fabrication,

2. Programmable ROM (PROM). The required contents are written in a permanent way by burning out internal interconnections (fuses). It is a one-off procedure.

3. Erasable PROM (EPROM). Data is stored as a charge on an isolated gate capacitor ("floating gate"). Data is removed by exposing the PROM to the ultraviolet light.
4. Electrically Erasable PROM (EEPROM) also known as Flash Memory. It is also base on the concept of the floating gate. The contents can be re-programmed by applying suitable voltages to the EEPROM pins. The Flash Memories are very important data storage devices for mobile applications.

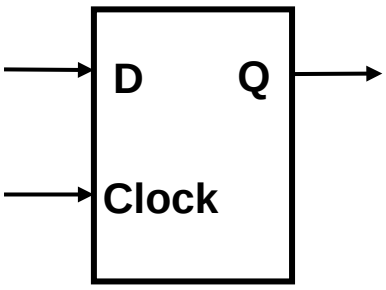
- Read/Write (R/W) memory, also known as Random Access Memory (RAM). From the point of view of the data storage mechanism RAM are divided into two main groups:

1. Static RAM, where data is retained as long as there is power supply on.

2. Dynamic RAM, where data is stored on capacitors and requires periodic refreshment.

b. Write a VHDL code to describe D-Latch with clock enabled.?

Answer:




```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
```

```
ENTITY latch IS
    PORT (      D, Clock      : IN    STD_LOGIC ;
                Q       : OUT STD_LOGIC) ;
END latch ;

ARCHITECTURE Behavior OF latch IS
BEGIN
    PROCESS ( D, Clock )
    BEGIN
        IF Clock = '1' THEN
            Q <= D ;
        END IF ;
    END PROCESS ;
END Behavior;
```

Q.7

Explain the importance of scaling of MOS transistor dimensions. Explain the types of scaling and show the effects of parameters in constant voltage scaling.

Answer:

Importance of Scaling

- Circuit designers can not control threshold Voltage and process parameters.
- They only control the width, length, and connection scheme of the transistors of a particular process.
- Since designer cannot change V_T, he/she has to understand how W and L affect V_T and thus a circuit's performance.
- Hand calculation only gives rough estimation. Thus when SPICE simulation and hand calculations do not match, short channel and other effects come into picture and a designer should know how they are affecting the performance before designing the circuit.

TWO TYPES OF SCALING

- Constant field or full scaling.
  - Tries to maintain the same electric filed distribution in the scaled device.
  - Not always possible (The transistors still have to be able to interface with the outside world.)
- Constant voltage scaling.
  - VDD, VT are unchanged.
  - Power dissipation and density go up.

To describe scaling, a scaling factor S>1 is introduced.

Constant Voltage Scaling :

- Power supply and terminal voltages are kept constant, while all the process dimensions are scaled by (1/S).
- Doping densities are increased by a factor of S^2 to keep charge-field relationship preserve.

Quantity	Befor scaling	After scaling
Oxide capacitance	C_{ox}	$C_{ox}' = Cox\ S$
Drain Current	I_d	$I_d'=I_d\ S$
Power Dissipation	P	P'=P. S
Power Density	P/Area	$P'/Area' = S^3$. P/Area
Dimensions	W, L, Tox, xj.	Down by S
Voltages	Vdd, Vt	Unchanged
Doping Densities	NA, ND	Up by S^2

Text Books

1. Kang S. M. and lablebici, Y. "CMOS Digital Integrated Circuit: Analysis and Design", Mc Graw Hill, 1996.

2. S. M. Sze, "Semiconductor Devices", 2nd Edition, John Wiley & Sons, 2002.