Q.1 a. What are the characteristics of a RISC processor?

Answer: Page no 284 – 285 of Text Book 1

b. State the purpose of Micro program Sequencer.

Answer: Page no 235 of Text Book 1

c. What is Burst mode DMA transfer?

Answer: Page no 418 of Text Book 1

d. What are Vectored and Non vectored interrupts?

Answer: Page no 408 of Text Book 1

e. What is stack memory? State the application of it.

Answer: Page no 251 of Text Book 1

f. What is arithmetic shift operation? Explain with an example.

Answer: Page no 199 of Text Book 1

g. How LRU replacement policy is implemented in cache memory?

Answer: Page no 469-470 of Text Book 1

Q.2 b. Give the flow chart for BCD multiplication and give the data flow for multiplication of 32 with 18 in BCD.

Answer: Page no 370 of Text Book 1

Q.3 a. Discuss the steps followed in 2-pass Assembler with flow chart.

Answer: Page no 191 of Text Book 1

b. Design the control unit for a CPU which can execute following:-

Instruction	Instruction Code	Operation
INCOR	00 AAAAAA	AC ← (AC+1) V M[AAAAAA]
DADD	01 AAAAAA	AC ← AC+M[AAAAAA]+M[AAAAAA+1]
SKIP AND	11 AAAAAA	AC ← AC^M[AAAAAA], PC ← PC+1

Answer: Page no 233 of Text Book 1

Q.4 a. What is Micro programmed Control Unit? Explain different methods for designing of Micro programmed Control Unit.

Answer: Page no 216 of Text Book 1

b. What are the different sources of interrupts? List different types of interrupts and explain how priority is decided in Daisy Chaining method.

Answer: Page no 153 & 409 of Text Book 1

Q.5 a. Design an Associative Memory of m word, n cells per word. Derive the match logic for each word stored in the memory. Draw the internal organization of a typical cell of Associative Memory.

Answer: Page no 458 of Text Book 1

b. Consider the following page address generated by a two level cache memory that used demand paging and has a cache capacity of four pages.
1, 6, 4, 5, 1, 4, 3, 2, 1, 2, 1, 4, 6, 7, 4, 1, 3, 1, 7
Assume that the cache was initially has the page 1, 2, 3 & 4 in it. Which page replacement policy is more suitable and why?

Answer: Page no 464-471 of Text Book 1
(Least Recently used in better)

Q.6 a. What is pipeline conflicts? How are they managed?

Answer: Page no 315 of Text Book 1

b. What is parallel processing? Differentiate four types of parallel processing techniques with suitable diagrams.

Answer: Page no 301 of Text Book 1

Q.7 Write note on the following:-
(i) Wallace Tree Multiplier.
(ii) Serial and parallel data communication.

Answer: (i) Page no 355 of Text Book 2
(ii) Page no 431 of Text Book.

Text Books

1. Morris Mano - Computer System Architecture - PHI, Eastern Economy Edition - 2001.

2. John D. Carpinelli - Computer Systems Organization and Architecture - Pearson Education Asia - 1st Edition.