Q.2   **a.**   **Explain the main characteristics of an embedded system. Define the main design technology.**   **(8)**

Answer:

> characteristics of embedded systems.
- Single functioned: executes single program repeatedly.
- Tightly constrained: low cost, low power, small and fast.
- Reactive and real time: continuously reacts to change in system environment and computes certain results without delay.

> Txt Book-1, Page No: 16

     b.   **Explain the design matrix for embedded systems.**   **(8)**

Answer: **Refer Page 4 of Text Book-I**

Q.3   **a.**   **Explain the following:**   **(8)**
             (i) Combinational and sequential circuits
             (ii) Function of Single purpose processors

Answer:

a(i). - The output of sequential logic circuits not only depends on current inputs but also on past sequence of inputs. The sequential circuits are constructed using combinational logic and a no. of memory elements with some or all of memory o/ps fed back into the combinational logic forming a feedback path or loop.
- A very simple sequential circuit with no inputs created using inverters to form a feedback loop.
sequential circuit = combinational logic + Memory elements.
- A state variable in sequential circuit represents the single bit-variable stored in a memory element in circuit.
- Each memory element maybe state 0 or state 1 depending on the current value stored in the memory element.

a(ii) Page No: 10, txt Book-1

     b.   **Explain with the help of figure RT level Single purpose processor design.**   **(8)**

Answer: **Refer pages 44-45 of Text book - I**
Q.4   **a.**   **Explain with the help of block diagram processor architecture in detail.**   **(8)**

Answer:

The processor architecture provides many functions in a single package. The architecture of 8051 includes

- 8 bit ALU, Accumulator, 8 bit register and 8 bit data bus.
- Boolean processor
- multiply / divide and compare instructions
- 4 register banks
- fast interrupt with register bank switching
- Interrupts into selectable priority.
- Dual 16 bit address bus
- on chip RAM – 128 bytes & on chip ROM – 4kB

Block diagram of 8051

Block diagram of 8051
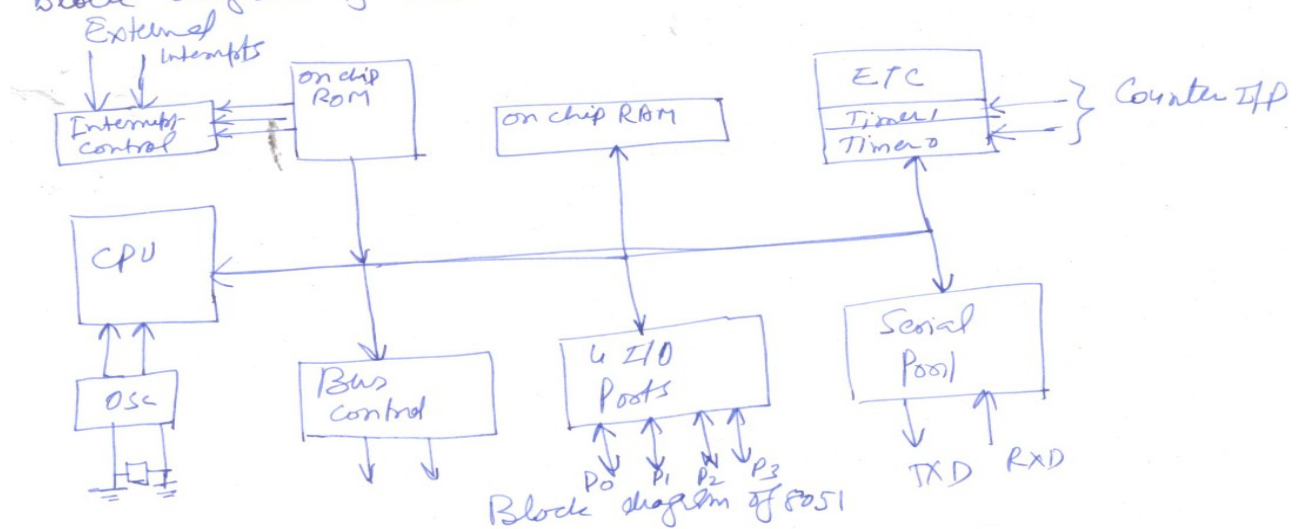
    b. Write selection criterion of microcontroller.   **(8)**

Answer:

Selection criterion of microcontroller
→ Memory Requirement / Amount of RAM / ROM on chip
→ No. of bits required / No of I/P
→ Speed
→ Power consumption
→ Cost per unit
→ Availability of development tools
→ Availability of needed quantity and future requirement.

    Q.5 a. What are LCD controllers?   **(8)**

Answer:

LCD controller:-

These LCD screen are limited to mochrone text and are often used in copiers, fax machines, laser printers, industrial test equipments networking equipment such as routers and storage devices. The screen comes in a small sizes with standard configurations. common sizes are 8x1, 16x2, 20x2 and 20x4. Larger sizes are made with 32, 40 and 80 characters with 1, 2, 4 or 8 lines. The most commonly manufactured larger configuration is 40x4 characters, which requires two individually addresseble to 80 characters. A common smaller size is 16x2 and the issue is readily available as surplus stocks for prototyping work.

Character LCD can come with or without backlight, which may be LED, fluorescent or electroluminescent. It has following pins
Ground, Vcc (+3.3V to 5V) Contrast adjustment, register select, RD/WR, clock enable Bit 0, Bit 1, Bit 2, Bit 3, Bit 4, Bit 5, Bit 6, Bit 7, backlight Anode, backlight Cathode. The nominal operating voltage for LED backlight is 5V at full brightness, with dimming at lower voltages dependent on the details such as color

b. Discuss the main features of times, counters and watch dog timers. **(8)**

Answer:

Timers: Measurement of time intervals
   - To generate timed output events eg hold traffic light
   - To measure input events eg measurent of car speed

Counters: like timer, but counts pulse on a general input signal rather then clock eg counts cars passing over a sensor, configure deice as either a timer or counter

Watchdog timer: must reset timer every X time unit, else timer generates a signal, common use: detect failure, self reset, timeouts eg. ATM machine.

**Q.6 a. Explain common memory types in detail.** **(8)**

Answer:

. common types of memory

1. Volatile Memory : holds contents while power is applied to the memory device. eg RAM, SRAM, SSRAM, SDRAM, FPGA on chip

2. Non Volatile Memory :- holds contents when power is switched off, making them good choices for storing information that must be retrieved after a system power cycle.

3. On chip memory : is the simplest type of memory for use in a FPGA based embedded system. It is independent of and implemented in FPGA itself. eg. cache, look up tables

b. Explain the main features of ROM and draw internal view of 8×4 ROM.   **(8)**

Answer:

Features of ROM :-

— Non volatile

— Can be read from but not written

— It is used to store software program for general purpose processors

— It stores constant data needed by system

— It implements combinational circuits.

Internal view of 8×4 ROM
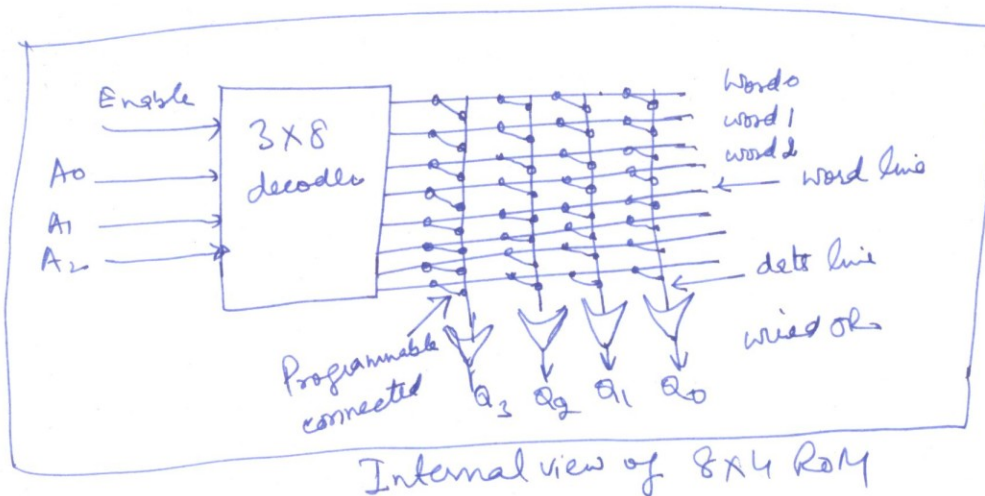
Q.7   a. Explain direct memory access with the help of suitable diagram.   **(8)**

Answer:

· Direct memory Access (DMA): is a feature of modern (4) computer that allows certain hardware subsystem within the computer to access system memory independently of the central processing unit. Without DMA, when the CPU is using programmed I/O, it is typically fully occupied for the entire duration of the read/write operation and it is thus unavailable to perform other work. With DMA, the CPU initiates the transfer, does other operations while transfer is in progress and receives an interrupt from DMA controller when operation is done. This feature is useful any time the CPU cannot keep up with the rate of data transfer or where the CPU needs to perform useful work while waiting for a relative slow I/O data transfer.

X–old value
Y– New value
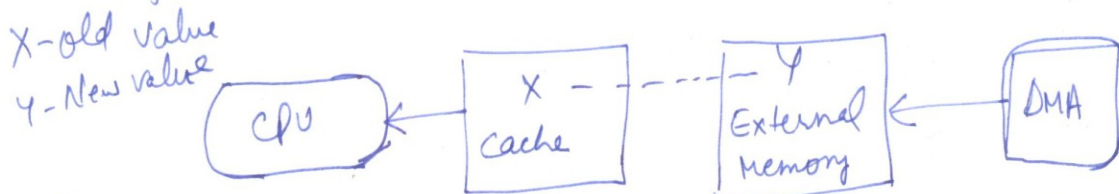
When a CPU accesses location X on the memory, the current value will be stored in the cache. Subsequent operations on X will update the cached copy of X, but not the external memory version of X, assuming a write back cache. If the caches is not flushed to the memory before the next time a device tries to access X, the device will receive a stale value of X. Similarly, if the cached copy of X is not invalidated when the device writes a new value to the memory, the the CPU will operate on the stale value of X.

    b. **Explain basic protocol concepts. With the help of suitable diagram, explain strobe and handshake protocol control methods.**   **(8)**

Answer: **Refer pages 140-141, Fig 6.2 of Text Book-I**

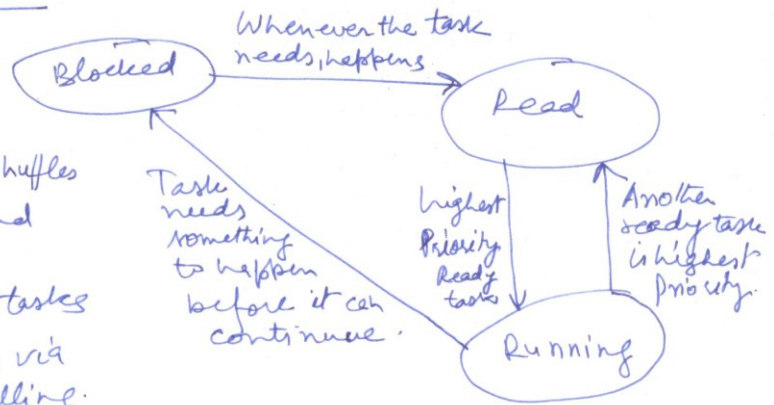 **Q.8** **a.** **Discuss the task states in RTOS.**   **(8)**

Answer:

Task states in RTOS

- Running ⎤
- Ready ⎦
- Blocked
- Scheduler → Schedules/Shuffles tasks between running and ready states.

Blocking is self blocking by tasks and moved to running state via another tasks interrupt signalling. When task is unblocked with higher priority over the running task, the scheduler switches context immediately.

[Diagram: Blocked → "Whenever the task needs, happens" → Ready. Task needs something to happen before it can continue (Blocked → Running). Highest Priority Ready tasks (Ready → Running). Another ready task is highest priority (Running → Ready).]

b. Explain shared data problem and Re-entrant functions in RTOS. **(8)**

Answer: Refer pages 167-169 of Text Book-II

Q.9 **Discuss the case study for sending application layer byte streams on a TCP/IP network using RTOS VxWorks.** **(16)**

Answer: Refer page 537 of Text Book-III

TEXT BOOKS

I.   Embedded System Design, A Unified Hardware/Software Introduction, Frank Vahid / Tony Givargis, 2006 reprint, John Wiley Student Edition
II. An Embedded Software Primer, David .E. Simon, Fourth Impression 2007, Pearson Education
III. Embedded Systems, Raj Kamal, 13th reprint 2007, Tata-McGrawHill Publications