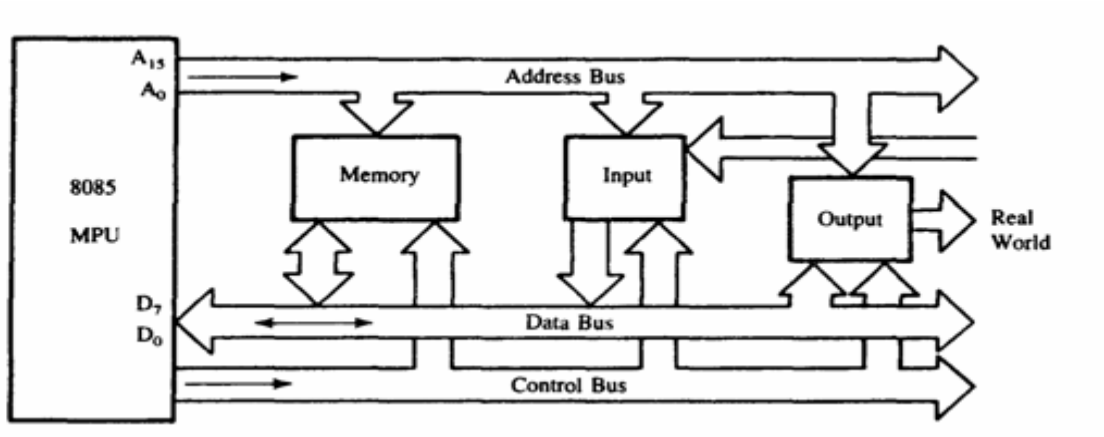
Q.2 a. Draw block diagram schematic of 8085 bus structure. Explain buses/ communication lines used by 8085. (6)

Answer:

8085 Bus organization structure:



8085 MPU and peripheral devices communicate through three set of lines called buses namely- address bus, data bus and control bus.

- **Address bus**- Group of 16 lines A0-A15, unidirectional from MPU to peripheral devices or a memory location. Each device or location is identified by binary number called address. The address bus is also used to send the port address when data is read onto the port or written onto the port..
- **Data Bus**- Consist of 8 parallel lines bidirectional through which instruction, data or address of data transfer takes place between microprocessor, memory or I/O devices.
- **Control Bus**- The lines which carry various synchronization signals to and from the microprocessor to coordinate the data transfer and other supervisory application.

3-Diagram + buses explained correctly 1 mark each (3+3) TOTAL 6marks

b. How many categories of instructions exist in 8085instruction set (as per operations performed)? Discuss each category with example. (10)

Answer:

Categories of 8085 instructions are as follows:

- **Data Transfer Instruction**:These instructions move data between registers, or between memory and registers. These instructions copy data from source to destination. While copying, the contents of source are not modified.
  Example: MOV B, C or MOV B, M
- **Arithmetic Instructions**:These instructions perform the operations like: addition, subtraction, increment, decrement etc.
  Addition-Any 8-bit number, or the contents of register, or the contents of memory location can be added to the contents of accumulator. The result (sum) is stored in the accumulator. No two other 8-bit registers can be added directly.
  Subtraction-Any 8-bit number, or the contents of register, or the contents of memory location can be subtracted from the contents of accumulator. The result is stored in the

accumulator. Subtraction is performed in 2's complement form. If the result is negative, it is stored in 2's complement form. No two other 8-bit registers can be subtracted directly. Increment/ decrement -The 8-bit contents of a register or a memory location can be incremented or decremented by 1.The 16-bit contents of a register pair can be incremented or decremented by 1. Increment or decrement can be performed on any register or a memory location.
Example: : ADD B or ADD M,ADI 45 H,SUB B or SUB M

- **Logical Instructions**-These instructions perform logical operations on data stored in registers, memory and status flags. The logical operations are: AND, OR, XOR,, Rotate, Compare, Complement
  Example: CMP B or CMP M,ANI 86H.
- **Branching Instructions**-The branching instruction alter the normal sequential flow. These instructions alter either unconditionally or conditionally.The program sequence is transferred to the memory location specified by the 16-bit address given in the operand.
  Example: JMP 2034 H, JZ 2034 H ,CALL 2034 H.
- **Control Instructions**-The control instructions control the operation of microprocessor.
  Example: NOP
  The CPU finishes executing the current instruction and halts any further execution. An interrupt or reset is necessary to exit from the halt state.
  Example- HLT, other examples are EI,DI, RIM

Each category explained correctly 2 marks (2X5) TOTAL 10 Marks

Q.3 a. Specify purpose of the following pair of instructions of 8085 and category to which they belong.
(i) CZ and CNZ
(ii) SPHL and PCHL
(iii)XRA and XRI
(iv) RAL and RLC **(8)**

Answer:

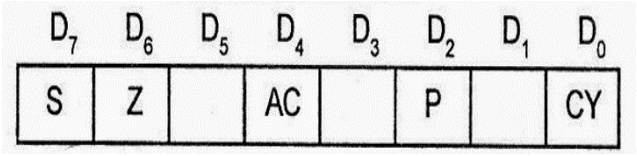
(i) **CZ and CNZ-**Both are branching instructions-Both give call to a subroutine conditionally.CZ gives call if flag status of zero flag is 1 and CNZ gives call when flag status is Z=0
(ii) **SPHL and PCHL**-Both are data transfer instructions. With SPHL the contents of register pair H and L are loaded onto stack pointer without affecting any flag. In PC HL the contents of register pair H and L are loaded onto program counter without affecting any flag.
(iii)**XRA and XRI** : both are arithmetic instructions performing exclusive OR operation with accumulator. With XRA contents of the operand placed in register or memory are XORed and result is placed in accumulator .Content of the operand are not changed.In XRI the operand (data) is XORed with accumulator and result is placed in accumulator
(iv)**RAL and RLC -**Both RLC and RAL perform logical operation on data.RAL rotates each binary bit of accumulator by one position through the carry flag. Bit D7 is positioned onto the carry flag and carry flag bit becomes LSB D0 In RLC each binary bit of accumulator is rotated left .Bit D7 replaces D0 but carry flag contents are not placed in Do as in RAL.

2 marks each for purpose and category defined correctly. (2X4) TOTAL 8 Marks

b. Describe the structure of flag register in 8085 stating purpose of each flag. (8)

Answer:

Structure of flag register in 8085–The flag register in 8085 is an 8-bit register which contains 5 bit positions.The ALU includes five flip-flops, which are set or reset after an operation accordingto data conditions of the result in the accumulator and other registers.



- **Sign Flag-** After execution of arithmetic or logical operation if bit D7 of the result is 1 then carry flag is set. This flag is used for signed numbers. If sign is 1 then number is viewed as negative number. In arithmetic operations with signed numbers bit D7 it is reserved for sign; but it is irrelevant for the operations of unsigned numbers.
- **Zero Flag-** If result of operation is 0 then the flag is set .It is modified by the results in accumulator as well as other registers.
- **AC- Auxiliary Carry-** In an arithmetic operation if the carry is generated by bit D3 and is passed on to D4 this flag is set. Thisflag is used only internally and not available for the programmer to change the sequence of program using JUMP instructions.
- **P-Parity-**After arithmetic or logical operation if the result has even number of 1s this flag is set.
- **CY Carry Flag-** I f an arithmetic operation results in generation of carry then this flag is set. Also serves as a borrow flag in subtraction.

3 Flag register + 1 each for explaining flag operation- 3+5= TOTAL 8 marks

Q.4 a. Write an assembly language program to subtract two eight bit numbers stored in memory locations D000 H and D001 H .The result is stored in D002H. (8)

Answer:

Assembly language program to subtract two eight bit numbers stored in memory locations D000 H and D001 H .The result is stored in D002H.-

```
LXI H, D000 H   : L points to the memory location D000 H
MOV A, M        : Get the contents of the location D000 H into accumulator
INX H           : Increment HL to pint next location
SUB M           : A= A-M Subtraction
INX H           : Increment HL to point memory location D0002H
MOV M,A         : store the result in D0002 H
HLT
```

Program correctly written – Total 8 marks

b. Mention task performed and addressing mode for each of the following instructions:

(i) ADD R **(ii) DCR R**
(iii)JM 16 bit **(iv) ADI 8 bit**
(v) JMP address **(vi) OUT 8 bit port address**
(vii) MVI R, 8 bit **(viii)NOP** **(8)**

Answer:

Sr No	Instruction	task	Addressing Mode
(i)	ADD R	Add (R) to A	Register
(ii)	DCR R	Decrement R	Register
(iii)	JM 16 bit	Jump to 16 bit address if sign flag is set	Immediate
(iv)	ADI 8 bit	Add 8 bit data to A	Immediate
(v)	JMP Address	Jumps to 16 bit address unconditionally	Immediate
(vi)	OUT 8 bit port address	Write data on the output port	Direct
(vii)	MVI R, 8 bit	Load register R with 8 bit data	Immediate
(viii)	NOP	No operation	Machine Control instruction

1 mark each for each instruction Total 8 marks

Q.5 a. What do you mean by non-mask able interrupt? Discuss format of SIM and RIM instruction in 8085 . (8)

Answer:

Non-mask able and mask-able interrupt –Maskable Interrupts can be masked i.e. they can be disabled by writing the proper control word in the control word register. Examples: RST 7.5, RST 6.5, RST 5.5 & INTR. Non-Maskable Interrupts can't be masked i.e. they cannot be disabled when enabled without servicing. They must need to be serviced. They even don't need EI & DI signals (EI= Interrupt Enable, DI= Disable Interrupt) to start or to halt. Example: TRAP.

SIM Instruction: SIM stands for Set Interrupt mask –is a single byte instruction used for

- Masking/unmasking RST 7.5, RST 6.5 and RST 5.5
- Reset 0 RST7.5 Flip-flop
- Perform serial output of data.

When Sim instruction is executed contents of accumulator decide the action to be taken. On execution of SIM the bitwise content of the accumulator decide the effective action to be taken as

D7	D6	D5	D4	D3	D2	D1	D0
SOD	SOE	X	R7.5	MSE	M7.5	M6.5	M5.5

The bits that are used for masking/unmasking are

Bit 3- If it is 0SIM instruction is not used for masking/unmasking

Bit2- If MSE is 1 and M7.5 is 1 RST 7.5 is masked. And if If MSE is 1 and M7.5 is 0 RST 7.5 is unmasked.

Bit 1- If MSE is 1 and M6.5 is 1 RST 6.5 is masked. And if If MSE is 1 and M6.5 is 0 RST 6.5 is unmasked

Bit 0-If MSE is 1 and M5.5 is 1 RST 5.5 is masked. And if If MSE is 1 and M5.5 is 0 RST5.5 is unmasked.

RIM instruction: RIM stands for read interrupt mask**.** It's a single byte instruction used for

- checking masked status of RST 7.5, RST 6.5 or RST 5.5
- Checking enable/disable interrupt
- Pending status of interrupt
- Perform serial input of data.

Meaning of accumulator contents that decide execution of RIM instruction is as shown

D7	D6	D5	D4	D3	D2	D1	D0
SID	IP7.5	IP6.5	IP5.5	IE	M7.5	M6.5	M5.5

First three least significant bits provide mask status of interrupts. Its value if is 1 then corresponding interrupt is masked.
If bit 3(IE) is 1 then interrupt system is enabled .the rest three bits indicate pending status of interrupts-If bit 4,5 or 6 is having value equal to 1 then RST 5.5,RST 6.5 and RST 7.5 requests arerespectively pending. On execution of RIM instruction data on the SID pin of 8085 gets loaded in this bit position.

Difference-2+ SIM/RIM –Fig +explanation (2+1) each- (2+3+3) Total 8 marks

b. List the main features of PPI 8255.What will be the control word format to initialize 8255 in following mode:

PORT A-Mode 0-input ;PORT B –mode 0 Output ; PORT C upper –Mode 0 output and PORT C lower- Mode 0 input (8)

Answer: Main features of PPI 8255:

- It's a programmable parallel I/O device
- Has 24 programmable pins arranged in 2-8 bit and 2-4 bit ports.
- Improves DC driving capability ,TTL compatible
- Three modes of operation Mode-0 ,Mode-1 and Mode-2
- Control register defines format for each I/O port.

Control register format of 8255 to operate as:PORT A-Mode 0-input; PORT B –mode 0 Output; PORT C upper –Mode 0 output and PORT C lower- Mode 0 input

D7	D6	D5	D4	D3	D2	D1	D0
1	MODE		PA	PC_U	MODE	PB	PC_L

Initialization is:-- Port A mode 0 input D6=0 D5=0 and D4=1
Port C upper- Mode 0 output D3=0
Port B mode 0 output – D2=0 D1=0
Port C lower- Mode 0 input – D0=1 = **95 H**

Control word format will be

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1

Features listed -2 +correct interpretation of control register -6 (2+6) Total 8 marks

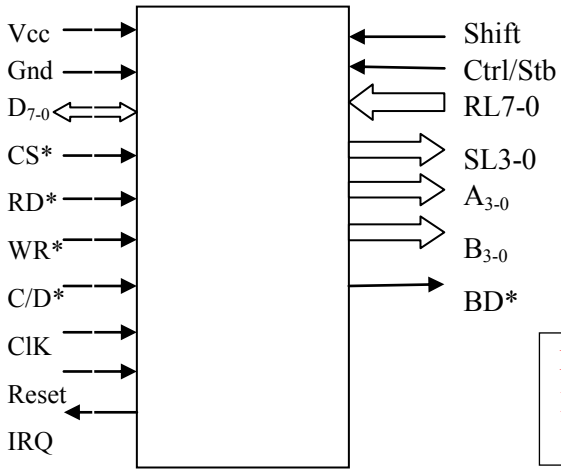
Q.6 a. Draw functional pin diagram of Intel 8279-keyboard and display controller and discuss functions for the following pins-

(i) Reset (ii) Shift
(iii) Ctrl/Stb (iv) IRQ (8)

Answer:

Functional pin diagram of 8279 keyboard and display Controller:

(i) Reset- Active high input pin normally connected to reset out pin of 8085.When 8085 is reset it sends pulse of logic 1 resetting 8279.
(ii) Shift- Connected to shift key on the keyboard. The information of the shift key is meaningful /important only if 8279 is used to interface matrix of switch sensors.
(iii) Ctrl/STB- This input pin is connected to the Ctrl/stb key on the keyboard. It data is meaningful only if 8279 is used to interface matrix keyboard.
(iv) IRQ- It is active high output pin normally connected to the interrupt pin of the processor.

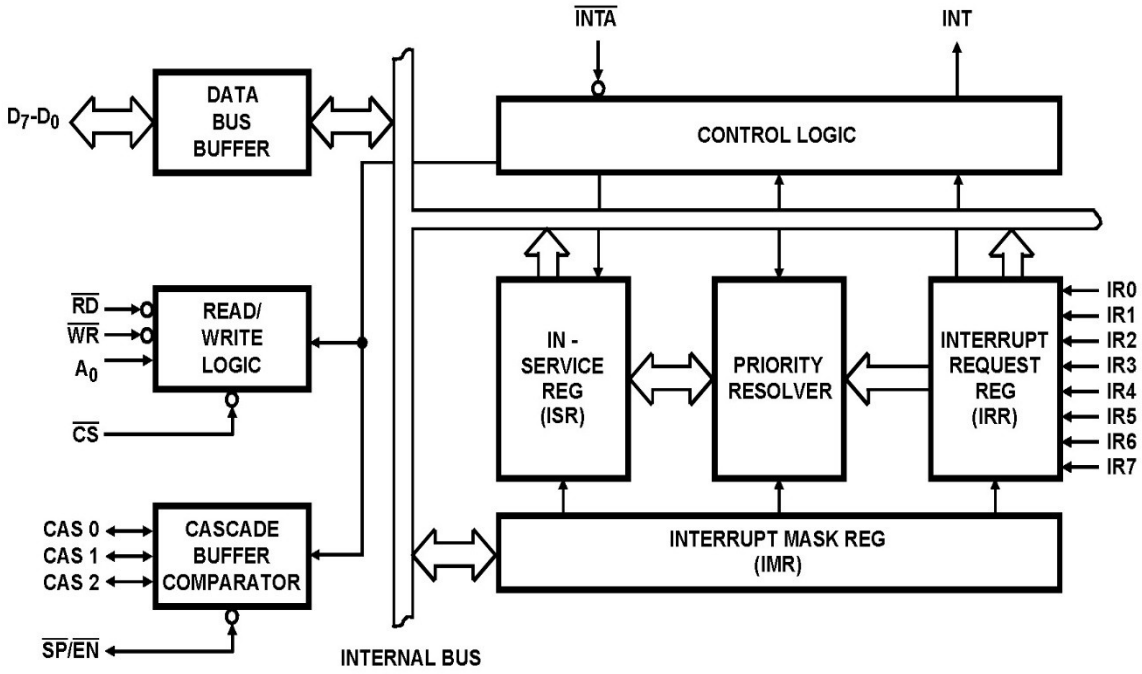


Functional pin diagram 4marks+ pin description 1 mark each (4+4) =Total 8 marks

b. Draw functional block diagram of 8259 programmable interrupt controller. List out the function of each block. . (8)

Answer:

Interrupt controller Intel 8259 functional block diagram:



- Data transfers data between microprocessor and internal bus.
- Read/write logic- When Address line A0 is at logic 0 the controller is selected to write command .the chip select logic and A0 determine the port address of the controller.
- Cascaded buffer /comparator- In master mode functions as cascaded buffer. In slave mode functions as comparator
- Control logic- Has two pins INT- connected to interrupt pin of MPU and INTA – indicates interrupt acknowledge signal from MPU.
- IRR- Interrupt Request Register- stores all pending interrupt requests

- ISR (In Service Register) Stores all interrupt levels currently being processed.
- Priority resolver- sets the priority of the bit set in IRR looking up to ISR handles interrupt requests as per priority.
- Interrupt Mask Register- IMR- It's a programmable register used to mask unwanted interrupt request.

Block diagram 4marks+ functions 0.5 mark each (4+4) =Total 8 marks

Q.7 a. What is the need for DMA controller? List features of DMA controller 8257. Also specify functions of following pins of Intel 8257 DMA Controller.

(i) ADSTB (ii) $\overline{IOW}$ (iii)HRQ (iv) HLDA (8)

Answer:

Need for DMA controller-. In a microcomputer, microprocessor is connected with memory and different I/O devices. To perform operations of data transfer, status check I/O and interrupt data transfer, as each task is routed through MPU. Overall performance becomes relatively slow because each instruction needs to be fetched and executed by MPU.With DMA controller faster data transfer can take place bypassing MPU. DMA controller also facilitates high speed data transfer between system memory and floppy

Features of DMA-

- It is a 4 channel direct memory access interface.
- Can be operated in three modes DMA read,DMA write and DMA verify
- It has two group of signals – interfacing with MPU and for communication with peripherals.
- Operates in two priorities Fixed and rotating

PIN functionality of DMA 8257:

(i) ADSTB- Address strobe Active high output signals that are used to latch a higher order address byte to generate 16 bit address.

(ii) $\overline{IOW}$ -Active low bidirectional tristate line. In master mode it's a control output to a peripheral during DMA cycle. In slave mode allows the content of data bus to be loaded into 8 bit mode set register

(iii)HRQ - HOLD request connected to hold input of CPU. It has to mandatorily confirm specified set up and hold time. -

(iv)HLDA-Hold acknowledge- this input from CPU indicates that 8257 has acquired control of system bus.

Need for DMA -2+Features-2 +Pin functions 1 each- (2+2+4) total 8 marks

b. What is the need for 8253 interval timer in micro computer system? State functionality of following pins of 8253

(i) $\overline{CS}$ (ii) CLK (iii) GATE (iv) $\overline{RD}$ (v) $\overline{WR}$ (vi) OUT (8)

Answer:

Need of a programmable interval timer in microcomputer system-There are many situations where accurate delays are required to be generated in a microcomputer system. Use of hardware like timer 555 is processor time consuming process .So to introduce accurate delays using hardware programmable interval timer is used. The counters can be configured to work in following modes-

- Mode0 Interrupt on the terminal count
- Mode1- Re-trigger able monostable multi
- Mode 2- rate generator
- Mode3- Square wave generator
- Mode 4- software triggered strobe
- Mode 5- hardware triggered strobe

Functionality of pins of IC 8253 :

Sr No	PIN	Function
i	$\overline{CS}$	Chip select Active low input signal used to select Ic 8253
ii	CLK	/clock input- 3 independent counters .The pulses applied these pins can be counted by respective counters
iii	GATE	Gate control Active high input signal used to allow external hardware to control the respective counter
iv	$\overline{RD}$	Read Active low input used in coordination with A0 A1 to send data tfrom appropriate counter to data lines
v	$\overline{WR}$	Write Active low input signal used in coordination with A0 A1 to load counters
vi	OUT	Active high output lines. Output depends upon counter mode selected.

Need (2) + Pins correctly specified 1 each (2+6) TOTAL 8 marks

Q8. a. Discuss in brief what information is indicated on Intel 8251 USART control port to configure it for transmission / reception in asynchronous mode? (8)

Answer:

Intel 8251 USART configuration for transmission /reception in asynchronous mode: The parallel data to be transmitted in serial format is sent by processor to the transmit buffer of 8251.The transmit buffer is an 8 bit port that can be written but not read by the processor. The processor write to the transmit buffer by activating CS* and WR* inputs of 8251.Intel 8251 programmed and configured to suit our requirements by writing on to the control port. The control port is used to supply information about- mode instruction, synchronization of characters (s) and command instruction. For asynchronous transmission/reception information indicted includes-

Number of bits/character- ASCII code is normally used for representing a character .It uses a 7 bit code. Extended ASCII code used 8 bits that are used when some special characters are to be represented./intel allows user to specify character lengths as 5,6,7 or 8 bits by writing appropriate bit on MI.

- **Parity bit**- Serial communication since used over long distances, during transit data may get corrupted because of noise on the communication medium. The receiver of the data needs to be sure about the correctness of the received data. This is achieved by appending a parity bit at the end of the character. there are two types of parity bits –even and odd. Even parity bit is appended if data has number of 1's in the data are even.

- **Start and stop bit**- The time gap included in the asynchronous transmission/ reception is identified by start bit appended at the beginning and stop bit at the end of the information. When there is nothing to transmit the TxD of 8251 will be in 1 state ,receiver will know that transmission state is on but nothing is being tranmitted.At the onset on information transmission a start bit is sent which is always logical 0 then

LSB of information and then MSB of information ,parity bit is sent then followed by stop bit at the end. Stop bit is always logical 0.The number of stop bits can be programmed to be 1,1.5 or 2 bits.
Even if transmitter/ receiver frequency mismatch exists there is no problem in the communication as with every start bit synchronisation takes place. Also the number of stop bits cater for the time gaps.

Number of characters for transmitting and receiving a bit- Intel 8251 uses a transmit clock TXC* input to send out the information in transmit shift register. For every falling edge of the TxC* a of transmit shift register is sent out on TxD output if 8251 is programmed in X1 mode If X16 mode a bit is sent out for every 16.clock.In X64 mode it is sent out after every 64 clock transmission on TxC*.

All configuration information explained -Total 8 marks

b. Write an assembly language program for multiplication of two 8 bit numbers X and Y using repetitive addition (8)

Answer:

Assembly language program for multiplication of two 8 bit numbers X and Y using repetitive addition.-

Program	Comment
LXI H ,0000H	Initialize HL pair
MVI C,X	Load first nuber in register C
MVI B 00H	Clear register B
MVI D,Y	Load 2nd number in D
L1: DAD B	HL + BC-> HL
DCR D	Decrement D
JNZ L1	Repeat till zero flag =1
SHLD 5000H	Store the result in 5000H

Correct program TOTAL 8 marks

Q.9 a. Compare & contrast microcontrollers and microprocessors. List features of 8051 microcontroller. (8)

Answer:

Microcontroller Vs microprocessor (at least **three** points of comparison are expected)

Microprocessor	Microcontroller
Single memory that includes program and data memory	Separate program and data memory
Several instructions for data transfer	Limited instructions(one or two) for data transfer
Different ICs for memory & I/O	Built in memory & I/O
Few multifunctional pins	More multifunctional pins

- Features of 8051 microcontroller:(any **ten** features are expected)
  - 8 bit CPU optimized for control operations
  - 4 KB on chip program memory
  - Two 8-bit timer controllers
  - Full duplex serial data transmitter/receiver

- Four register banks
- 128 bytes of on chip data memory
- On chip oscillator and clock circuits
- 8-bit program status word and stack pointer
- 64KB program RAM and 64KB external RAM addressability
- Direct bit and byte addressability
- Binary/decimal arithmetic
- Integrated Boolean processor for control applications
- Signed overflow detection and parity computation

3 marks for comparison+ 0.5 marks for each feature(0.5X10) 3+5= total 8 marks

b. Describe (with suitable examples) all the addressing modes available in 8051 (8)

Answer: Addressing modes available in 8051

- **Immediate Addressing-** Immediate addressing is so-named because the value to be stored in memory immediately follows the operation code in memory. That is to say, the instruction itself dictates what value will be stored in memory

  For example, the instruction: MOV A,#20H

  This instruction uses Immediate Addressing because the Accumulator will be loaded with the value that immediately follows in this case 20 (hexadecimal).Immediate addressing is very fast since the value to be loaded is included in the instruction. However, since the value to be loaded is fixed at compile-time it is not very flexible.
- **Direct Addressing-** Direct addressing is so-named because the value to be stored in memory is obtained by directly retrieving it from another memory location.

  For example: MOV A,30H

  This instruction will read the data out of Internal RAM address 30 (hex) and store it in the Accumulator. Direct addressing is generally fast since, although the value to be loaded is not included in the instruction, it is quickly accessible since it is stored in the 8051s Internal RAM. It is also much more flexible than Immediate Addressing since the value to be loaded is whatever is found at the given address--which may be variable. Also, it is important to note that when using direct addressing any instruction which refers to an address between 00h and 7FH is referring to internal Memory.
- **Indirect Addressing-**Indirect addressing is a very powerful addressing mode which in many cases provides an exceptional level of flexibility. Indirect addressing appears as follows:

  MOV A,@R0

  This instruction causes the 8051 to analyse the value of the R0 register. The 8051 will then load the accumulator with the value from Internal RAM which is found at the address indicated by R0. For example, lets say R0 holds the value 40H and Internal RAM address 40H holds the value 67H. When the above instruction is executed the 8051 will check the value of R0. Since R0 holds 40H the 8051 will get the value out of Internal RAM address 40H (which holds 67H) and store it in the Accumulator. Thus, the Accumulator ends up holding 67H.
- **External Direct**-External Memory is accessed using a suite of instructions which use what I call "External Direct" addressing. There are only two commands that use External Direct addressing mode:

  MOVX A,@DPTR

MOVX @DPTR,A

Both commands utilize DPTR. In these instructions, DPTR must first be loaded with the address of external memory that you wish to read or write. Once DPTR holds the correct external memory address, the first command will move the contents of that external memory address into the Accumulator. The second command will do the opposite: it will allow you to write the value of the Accumulator to the external memory address pointed to by DPTR.

- **External Indirect-**External memory can also be accessed using a form of indirect addressing which External Indirect addressing. This form of addressing is usually only used in relatively small projects that have a very small amount of external RAM. An example of this addressing mode is:

MOVX @R0,A

The value of R0 is first read and the value of the Accumulator is written to that address in External RAM. Since the value of @R0 can only be 00H through FFH the project would effectively be limited to 256 bytes of External RAM.

All addressing modes with example –Total 8 marks

TEXT BOOK

The 8085 Microprocessor; Architecture, Programming and Interfacing, K. Udaya Kumar and B. S. Umashankar, Pearson Education, 2008