Q.2 a. Perform the following conversions: **(8)**

(i) $(735)_8 = (?)_2$

(ii) $(37FD)_{16} = (?)_{10}$

(iii) $(37.45)_{10} = (?)_2$

(iv) BCD number 1001001110000110 in to its decimal equivalent.

Answer:

(i) $(735)_8 = (?)_2$

7 3 5

111 011 101

$\therefore \boxed{(735)_8 = (111011101)}$

(ii) $(37FD)_{16} = (?)_{10}$

$\Rightarrow (3\times16^3) + (7\times16^2) + (15\times16^1) + (13\times16^0)$

$\Rightarrow 12288 + 1792 + 240 + 13$

$= 14333$

$\therefore (37FD)_{16} = (14333)_{10}$

(iii) $(37.45)_{10} = (?)_2$

⇒

2 | 37		
2 | 18	1	↑
2 | 9	0	
2 | 4	0	
2 | 2	1	
2 | 1	0	
0	1	

$(37)_{10} = (100101)_2$

$0.45\times2 = 0.9 \quad 0$

$0.9\times2 = 1.8 \quad 1$

$0.8\times2 = 1.6 \quad 1$

$0.6\times2 = 1.2 \quad 1$

$0.2\times2 = 0.4 \quad 0$

$(0.45)_{10} = (0111)_2$

$\therefore (37.42)_{10} = (100101.01110)_2$

(IV) BCD Number is

1001 0011 1000 0110

9 3 8 6

Result = $(9386)_{10}$.

b. Define binary system. (2)

Answer:

Binary system :-

In the binary system there are only two symbols or possible digit values, 0 and 1. This base-2 system can be used to represent any quantity that can be represented in decimal or other number system. In binary system, the term binary digit is often abbreviated to the term bit.

c. What are advantages and limitations of digital system over analog system? (6)

Answer:

Advantages of Digital system

(1) Digital system are generally easier to design
(2) Information storage is easy
(3) Accuracy and Precision are greater.
(4) Operation can be programmed.
(5) Digital circuits are less affected by Noise.
(6) More digital circuitry can be fabricated on IC chips.

Limitation

(1) The real world is mainly Analog.

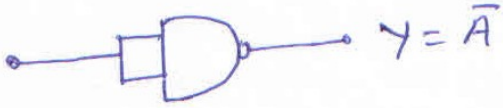
Q.3 a. What do you mean by universal gate? Implement AND, OR and NOT gate using any one of universal gate. (5)

Answer:

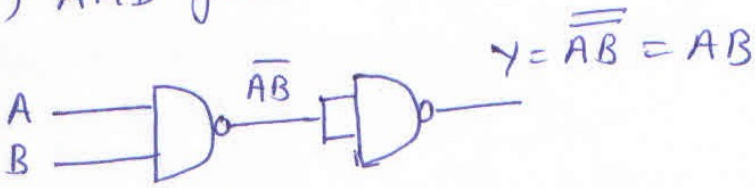
Universal gate :- The "NAND" operation and "NOR" operation have become very popular and are ~~widely~~ widely used, the reason being that only one type of gates, either NAND or NOR are sufficient for realization of any logical expression. Because of this reason, NAND and NOR gates are known as Universal gates.

Realization of gates by using NAND gate

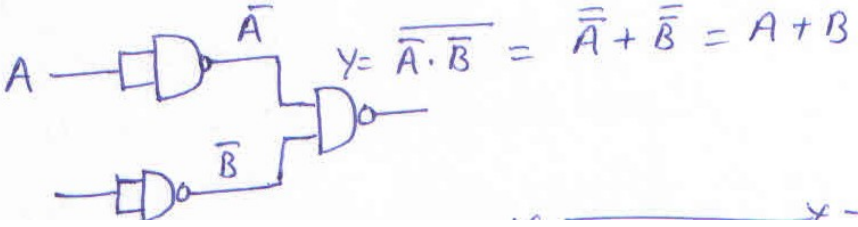
(i) NOT gate



(ii) AND gate



(iii) OR gate



b. Simplify the following expression, construct the corresponding logic circuit using basic gates. (6)

$Y = A + \bar{B}C + ABC + A\bar{B}C$

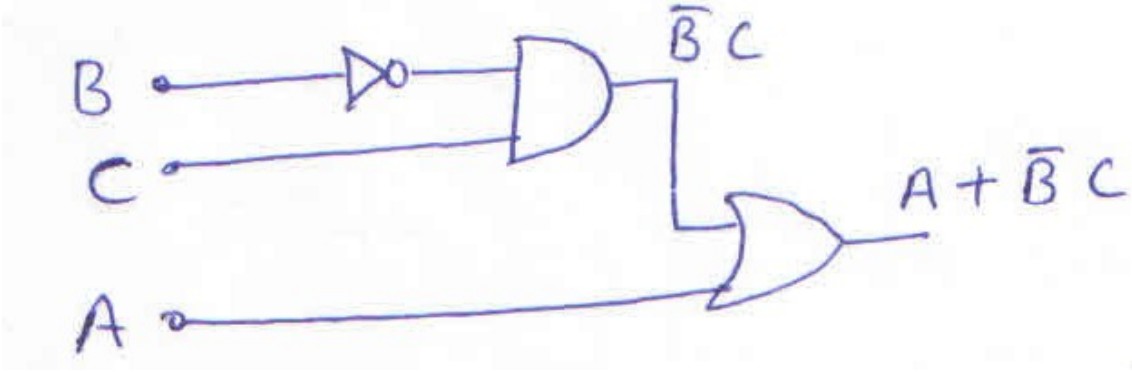
Answer:

Given $Y = A + \bar{B}C + ABC + A\bar{B}C$

$Y = A + \bar{B}C(A+1) + ABC$

$Y = A + \bar{B}C + ABC$

$Y = \bar{B}C + A(1+BC) = \bar{B}C + A$



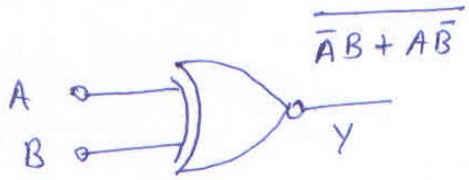
c. Draw the symbol of XNOR gate and explain its working with the help of truth table. (5)

Answer:

Exclusive-NOR gate :- XNOR gate

This gate has two inputs and one output. In Ex-NOR gate, the output is high when both inputs are high, otherwise output is low. A truth table and logic symbol is given below

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



$Y = \overline{A \oplus B} = AB + \bar{A}\bar{B}$

Q.4a. Perform the following operations: (8)

(i) Subtract -36 from - 15 using 2's complement.

(ii) Add 623 and 599 using BCD code.

Answer:

(i) Subtract -36 form -15 using 2's complement.

$-15 : (15)_{10} = (1111)_2 = 0001111$

$-(-36) :$ 2's complement = 1's complement + 1

$= 1110000 + 1$

$(-15)_{10} = 1110001$

$-15 = 1110001$

$-(-36) = 0100100$

$1\,0010101$

Discarded

the result is $0010101 = +21$

(ii) Add 623 & 599 using BCD

$623 = 0110\,0010\,0011$

$599 = 0101\,1001\,1001$

$1011\,1011\,1100$ ← Invalid sum.

$0110\,0110\,0110$ ← Add 6 to correct

$1\,0010\,0010\,0010$

1 2 2 2

b. Design and explain full adder circuit using truth table. (8)

Answer:

Design of Full Adder

Truth table of Full Adder is

A	B	Cin	Sum S	Carry Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table having three inputs A, B, Cin and two outputs S and Cout. There are eight possible cases for the three inputs, and for each case the desired output values are listed.

Since there are two outputs, we will design the circuitry for each output individually. For S, the truth table shows that there are four cases where S = 1.

Using SOP method, expression for S is

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

$$\text{Or } S = \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}) + A(\bar{B}\bar{C}_{in} + BC_{in})$$

$$\text{Or } S = \bar{A}(B \oplus C_{in}) + A(\overline{B \oplus C_{in}})$$

If we let $X = B \oplus C_{in}$, then

$$S = \bar{A}X + A\bar{X} = A \oplus X$$

Replacing X, we have

$$S = A \oplus [B \oplus C_{in}] \quad \text{---} \quad (1)$$

Similary SOP for Cout

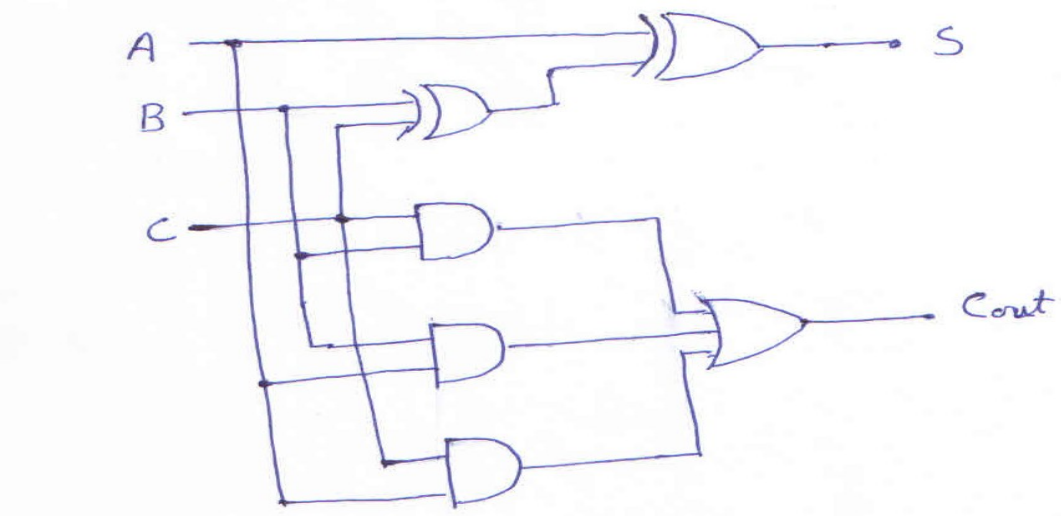
$$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in}$$

$$= BC_{in}(\bar{A} + A) + AC_{in}(\bar{B} + B) + AB(\bar{C}_{in} + C_{in})$$

$$= BC_{in} + AC_{in} + AB. \quad \text{---} \quad (2)$$

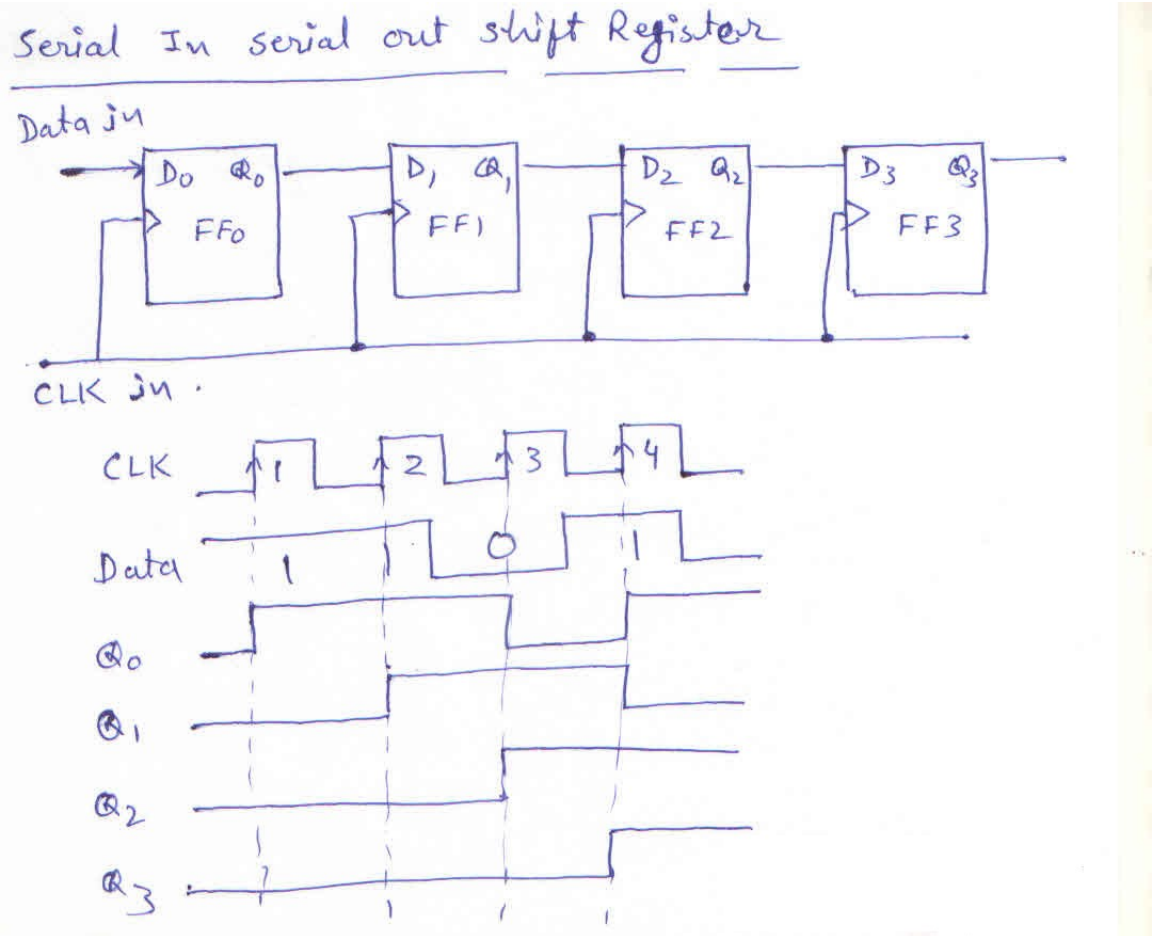
This expression cannot be simplified further.

Expression (1) and (2) can be implemented as shown in figur below.



Q.5 a. Draw the circuit of 4 bit serial in serial out shift register and explain its working. (8)

Answer:



Figur shows a 4 bit serial in serial out shift register consisting of four D flop flops FF_0, FF_1, FF_2, FF_3. As shown it is positive edge triggered device. We study the working of this register for the data 1010 in the following steps.

1. Bit 0 is entered in to data input line $D_0 = 0$, first clock pulse is applied. FF_0 is reset and stores 0.
2. Next bit 1 is entered $Q_0 = 0$, since Q_0 is connected to D_1, D_1 becomes 0.
3. Second clock pulse is applied. The 1 on the input line is shifted into FF_0, The '0' was stored in FF_0 is shifted into FF_1
4. Next bit 0 is entered and 3rd clock pulse applied. '0' is entered into FF_0, '1' stored in FF_0 is shifted to FF_1 and '0' stored in FF_1 is shifted to FF_2.
5. Last bit 1 is entered and 4th clock pulse applied. '1' entered in FF_0, '0' stored in FF_0 is shifted to FF_1, '1' stored in FF_1 is shifted to FF_2 and '0' stored in FF_2 is shifted to FF_3. This completes the serial entry of 4 bit data into the register. Now LSB '0' is on the output Q_3.
6. 5th clock pulse is Applied, LSB '0' is shifted out. The next bit '1' appears on Q_3 output.
7. 6th clock pulse is applied, the '1' on Q_3 is shifted out and '0' appears on Q_3 output.
8. 7th clock pulse is applied, '0' one Q_3 is shifted out Now '1' appears on Q_3 output.
9. 8th clock pulse is applied, '1'(one) on Q_3 is shifted out. When the bits are being shifted out, more data bits can be entered in

b. Explain design procedure to design synchronous counter whose state transition diagram is shown in Fig.1. (8)

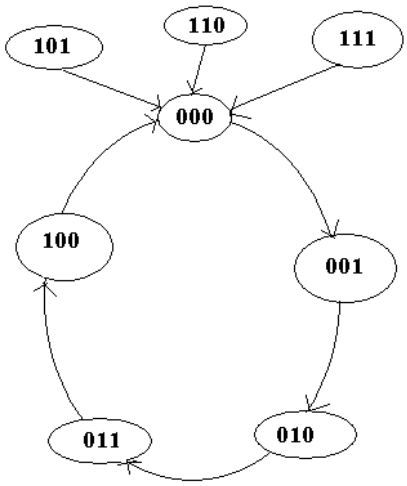
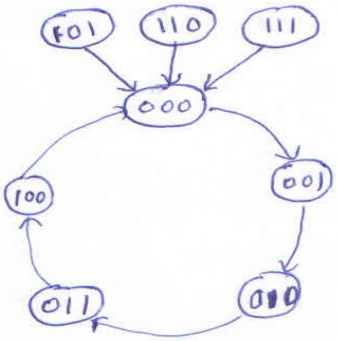


Fig.1

Answer:

Given state transition diagram is



Step 1 :- Determine the desired numbes of bits (FFs) and the desired counting sequence.

Step 2 :- From the state transition diagram set up a table that list all "present" states and their 'Next' states.

Table shown below shows Present state and Next state.

Line	Present state			Next state		
	C	B	A	C	B	A
1	0	0	0	0	0	1
2	0	0	1	0	1	0
3	0	1	0	0	1	1
4	0	1	1	1	0	0
5	1	0	0	0	0	0
6	1	0	1	0	0	0
7	1	1	0	0	0	0
8	1	1	1	0	0	0

Step 3 :- Add a column to this table for each J and K input. For each Present state, indicate the levels required at each J and K input in order to produce the transistion to the next state.

Line	Present state C B A	Next state C B A	J_C	K_C	J_B	K_B	J_A	K_A
1	0 0 0	0 0 1	0	X	0	X	1	X
2	0 0 1	0 1 0	0	X	1	X	X	1
3	0 1 0	0 1 1	0	X	X	0	1	X
4	0 1 1	1 0 0	1	X	X	1	X	1
5	1 0 0	0 0 0	X	1	0	X	0	X
6	1 0 1	0 0 0	X	1	0	X	X	1
7	1 1 0	0 0 0	X	1	X	1	0	X
8	1 1 1	0 0 0	X	1	X	1	X	1

Step 4 :- Design the logic circuits to generate the levels required at each J and K input.

Solve J_A, K_A, J_B, J_C, K_B, K_C using K-map from above table.

For J_A

	$\bar{A}$	A
$\bar{B}\bar{C}$	1	X
$\bar{B}C$	0	X
BC	0	X
$B\bar{C}$	1	X

$J_A = \bar{C}$

For K_A

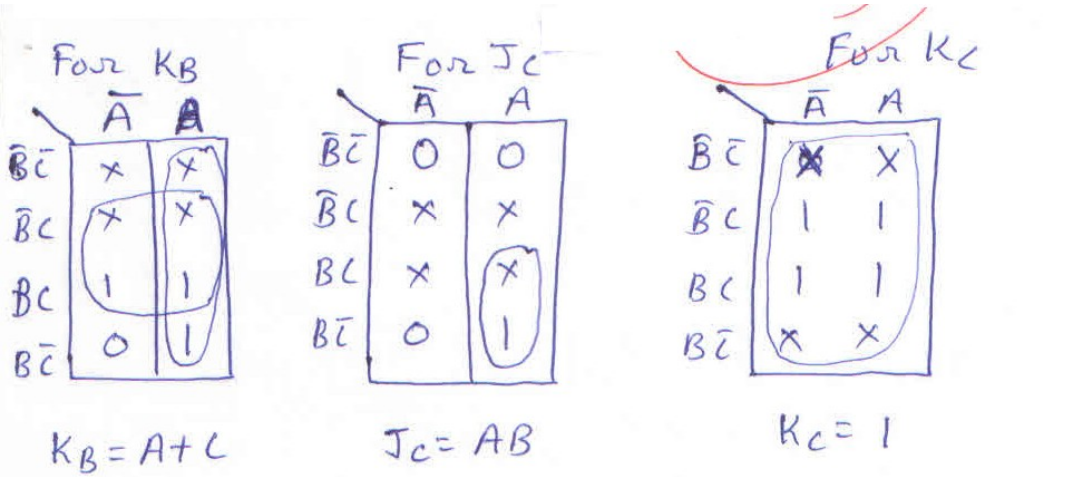
	$\bar{A}$	A
$\bar{B}\bar{C}$	X	1
$\bar{B}C$	X	1
BC	X	1
$B\bar{C}$	X	1

$K_A = 1$

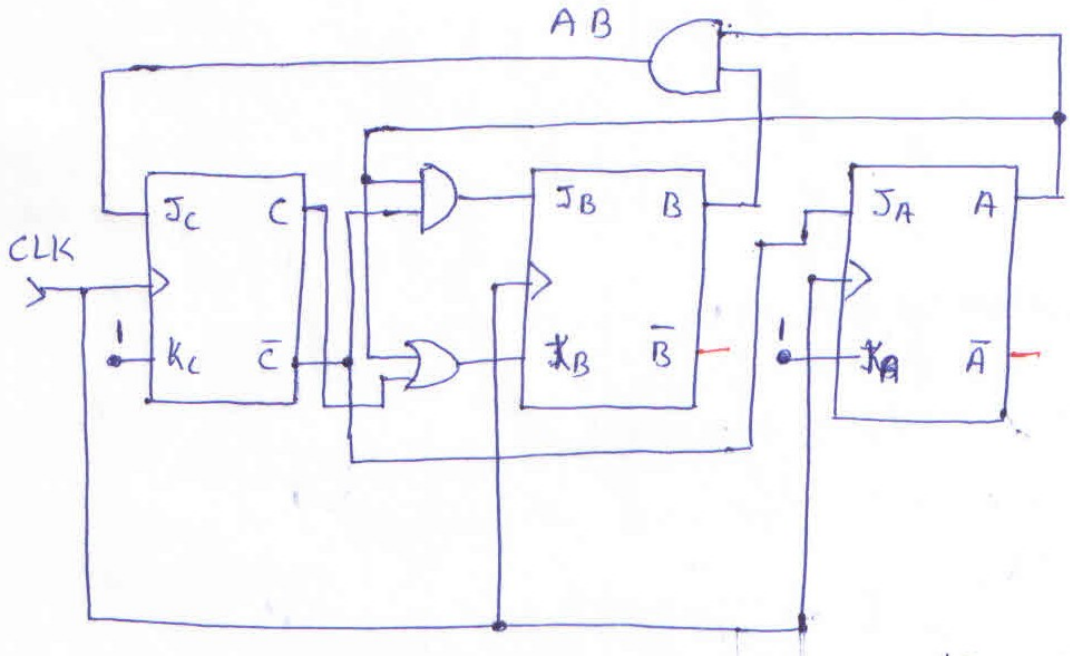
For J_B

	$\bar{A}$	A
$\bar{B}\bar{C}$	0	1
$\bar{B}C$	0	0
BC	X	X
$B\bar{C}$	X	X

$J_B = A\bar{C}$



Step-5 :- Implement the final expression.



Q.6 a. What is decoder? Explain working of a 3 to 8 line decoder with the help of its detailed logic diagram and truth table. (8)

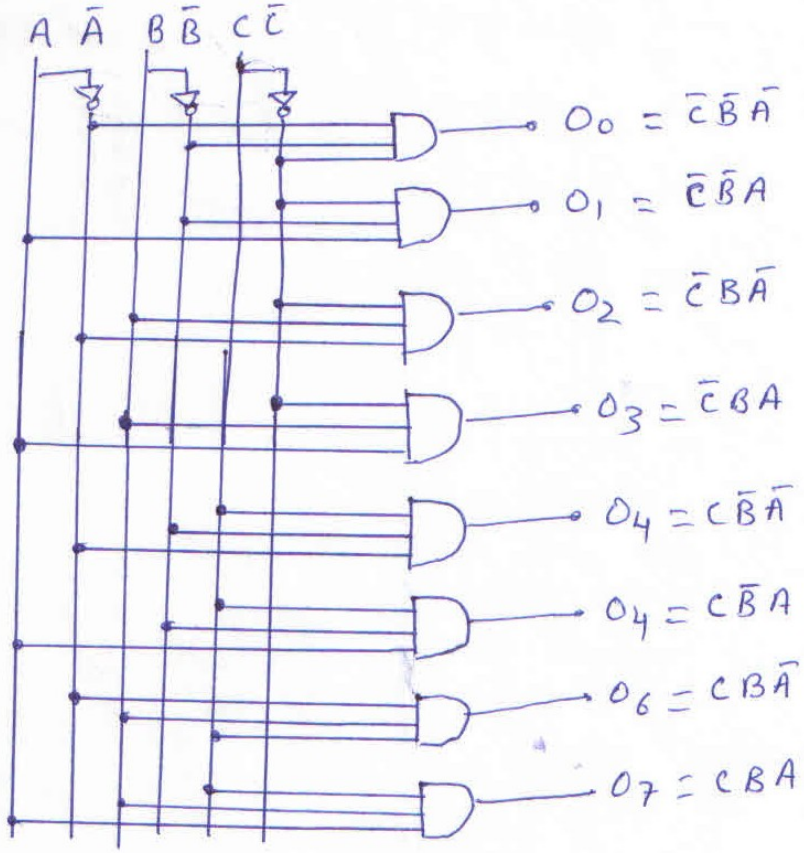
Answer:

Decoders :- A decoder is a logic circuit that accepts a set of inputs that represents a binary number and activates only the output that corresponds to that input number.

Figur shows Block diagram of General decoder.

For N inputs, there are $M = 2^N$ outputs.

Figur shown below the circuitry of four a decoder with three inputs and $2^3 = 8$ outputs. It uses all AND gates, and so the outputs are active HIGH. Note that for a given input code, the only output that is active is the one corresponding to the decimal equivalent of the binary input code. It can be called a 3 to 8 decoder.



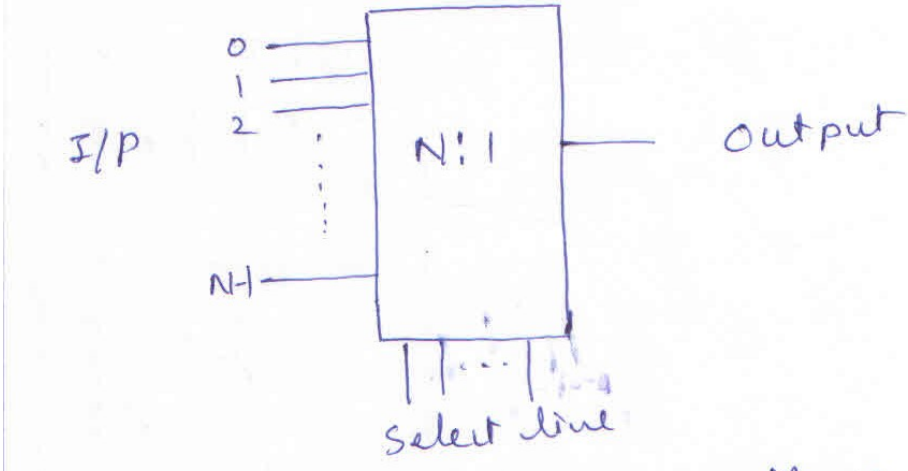
Truth table of 3 to 8 Decoder shown below.

C	B	A	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

b. What is multiplexer? Draw logic diagram of four inputs multiplexer and explain its working. (8)

Answer:

Multiplexer :- A multiplexer is a device having many inputs and one output. By applying control signals, any one of the input can be steered to the output. Figur shows block diagram of Multiplexer.

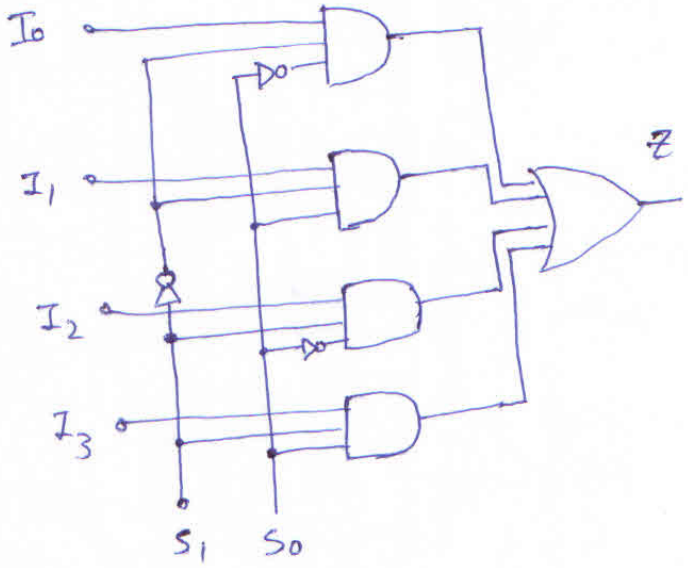


For N inputs, Select line $m \simeq 2^m = N$

Four - Input Multiplexer :

Figure shown below a multiplexer with 4 inputs and 2 data select lines. A two binary code on the data select inputs allows the corresponding data to appear at output Y. The data input lines are I_0, I_1, I_2, I_3 and select lines as S_0 & S_1. The data selection is shown in the truth table.

S_1	S_0	Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



It is clear that

when $S_0 = 0$, $S_1 = 0$, $Z = I_0$ $\therefore Z = I_0 \bar{S}_1 \bar{S}_0$

when $S_1 = 0$, $S_0 = 1$, $Z = I_1$ $\therefore Z = I_1 \bar{S}_1 S_0$

when $S_1 = 1$, $S_0 = 0$ $Z = I_2$ $\therefore Z = I_2 S_1 \bar{S}_0$

when $S_1 = 1$, $S_0 = 1$ $Z = I_3$ $\therefore Z = I_3 S_1 S_2$

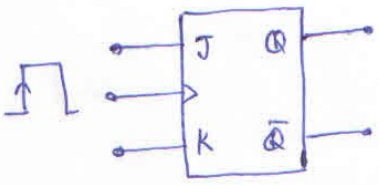
If above equation ORed together, then expression for output Z is

$$Z = I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 + I_3 S_1 S_2$$

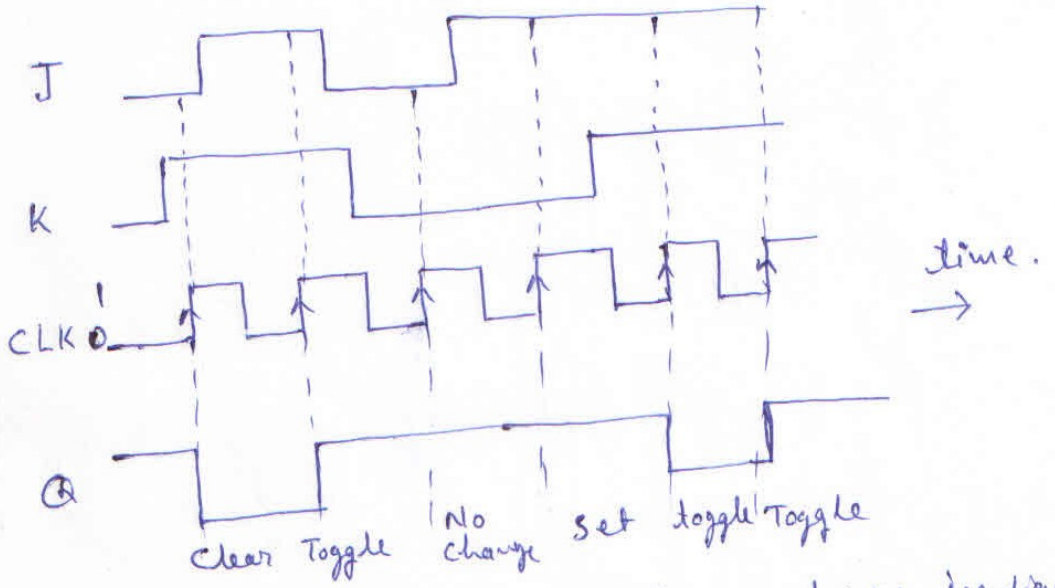
Q.7 a. Draw the logic diagram of JK flip flop and explain its working using truth table. (6)

Answer:

Clocked J-K Flip flop :-



J	K	CLK	Q	Remark
0	0	↑	Q_0	No change
1	0	↑	1	Set
0	1	↑	0	Reset
1	1	↑	$\bar{Q}_0$	Toggles



The truth table of JK flip flop is shown in figure above. The operation of this FF is shown by the wave form in figure above. Working of flip flop can be explained in the following steps.

(1) Initially all inputs are 0 and the Q output is assumed to be 1; that is $Q_0 = 1$

(2) when the positive going edge of the first clock pulse occurs, the J=0, and K=1, condition exists. Thus FF will be cleared to the Q=0 state.

(3) The second clock pulse finds J=K=1, when it makes its positive transition. This cause the FF to toggle to its opposite state, i.e. $Q_0 = 1$.

④ Next clock pulse finds J=K=0, so that the FF does not change states on this transition.

⑤ During next clock pulse, J=1, K=0. This is the condition that sets Q to the '1' state. However it is already 1, and so it will remain there.

⑥ During next clock pulse transition, J=K=1, and so the FF toggles to its opposite state.

Note that from these wave forms that the FF is not affected by the negative going edge of the clock pulse.

b. Consider the circuit shown in Fig.2, **(10)**

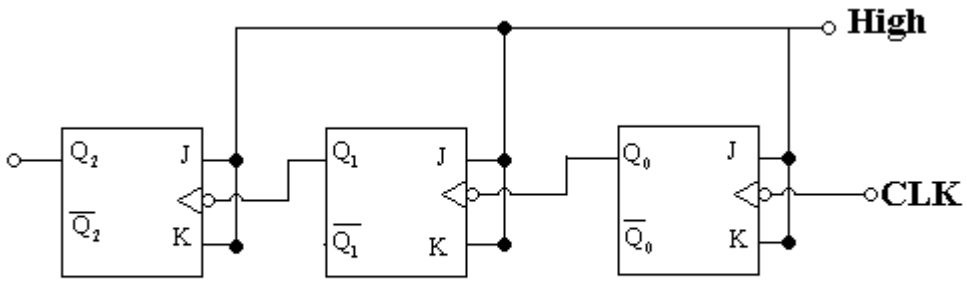


Fig.2

Answer:

(i) Determine the counter's MOD number

.

(ii) Determine the frequency at the output of the last FF (Q2) when the input clock frequency is 1MHz.

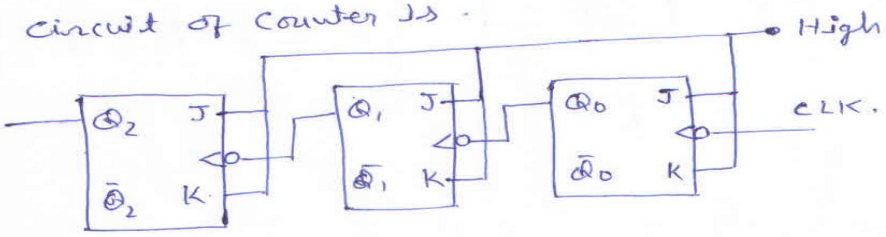
(iii) What is the range of counting state for this counter?

(iv) Assume starting state is 000. What will be the counter's state after 129 pulses?

(v) Draw waveforms at Q_0, Q_1, and, Q_2 for the 10 input clock pulses.

Answer:

Given circuit of Counter is :



(a) MOD Number :-

MOD Number $= 2^3 = 8$

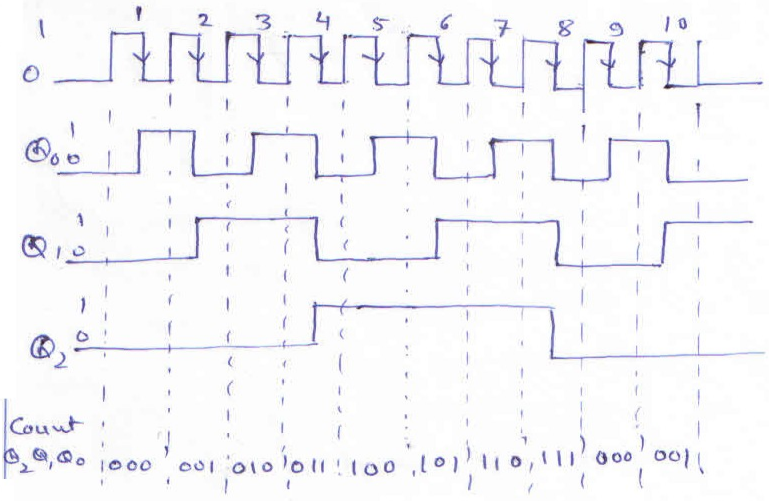
(b) The Frequency of last Flip flop will equal the input clock frequency divided by MOD number. That is

$$f(\text{at } Q_2) = \frac{1MHz}{8} = 125\,KHz.$$

(c) The counter will be count ~~from~~ 000 to 111 for a total of 8 states. Note that the number of states is the same as the ~~mode~~ MOD number.

(d) Since this is a MOD-8 Counter, every 8 clock pulses will bring the counter back to its starting state. Therefore, after 128 pulses the count is back to 000. The 129th pulse bring the counter to the 001 counter.

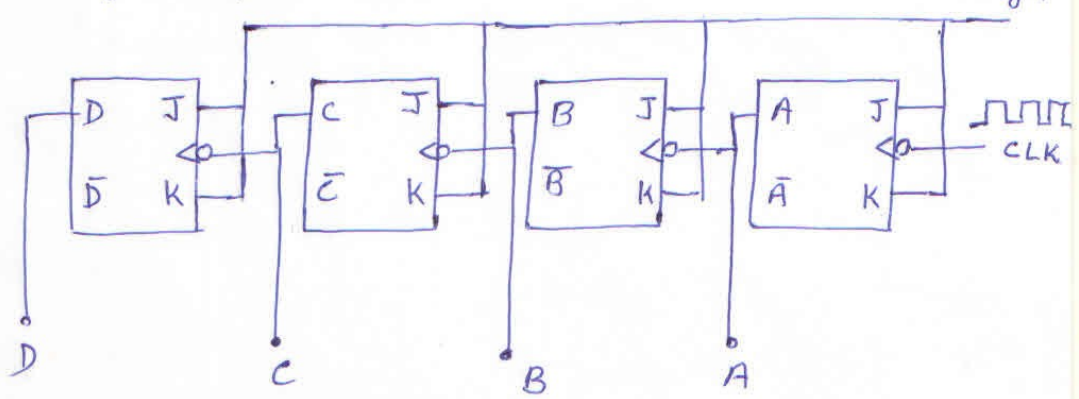
(e) Wave forms at Q_0, Q_1, Q_2 is shown below for 10 input clock pulses.

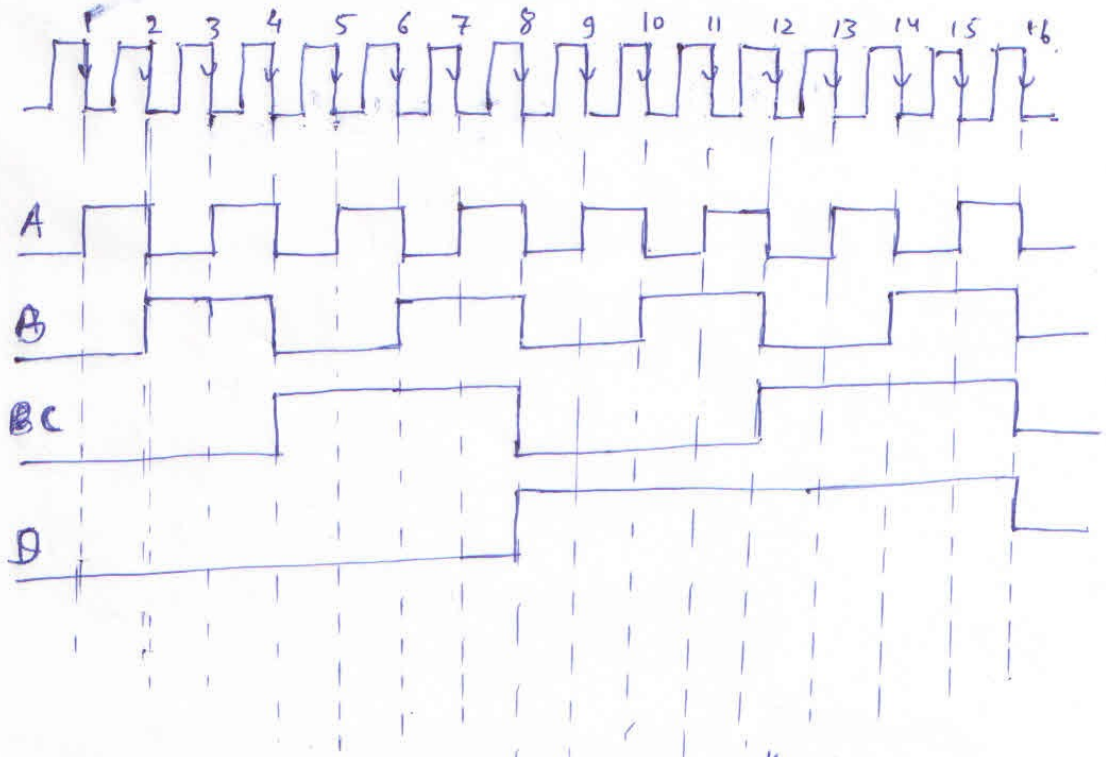


Q.8 a. Explain working principle of ripple counter with suitable logic diagram. (8)

Answer:

Figure shows the circuit of 4 bit ripple counter consisting of 4 edge triggered Flip flops.





Operation of Ripple counter is as follows.

(1) The clock pulse is applied only to the CLK input of flip flop A. A will toggle its operation each time to the clock pulses make a negative transition. Note that J = K = 1.

(2.) The normal output of flip flop A acts as the CLK input for flip flop B, and so flip flop B will toggle each time the A output goes from 1 to 0. Similarly, flip-flop C will toggle when B goes from 1 to 0, and flip flop D will toggle when C goes from 1 to 0.

(3) FF outputs D, C, B and A represents a four bit binary number with D as the MSB. Lets assume that all FFs have been cleared to the '0' state. The wave form shown that binary sequence of counting from 0000 to 1111 is followed as clock pulses are continuously applied.

(4) After the NGT (negative Trigger) of the fifteenth clock pulse has occurred, the counter FFs are in the 1111 condition. On the sixteenth NGT, flip flop A goes from 1 to 0, which causes flip flop B goes from 1 to 0, and so on; until the counter is in the 0000 state.

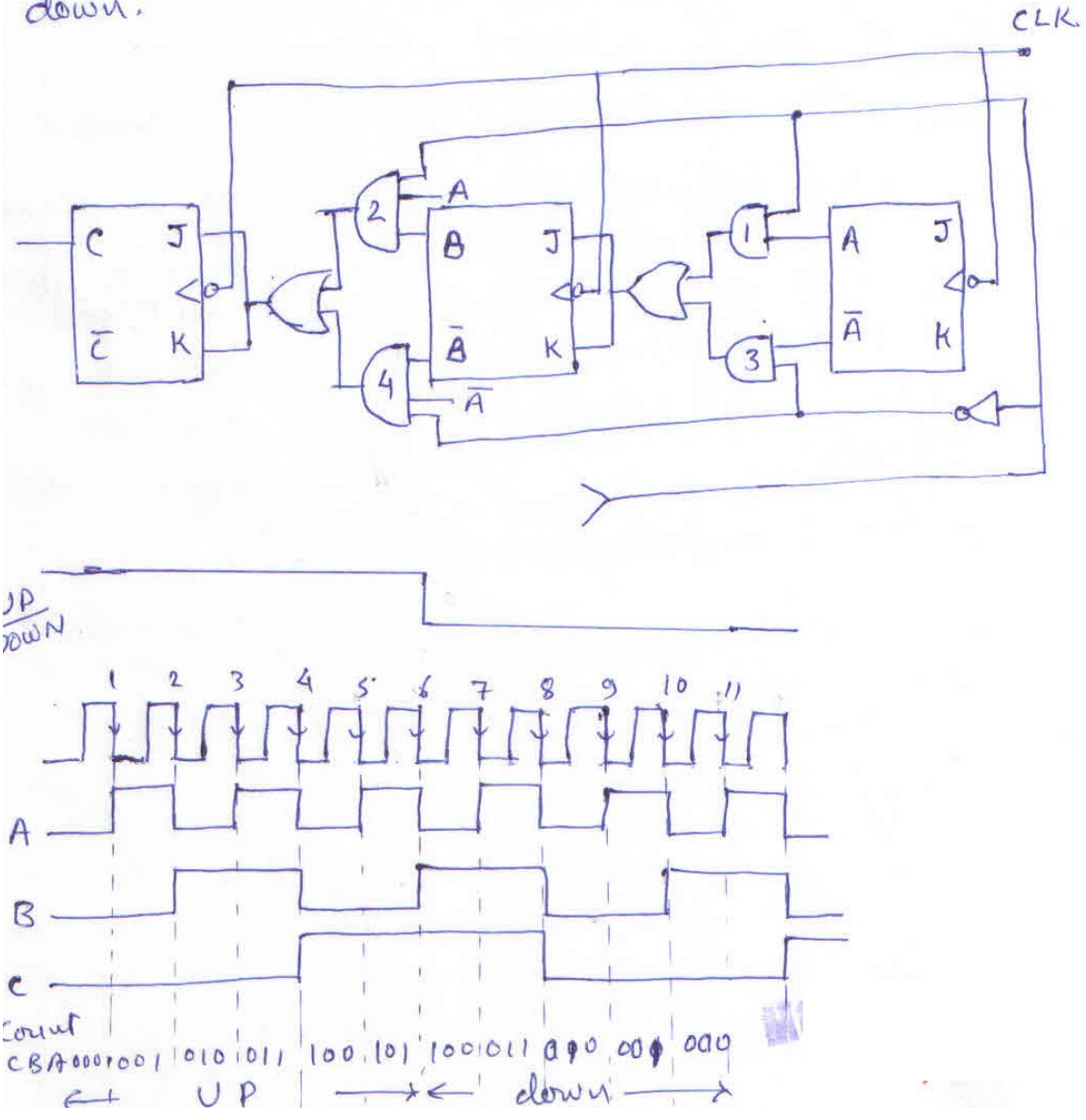
This type of counting arrangement is called Asynchronous counter.

b. Design a mod 8 synchronous up/down counter and explain its working with the help of timing wave form. (8)

Answer:

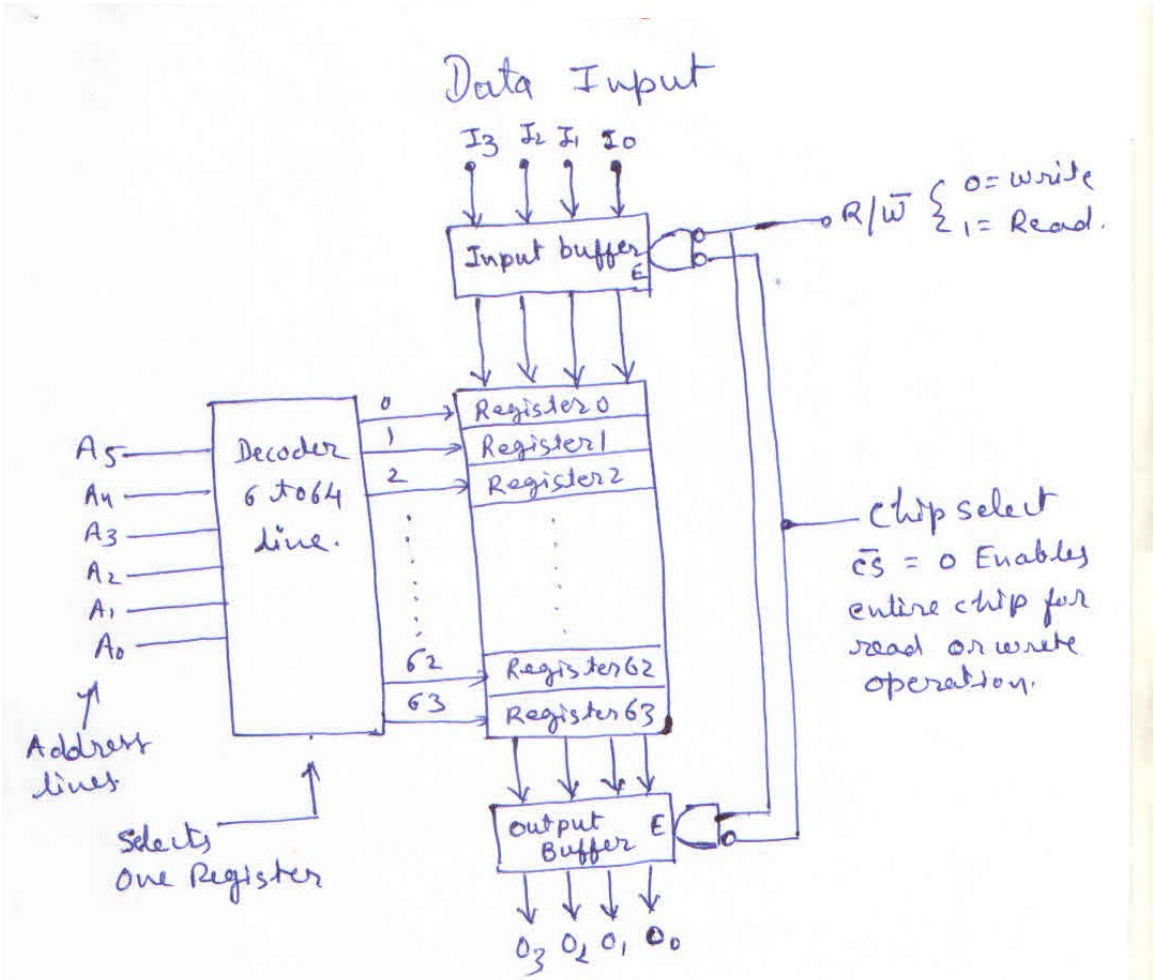
Figur shows a parallel up clown counter. The control input UP/$\overline{\text{DOWN}}$ controls whether the normal FF outputs or the inverted FF outputs are fed to the J and K inputs of the successive FFs. When UP/$\overline{\text{DOWN}}$ is held HIGH, AND gates 1 & 2 are enabled while AND gates 3 and 4 are disabled. This allows the A and B outputs through gates 1 and 2 to the J,K inputs of FFs B and

When UP/$\overline{DOWN}$ is held LOW, AND gates 1 and 2 are disabled while AND gates 3 and 4 are enabled. This allows the A and B outputs through gate 3 and 4 into the J and K inputs of FFs B & C. The The wave forms in the given figure illustrate the operation. Notice that for the first five clock pulses, UP/$\overline{DOWN}$ = 1 and the counter count up; for the last five pulses, UP/DOWN = 0, and the counter counts down.



Q.9 a. Explain with neat diagrams RAM architecture. (8)

Answer:



Figur shows simplified architecture of a RAM that stores 64 words of four bit each. These word have addresses ranging from 0 to 63. In order to select one of the 64 address locations for reading or writing, a binary address code is applied to a decoder circuit. Since $64 = 2^6$, the decoder requires 6 bit Input code. Each address code activates one particular decoder output, which, in tern enable its co-rresponding register. For example, assume an applied Address Code of

$$A_5 A_4 A_3 A_2 A_1 A_0 = 011010$$

Since 011010 = 26, decoder output 26 will go high, register 26 selected for either read or a write operation.

Read operation :- In order to read the contents of the selected register, the READ/WRITE ($R/\bar{W}$) input must be 1 and $\bar{CS}$ input must be activated.

Write operation :- For write operation $R/\bar{W} = 0$ and $\bar{CS} = 0$.

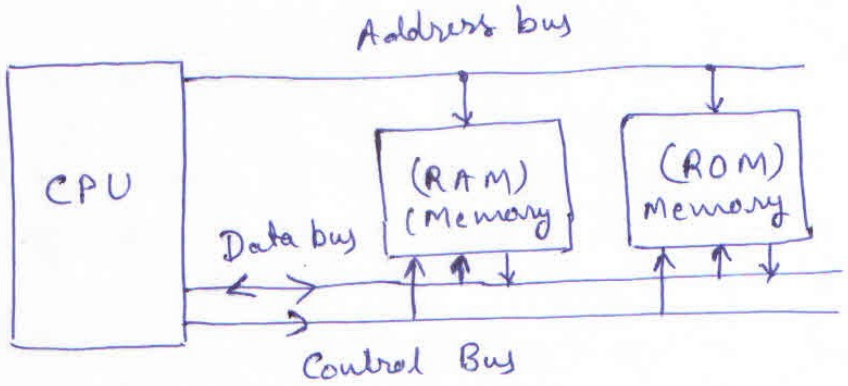
where $\bar{CS}$ = chip select input which used to enable the entire chip or disable it completely.

b. Describe CPU – Memory connection with suitable block diagram. (8)

Answer:

CPU - Memory connection

A computer's main memory is made up of RAM and ROM that are interfaced to the CPU over three groups of signal line or buses, called Address bus, data bus and control bus as shown in figure.



Whenever the CPU wants to write data to a particular memory location, the following steps must occur.

Write Operation

1. The CPU supplies the binary address of memory location where the data are to be stored. It places this address on the address bus lines.
2. The CPU places the data to be stored on the data bus lines.
3. The CPU activates the appropriate control signal lines for the memory write operations.
4. The memory decode the binary address to determine which location is being selected for the store operation.
5. The data on the data bus are transferred to the selected memory location.

Read Operation :-

1. The CPU supplies the binary address of the memory location from which data are to be retrieved. It places this address on the address bus lines.
2. The CPU activates the appropriate control signal for the memory read operation.
3. The memory ICs decode the binary address to determine which location is being selected for the read operation.
4. The memory ICs place data from the selected memory location onto the data bus, from which they are transferred to the CPU.

TEXT BOOK

Digital Systems – Principles and Applications, Ronald J Tocci, Neal S. Wildmer, Gregory L. Moss, Ninth Edition, Pearson Education, 2008