

**Q.2 a. Write down the different levels of integration of IC industry. (4)**

**Answer:**

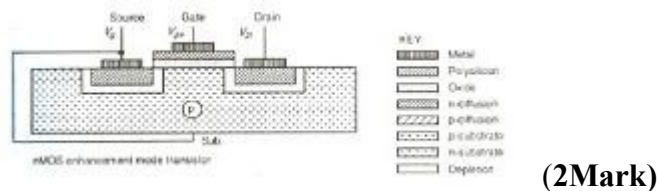
Levels of Integration:-

- i) SSI: - (10-100) transistors => Example: Logic gates
- ii) MSI: - (100-1000) => Example: counters
- iii) LSI: - (1000-20000) => Example: 8-bit chip
- iv) VLSI: - (20000-1000000) => Example: 16 & 32 bit up

**b. With neat sketch explain briefly PMOS & NMOS enhancement mode transistor. (8)**

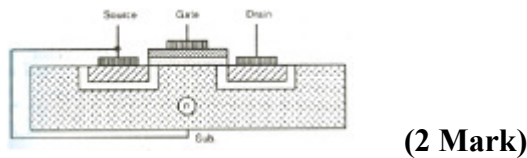
**Answer: N-MOS enhancement mode transistor:-**

This transistor is normally off. This can be made ON by giving a positive gate voltage. By giving a +ve gate voltage a channel of electrons is formed between source drain. (2Mark)



**P-MOS enhancement mode transistor:-**

This is normally on. A Channel of Holes can be performed by giving a -ve gate voltage. In P-Mos current is carried by holes and in N-Mos it's by electrons. Since the mobility is of holes less than that of electrons P-Mos is slower.2 Marks



**c. Enlist the masks sequence in CMOS p-well process. (4)**

**Answer:** Mask sequence.

Mask 1:

Mask 1 defines the areas in which the deep p-well diffusion takes place.

Mask 2:

It defines the thin oxide region (where the thick oxide is to be removed or stripped and thin oxide grown)

Mask 3:

It's used to pattern the polysilicon layer which is deposited after thin oxide. Mask 4: A p+ mask (anded with mask 2) to define areas where p-diffusion is to take place.

Mask 5:

We are using the -ve form of mask 4 (p+ mask) It defines where n-diffusion is to take place.

Mask 6:

Contact cuts are defined using this mask.

Mask 7:

The metal layer pattern is defined by this mask.

Mask 8:

An overall passivation (over glass) is now applied and it also defines openings for accessing pads. (sequence is correct ½ Mark each)

**Q.3 a. Define Stick Diagram. Explain the NMOS encodings in it. (8)**

**Answer:** Stick diagrams may be used to convey layer information through the use of a color code. For example: n-diffusion--green poly--red blue-- metal yellow--implant black--contact areas. (2mark)

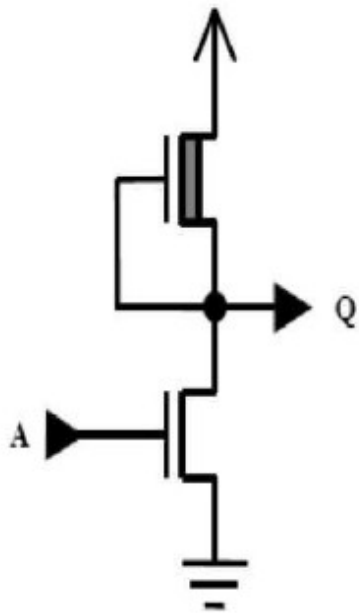
**Encodings for NMOS process:**

| COLOR  | STICK ENCODING  | LAYERS  | MASK LAYOUT ENCODING | CIF LAYER |
|--|-----------------|---|----------------------|-----------|
| GREEN  |                 | n-diffusion (n <sup>+</sup> active)<br>Thin <sub>ox</sub> * |                      | ND        |
| RED  |                 | Polysilicon   |                      | NP        |
| BLUE   |                 | Metal 1   |                      | NM        |
| BLACK  |                 | Contact cut   |                      | NC        |
| GRAY   | NOT APPLICABLE  | Overglass   |                      | NG        |
| nMOS ONLY<br>YELLOW  |                 | Implant   |                      | NI        |
| nMOS ONLY<br>BROWN   |                 | Buried contact  |                      | NB        |
| FEATURE  | FEATURE (STICK) | FEATURE (SYMBOL)  | FEATURE (MASK)       |           |
| n-type enhancement mode transistor                           |                 |   |                      |           |
| Transistor length to width ratio L: W should be shown.       |                 |   |                      |           |
| n-type depletion mode transistor<br>nMOS only                |                 |   |                      |           |
| Source, drain and gate labelling will not normally be shown. |                 |   |                      |           |

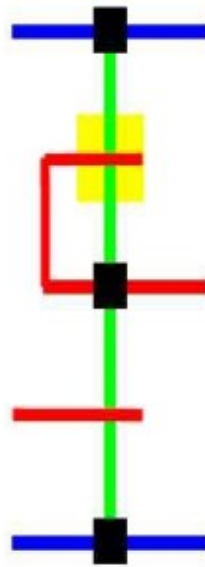
(6 Mark)

**b. Implement schematic, stick diagram and corresponding layout of nMOS depletion load inverter. (8)**

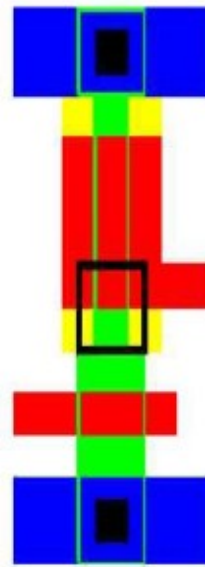
**Answer:**



(2.5 mark)



(2.5 Mark)



(3Mark)

Figure: nMOS depletion load inverter

**Q.4 a. Draw and explain nMOS depletion mode transistor pull-up and transfer characteristics. (8)**

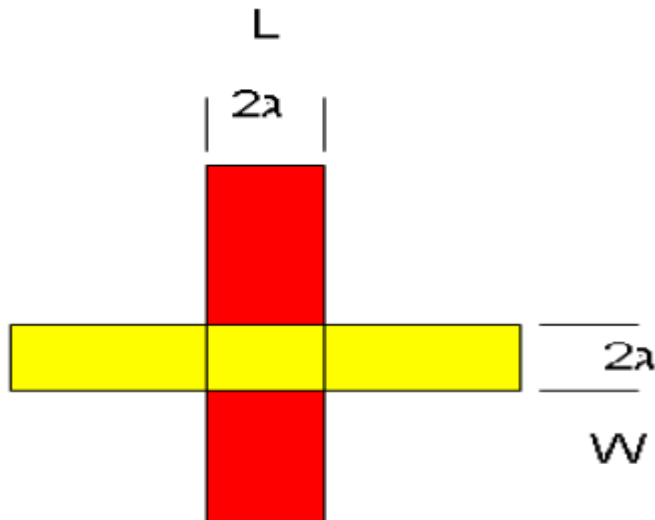
Answer: Text1 – 2.9 – 2 Figure 2.12.(Text :3 Mark, fig: 5 Mark)

**b. Explain the functionality of BiCMOS Drivers. (8)**

Answer: Text1 – 4.8.3 BiCMOS Drivers. (there are three figures in this answer Give 1 Mark to each , give 5 Mark to description )

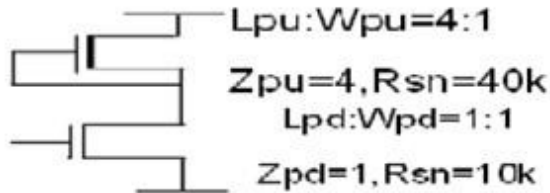
**Q.5 a. Explain the procedure to calculate sheet resistance of MOS transistors. (8)**

Answer:



(2 marks)

The N transistor above is formed by a 2 $\mu$ m wide poly and n diffusion. The L/W ratio is 1. Hence the transistor is a square, therefore the resistance R is  $1\mu\text{m} \times R_s$  ohm/ $\mu\text{m}$  i.e.  $R=1 \times 10^4$ . If L/W ratio is 4 then  $R = 4 \times 10^4$ . If it is a P transistor then for L/W =1, the value of R is  $2.5 \times 10^4$ .



(6 mark)

- b. Define sheet resistance and standard unit of capacitance  $\square C_g$ . Find the static and dynamic resistance of a minimum sized CMOS inverter. (8)

Answer:

- Q.6 a. Explain the Limits of miniaturization and Limits of interconnect and contact resistance. (8)

Answer:

#### Limits of miniaturization

- minimum size of transistor; process tech and physics of the device
- Reduction of geometry; alignment accuracy and resolution
- Size of transistor measured in terms of channel length L
  - $L=2d$  (to prevent push through)
- L determined by  $N_B$  and  $V_{dd}$
- Minimum transit time for an electron to travel from source to drain is

$$V_{drift} = \mu E$$

$$t = \frac{L}{V_{drift}} = \frac{2d}{\mu E}$$

- $v_{s}$  maximum carrier drift velocity is approx.  $V_{sat}$ , regardless of supply voltage (6 mark)

**Limits of interconnect and contact resistance**

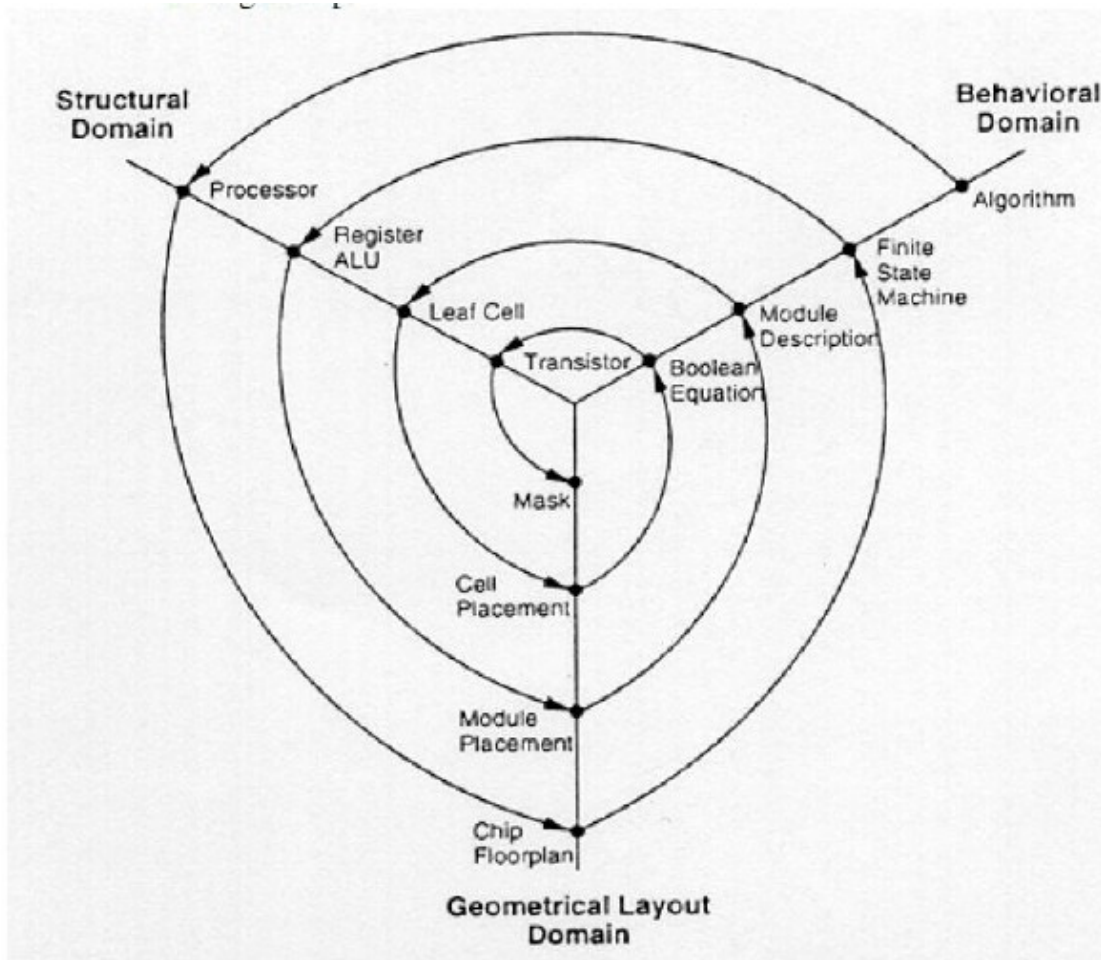
- Short distance interconnect- conductor length is scaled by  $1/\alpha$  and resistance is increased by  $\alpha$
- For constant field scaling, I is scaled by  $1/\alpha$  so that IR drop remains constant as a result of scaling.-driving capability/noise margin.

(2mark)

**b. Draw and explain typical VLSI design flow in three domains (Y –Chart).**

(8)

Answer:



Typical VLSI design flow in three domains(Y-chart)

(fig:

4mark,explanation :4 mark)

**Q.7 a. Enlist the CMOS subsystem design process steps.**

(8)

Answer:

1. Structured design begins with the concept of hierarchy
2. It is possible to divide any complex function into less complex sub functions that is up

to leaf cells

3. Process is known as top-down design

4. As a systems complexity increases, its organization changes as different factors become relevant to its creation

5. Coupling can be used as a measure of how much submodels interact

6. It is crucial that components interacting with high frequency be physically proximate, since one may pay severe penalties for long, high-bandwidth interconnects  
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7. Concurrency should be exploited – it is desirable that all gates on the chip do useful work most of the time

8. Because technology changes so fast, the adaptation to a new process must occur in a short time.

Hence representing a design several approaches are possible. They are:

- Conventional circuit symbols
- Logic symbols
- Stick diagram
- Any mixture of logic symbols and stick diagram that is convenient at a stage
- Mask layouts
- Architectural block diagrams and floor plans

(If the steps are written in correct sequence give 1 mark each step)

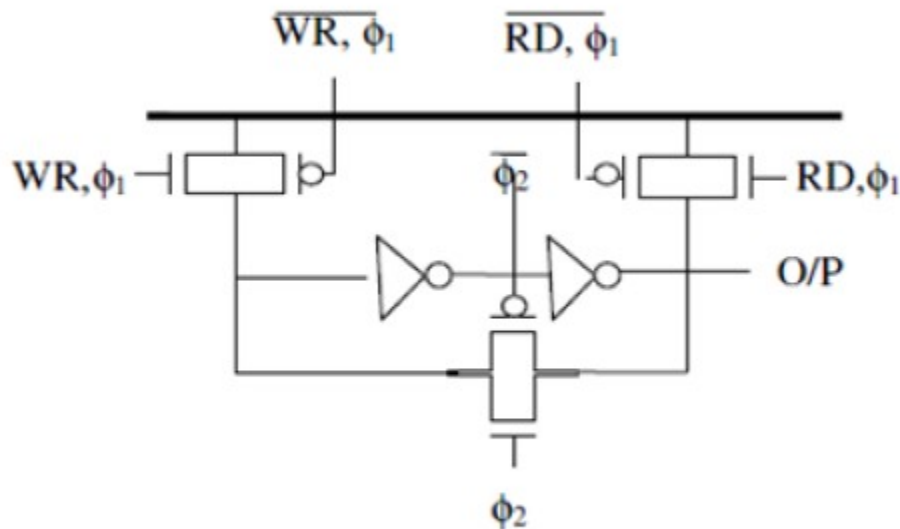
**b. Draw and explain 4-bit ALU functions implementation with an adder. (8)**

Answer: Text1- 8.3.2 , Figure 8.12.

(4mark) (4 mark)

**Q.8 a. Write the circuit of CMOS pseudo static memory cell and explain briefly working of it. (8)**

Answer:



CMOS pseudo-static memory Cell

mark)

(3



**Working**

- dynamic RAM need to be refreshed periodically and hence not convenient
- static RAM needs to be designed to hold data indefinitely
- One way is connect 2 inverter stages with a feedback.
- say  $\phi_2$  to refresh the data every clock cycle
- bit is written on activating the WR line which occurs with  $\phi_1$  of the clock
- bit on Cg of inverter 1 will produce complemented output at inverter 1 and true at output of inverter 2
- at every  $\phi_2$ , stored bit is refreshed through the gated feedback path
- stored bit is held till  $\phi_2$  of clock occurs at time less than the decay time of stored bit
- to read RD along with  $\phi_1$  is activated

**Note:**

- WR and RD must be mutually exclusive
- $\phi_2$  is used for refreshing, hence no data to be read, if so charge sharing effect, leading to destruction of stored bit
- cells must be stackable, both side-by-side & top to bottom
- allow for other bus lines to run through the cell

**(5 mark)**

- b. Explain the optimization of nMOS inverter. (8)**

**Answer:** Text1- 10.1.1.2 – nMOS Inverter.

- Q.9 a. Explain different aspects of CAD Design Tools. (8)**

**Answer:** Text 1 – 10.12. (1.5 marks to each aspect as there are five aspects)

- b. Explain the advantages & disadvantages of implementing BIST include. (8)**

**Answer:**

**TEXT BOOK**

**Basic VLSI Design, Douglas A. Pucknell and Kamran Eshraghian, PHI, 3<sup>rd</sup> Edition, 2007**