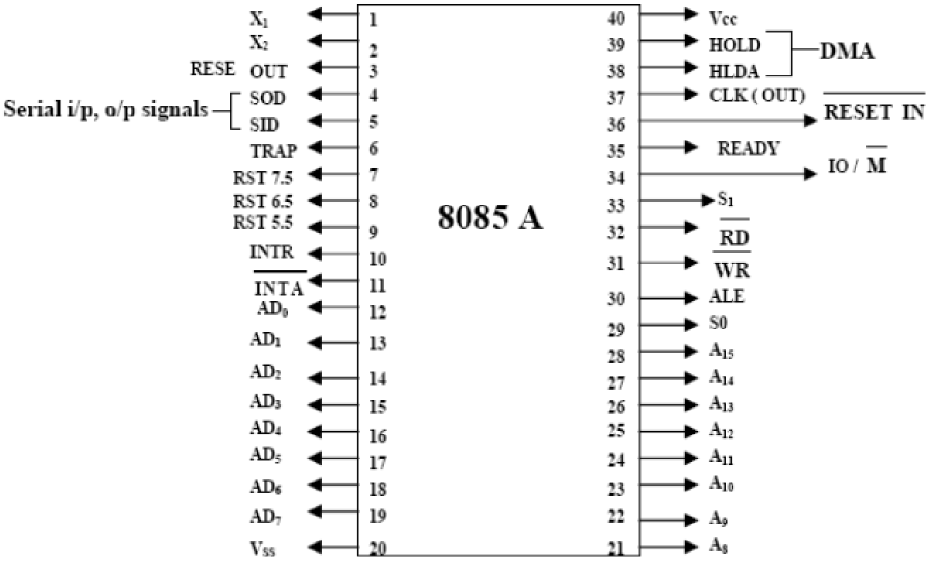
Q2. a **Write the Pin Diagram of the 8085 microprocessor and explain the functions performed by each pin** 10

Ans:



Pin Diagram of 8085

02

A8 - A15

Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/0 address,

AD0 - AD7

Multiplexed Address/Data Bus; Lower 8 bits of the memory address (or I/0 address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus

ALE (Output)

Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on chip latch of peripherals.

SO, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S1	S0	Function
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

RD (Output)

READ: indicates the selected memory or I/0 device is to be read and that the Data Bus is available for the data transfer.

WR (Output)

WRITE: indicates the data on the Data Bus is to be written into the selected memory or I/0 location. Data is set up at the trailing edge of WR.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD: indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request. will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3stated.

HLDA (Output)

HOLD ACKNOWLEDGE: indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycles after HLDA goes low.

INTR (Input)

INTERRUPT REQUEST is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

INTA

INTERRUPT ACKNOWLEDGE: is used instead of (and has the same timing as) RD during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259, Interrupt chip or some other interrupt port.

RESTART INTERRUPTS

These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 ~~ Highest Priority
RST 6.5
RST 5.5 Lowest Priority

TRAP (Input)

Trap interrupt is a non-maskable restart interrupt. It is recognized at the same time As INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

RESET IN (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flipflops. None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X1, X2 (Input)

Crystal or R/C network connections to set the internal clock generator X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/ C network is used as an input to the CPU. The period of CLK is twice the X1, X2 input period.

IO/M (Output)

IO/M indicates whether the Read/Write is to memory or l/O Tristated during Hold and Halt modes.

SID (Input)

Serial input data line The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

Vcc and Vss

+5 volt supply and ground Reference. 8

b. **Explain with suitable examples the 8085 Addressing modes.** 06

Ans: Addressing modes are the manner of specifying effective address. 8085 Addressing mode can be classified into:

1 - Direct addressing mode: the instruction consist of three byte, byte for the opcode of the instruction followed by two bytes represent the address of the operand Low order bits of the address are in byte 2 High order bits of the address are in byte 3

Ex: **LDA 1000h** This instruction load the Accumulator is loaded with the 8-bit content of memory location [1000h]

2 - Register addressing mode The instruction specifies the register or register pair in which the data is located

Ex: **MOV A,C** Here the content of C register is copied to the Accumulator

3 - Register indirect addressing mode The instruction specifies a register pair which contains the memory address where the data is located.

Ex. **MOV M , A** Here the **HL** register pair is used as a pointer to memory location. The content of Accumulator is copied to that location

4- Immediate addressing mode: The instruction contains the data itself. This is either an 8 bit quantity or 16 bit (the LSB first and the MSB is the second)

Ex: **MVI B , FEh and LXI H , 1000h** First instruction loads the Accumulator with the 8-bit immediate data FEh Second instruction loads the **HL** register pair with 16-bit immediate data 1000h

Q3. a **What are the functions performed by these instructions? Explain with example.**

i) **INR M**
ii) **CMA**
iii) **EXHG**
iv) **XRA A**

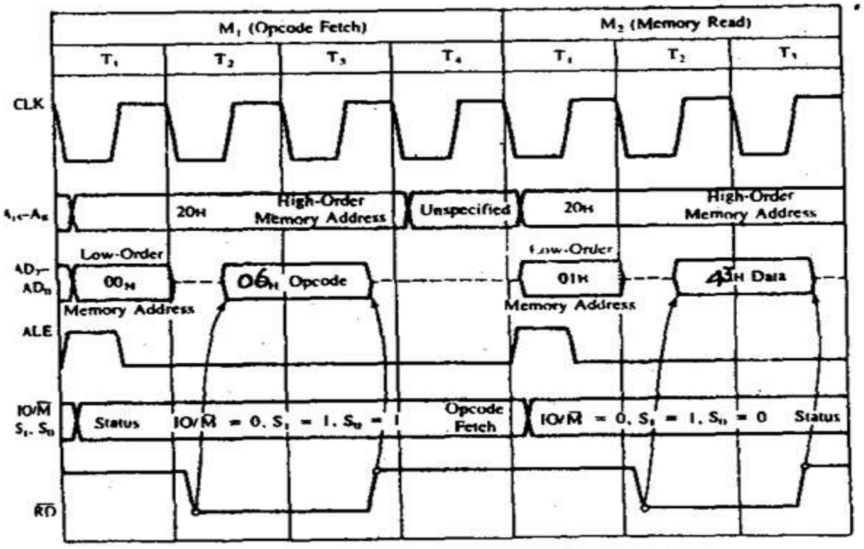
Ans:

i) INR M :The contents of register pair HL will be incremented after the execution of this instruction 02

Ex: Before execution (HL)=1000

After execution of INR M the contents are (HL)=1001

ii) CMA: The contents of Accumulator gets complimented after the execution of this instruction 02

	Ex: Before execution (A)=F0 After execution of CMA the contents become (A)=0F iii) EXHG: The contents of register pair HL and DE gets exchanged after the execution of this instruction Ex: Before execution (HL)=1000 and (DE)=2000 After execution of EXHG the contents are (HL)=2000 and (DE)=1000 iv) XRA A: Ex-or the contents of Accumulator with itself.[Accumulator gets cleared] Ex: Before execution (A)=7E After execution of XRA A the contents are (A)=00	02 02
b. Ans:	**Explain different branching operations performed in 8085** Branching Operations: This group of instructions alters the sequence of program execution either conditionally or unconditionally. **Jump -** Conditional jumps are an important aspect of the decision-making process in the programming. These instructions test for a certain conditions (e.g., Zero or Carry flag) and alter the program sequence when the condition is met. In addition, the instruction set includes an instruction called *unconditional jump.* **Call, Return, and Restart -** These instructions change the sequence of a program either by calling a subroutine or returning from a subroutine. The conditional Call and Return instructions also can test condition flags.	04
c. Ans:	**Write the timing diagram for MVI B, 43H.** Timing diagram for MVI B, 43H. • Fetching the Opcode 06H from the memory 2000H. (OF machine cycle) • Read (move) the data 43H from memory 2001H. (memory read)  M₁ (Opcode Fetch) M₂ (Memory Read) T₁ T₂ T₃ T₄ T₁ T₂ T₃ CLK A₁₅–A₈ 20H High-Order Memory Address Unspecified 20H High-Order Memory Address AD₇–AD₀ Low-Order 00H Memory Address 06H Opcode Low-Order 01H Memory Address 43H Data ALE IO/M̄ S₁, S₀ Status IO/M̄ = 0, S₁ = 1, S₀ = 1 Opcode Fetch IO/M̄ = 0, S₁ = 1, S₀ = 0 Status RD̄	04

Q4.a **Write an Assembly Language Program to exchange N number of data's which are stored starting from Location X with data's which are stored starts at location Y.** 08

Ans: Initialization:
Source at location: LOC X
Destination at location: LOC Y
Counter: N at register B

```
         MIV B, N
         LXIH LOC X
         LXID LOC Y
         MOV C,M
         LDAX, D
LOOP:    MOV M,A
         MOV A,C
         STAX D
         INX H
         INX D
         DCR B
         JNZ LOOP
         HLT
```

b. **Let array of N numbers are stored starting from Location X, write an Assembly Language Program to find the largest number in the array and store the same at location Y.** 08

Ans: Source at location: LOC X
Destination at location: LOC Y
Counter: N at register B

```
         MIV B, N-1
         LXIH LOC X
         MOV A,M
  LOOP:  INX H
         CMP M
         JNC OUT
         MOVA,M
   OUT:  DCR B
         JNZ LOOP
         STA LOCY
         HLT
```

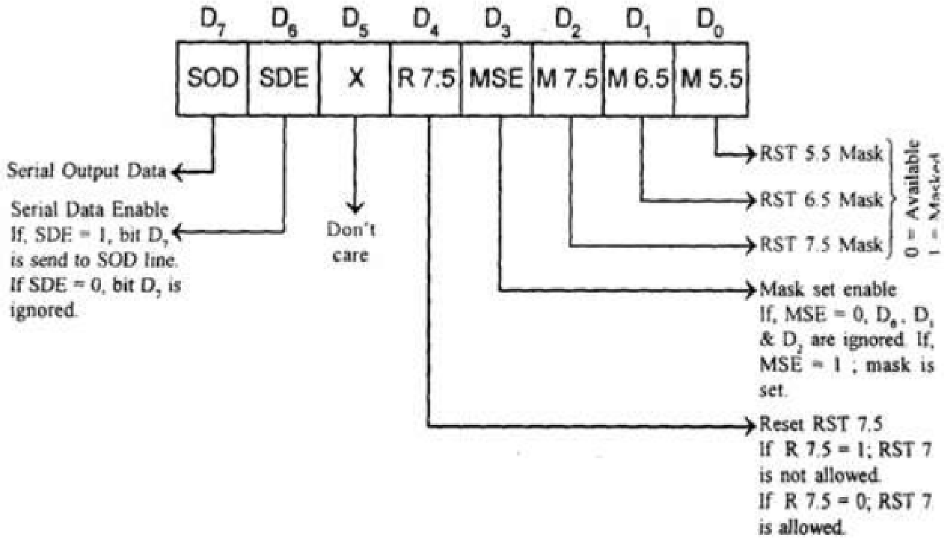
Q5.a **What is an interrupt? Explain the functions performed by SIM and RIM instructions for interrupt operation.** 04 +

04

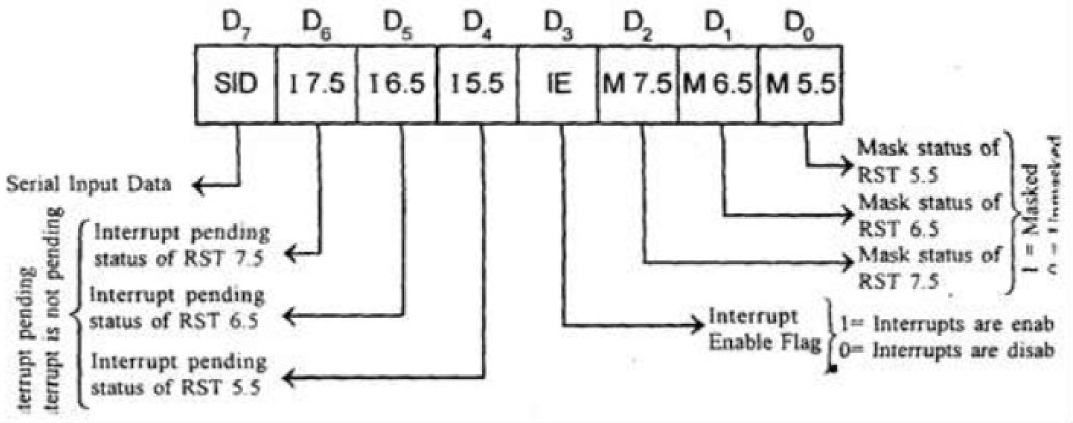
Ans: The 8085 provide additional masking facility for RST 7.5, RST 6.5 and RST 5.5 using SIM instruction.

The status of these interrupts can be read by executing RIM instruction.

The masking or unmasking of RST 7.5, RST 6.5 and RST 5.5 interrupts can be performed by moving an 8-bit data to accumulator and then executing SIM instruction.


D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
SOD
SDE
X
R 7.5
MSE
M 7.5
M 6.5
M 5.5
Serial Output Data
Serial Data Enable If, SDE = 1, bit D_7 is send to SOD line. If SDE = 0, bit D_7 is ignored.
Don't care
RST 5.5 Mask
RST 6.5 Mask
RST 7.5 Mask
0 = Available
1 = Masked
Mask set enable If, MSE = 0, D_0, D_1 & D_2 are ignored. If, MSE = 1 ; mask is set.
Reset RST 7.5 If R 7.5 = 1; RST 7 is not allowed. If R 7.5 = 0; RST 7 is allowed.

The status of pending interrupts can be read from accumulator after executing RIM instruction. When RIM instruction is executed an 8-bit data is loaded in accumulator, which can be interpreted as shown in fig.

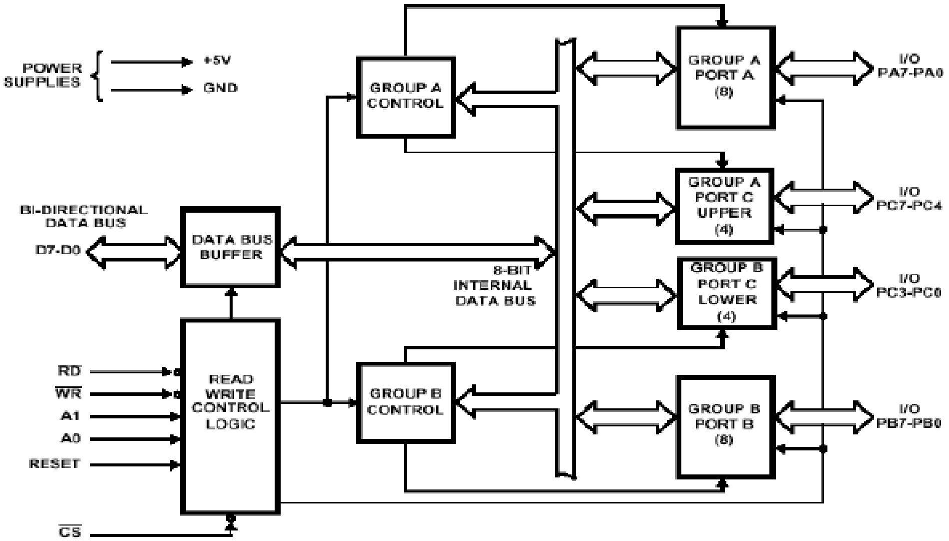


b. **Explain the working of 8255 Programmable Peripheral Interface.** 08

Ans:

- The 8255 has 24 I/O pins that can be grouped primarily into two 8 bit parallel ports: A and B, with the remaining 8 bits as Port C
- The 8 bits of port C can be used as individual bits or be grouped into two 4 bit ports: C Upper (CU) and C Lower (CL).
- The functions of these ports are defined by writing a control word in the control register.
- 8255 can be used in two modes: Bit set/Reset (BSR) mode and I/O mode.

- The BSR mode is used to set or reset the bits in port C.
- The I/O mode is further divided into 3 modes: mode 0, mode 1 and mode 2.
- In mode 0, all ports function as simple I/O ports.
- Mode 1 is a handshake mode whereby Port A and/or Port B use bits from Port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status check and interrupt.
- In mode 2, Port A can be set up for bidirectional data transfer using handshake signals from Port C, and Port B can be set up either in mode 0 or mode 1.



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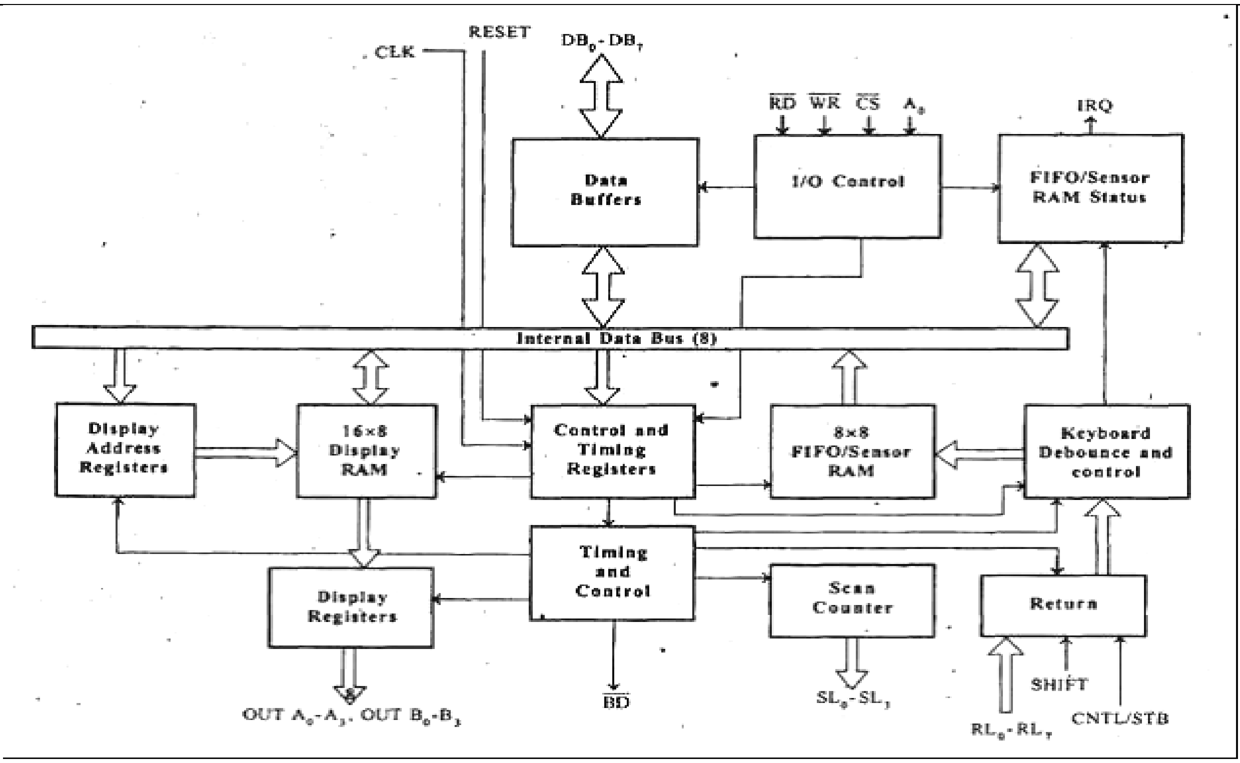
Q6.a **With neat block diagram explain the function performed by Programmable Keyboard/Display Interface – 8279**

Ans: A programmable keyboard and display interfacing chip. Scans and encodes up to a 64-key keyboard. Controls up to a 16-digit numerical display. Keyboard section has a built-in FIFO 8 character buffer. The display is controlled from an internal 16x8 RAM that stores the coded display information. 04

06



Display section:

- The display section has eight output lines divided into two groups A0-A3 and B0-B3.
- The output lines can be used either as a single group of eight lines or as two groups of four lines, in conjunction with the scan lines for a multiplexed display.
- The output lines are connected to the anodes through driver transistor in case of common cathode 7-segment LEDs.
- The cathodes are connected to scan lines through driver transistors.
- The display can be blanked by BD (low) line.
- The display section consists of 16 x 8 display RAM. The CPU can read from or write into any location of the display RAM.

Scan section:

- The scan section has a scan counter and four scan lines, SL0 to SL3.
- In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.
- In encoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output.
- The scan lines are common for keyboard and display.
- The scan lines are used to form the rows of a matrix keyboard and also connected to digit drivers of a multiplexed display, to turn ON/OFF.

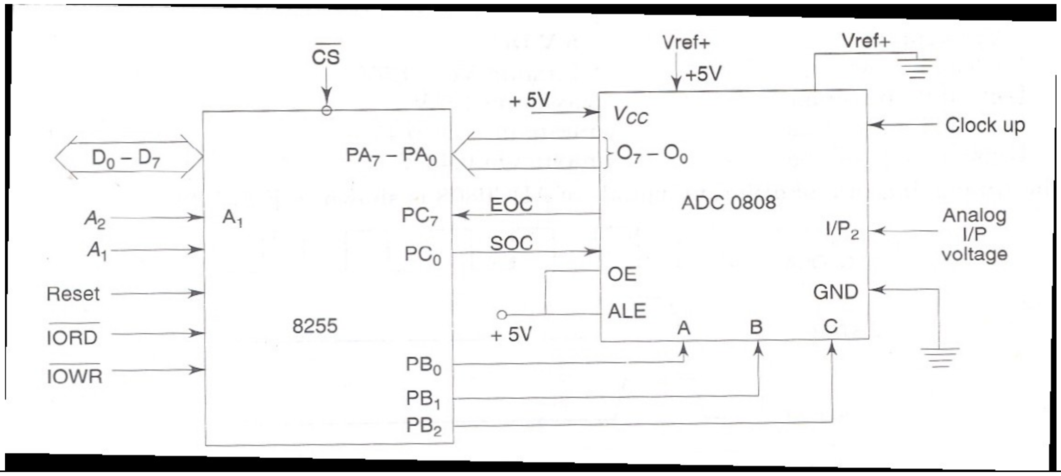
CPU interface section:

- The CPU interface section takes care of data transfer between 8279 and the processor.
- This section has eight bidirectional data lines DB0 to DB7 for data transfer between 8279 and CPU.

- It requires two internal address A =0 for selecting data buffer and A = 1 for selecting control register of8279.
- The control signals WR (low), RD (low), CS (low) and A0 are used for read/write to 8279.
- It has an interrupt request line IRQ, for interrupt driven data transfer with processor.
- The 8279 require an internal clock frequency of 100 kHz. This can be obtained by dividing the input clock by an internal prescaler.
- The RESET signal sets the 8279 in 16-character display with two -key lockout keyboard modes.

B **Explain how an ADC 0808 can be interfaced to microprocessor using 8255.** 06

Ans:



Q7.a **Write the ICW1 (Initialization Command Word One),ICW2,ICW3 and ICW4 of 8259.** 04 x 02

Ans: **ICW1:**

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	A7	A6	A5	1	LITM	ADI	SNGL	IC4

D0 1=ICW4
0=No ICW4
D1 1=Single
0=Cascaded
D2 Call Address Interval
1=Interval of 4 bytes
0=Interval of 8 bytes
D3 1=Level Triggered
0=Edge Triggered

Needed A7-A5 of Interrupt vector address
Needed MCs 80/85 mode only

ICW2:

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	T_7	T_6	T_5	T_4	T_3	A_{10}	A_9	A_8

T7-T3 are A3 – A0 of Interrupt vector address
A10 – A9 , A8 – Selected according to Interrupt request level.
They are not the address lines to microprocessor
A0 – 1 Selects ICW2

ICW3:

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Sn = 1 – IRn Input has a slave
=0 – IRn Input does not have a slave

ICW4:

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

D2 D1 D0 – 000 to 111 for IR0 to IR7 or slave 1 to slave 8

b. **What is DMA? Which are pins of 8085 are used for this operation? Explain the operation performed by DMA Controller 8257.** 08

Ans: DMA means, accessing the memory directly. This is required when bulk of data is transmitting between memory and I/O devices.

HOLD and HLDA pins of 8085 is used for DMA operation.
The *Direct Memory Access* or DMA mode of data transfer is the fastest amongst all the modes of data transfer. In this mode, the device may transfer data directly to/from memory without any interference from the CPU. The device requests the CPU (through a DMA controller) to hold its data, address and control bus, so that the device may transfer data directly to/from memory.
The DMA data transfer is initiated only after receiving HLDA signal from the CPU.
Intel's 8257 is a four channel DMA controller designed to be interfaced with their family of microprocessors. The 8257, on behalf of the devices, requests the CPU for bus access using local bus request input i.e. HOLD in minimum mode. In maximum mode of the microprocessor RQ/GT pin is used as bus request input. On receiving the HLDA signal (in minimum mode) or RQ/GT signal (in maximum mode) from the CPU, the requesting devices gets the access of the bus, and it completes the required number of DMA cycles for the data transfer and then hands over the control of the bus back to the CPU.

Q8.a **Mention different modes of operations of 8253 and explain in detail mode 2 and mode 3 operations.** 02

Ans: The 8253 has six modes of operations.
1. Mode0 (Interrupt on terminal count)
2. Model (Programmable monoshot)
3. Mode2 (Rate generator)
4. Mode3 (Square wave generator)
5.Mode4 (Software Triggered robe)
6.Mode5 (Hardware triggerred strobe)

MODE 2 This mode is called either rate generator or divide by N counter. In 04
this mode, if N is loaded as the count value, then, after N pulses, the output becomes low only for one clock cycle. The count *N* is reloaded and again the output becomes high and remains high for *N* clock pulses. The output is normally high after initialisation or even a low signal on GATE input can force the output high. If GATE goes high, the counter starts counting down from the initial value. The counter generates an active low pulse at the output initially, after the count register is loaded with a count value. Then count down starts and whenever the count becomes zero another active low pulse is generated at the output. The duration of these active low pulses are equal to one clock cycle. The number of input clock pulses between the two low pulses at the output is equal to the count loaded. Figure 1 shows the related waveforms for mode 2. Interestingly, the counting is inhibited when GATE becomes low.

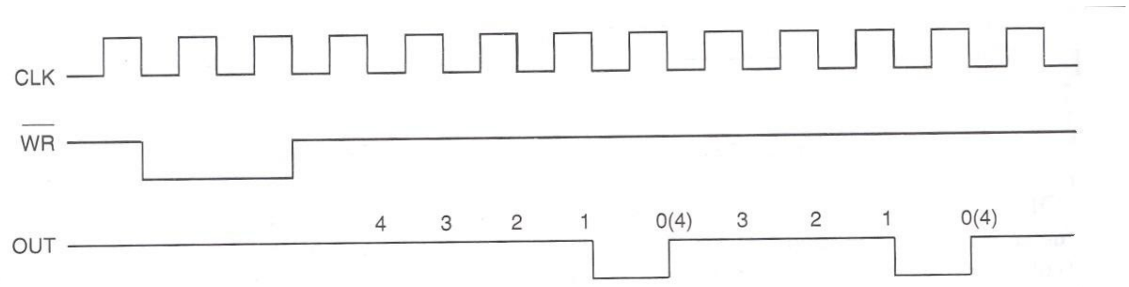


Figure 1: Waveforms at pin WR and OUT in Mode 2

MODE 3 In this mode, the 8253 can be used as a square wave rate generator. In terms of operation this mode is somewhat similar to mode 2. When, the count *N* loaded is even, then for half of the count, the output remains high and for the remaining half it remains low. If the count loaded
is odd, the first clock pulse decrements it by 1 resulting in an even count 04
value (holding the output high). Then the output remains high for half of the new count and goes low for the remaining half. This procedure is

repeated continuously resulting in the generation of a square wave. In case of odd count, the output is high for longer duration and low for shorter duration. The difference of one clock cycle duration between the two periods is due to the initial decrementing of the odd count. The waveforms for mode 3 are shown in Figure 2. In general, if the loaded count value 'N is odd, then for (N+l)/2 pulses the output remains high and for (N-l)/2 pulses it remains low.

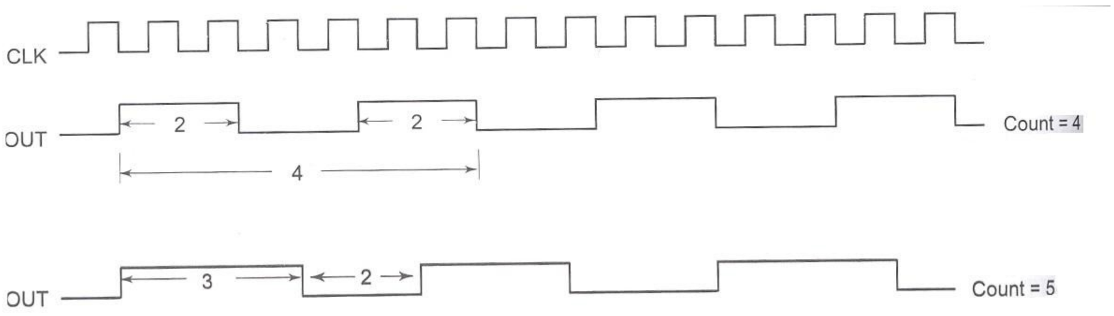


Figure 2: Waveforms for Mode 3

b. **Briefly discuss Asynchronous mode of operation using 8251.** 06

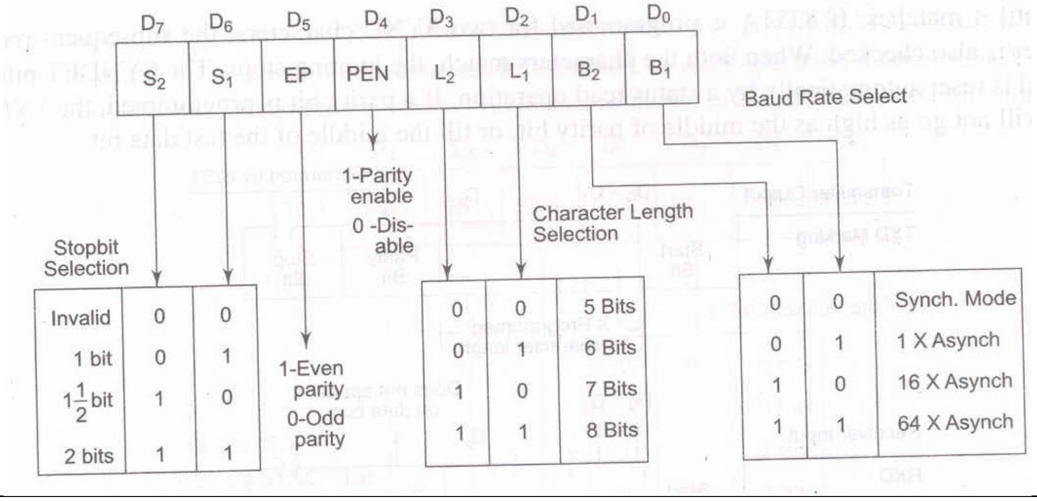
Ans: **Asynchronous Mode (Transmission)**

When a data character is sent to 8251A by the CPU, it adds start bits prior to the serial data bits, followed by optional parity bit and stop bits using the asynchronous mode instruction control word format. This sequence is then transmitted using TXD output pin on the falling edge of TXC.

Asynchronous Mode (Receive)

A falling edge on RXD input line marks a start bit. The receiver requires only one stop bit to mark end of the data bit string, regardless of the stop bit programmed at the transmitting end. The 8-bit character is then loaded into the into parallel I/O buffer of 8251. RXRDY pin is raised high to indicate to the CPU that a character is ready for it. If the previous character has not been read by the CPU, the new character replaces it, and the overrun flag is set indicating that the previous character is lost.

Mode instruction format for Asynchronous mode



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1

Invalid	0	0
1 bit	0	1
$1\frac{1}{2}$ bit	1	0
2 bits	1	1

0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

0	0	Synch. Mode
0	1	1 X Asynch
1	0	16 X Asynch
1	1	64 X Asynch

Q9.a **Explain the architecture of 8051 with neat diagram.** 08

Ans:

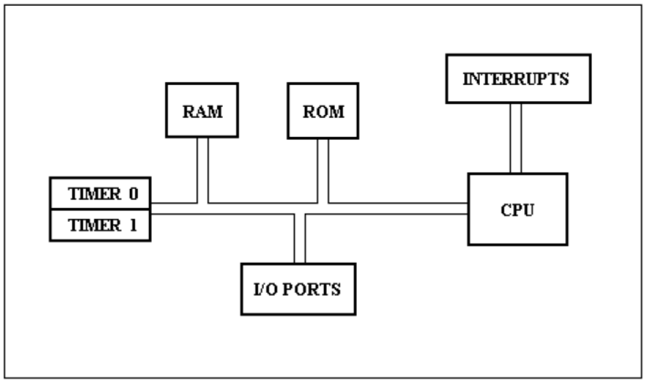


Fig: Architecture of 8051

- **Memory Organization**
  - Logical separation of program and data memory
  - Separate address spaces for Program (ROM) and Data (RAM) Memory
  - Allow Data Memory to be accessed by 8-bit addresses quickly and manipulated by 8-bit CPU
- **Program Memory**
  - -Only be read, not written to
  - -The address space is 16-bit, so maximum of 64K bytes
  - -Up to 4K bytes can be on-chip (internal) of 8051 core
  - -PSEN (Program Store Enable) is used for access to external Program Memory
- **Data Memory**
  - -Includes 128 bytes of on-chip Data Memory which are more easily accessible directly by its instructions
  - -There is also a number of Special Function Registers (SFRs)
  - -Internal Data Memory contains four banks of eight registers and a special 32- byte long segment which is bit addressable by 8051 bit-instructions
  - -External memory of maximum 64K bytes is accessible by “movx”

b **Explain the interrupt structure of 8051.** 08

Ans:

- 8051 provides 4 interrupt sources
  □ 2 external interrupts
  □ 2 timer interrupts
- □ They are controlled via two SFRs, IE and IP
- Each interrupt source can be individually enabled or disabled by setting or clearing a bit in IE (Interrupt Enable). IE also exists a global disable bit, which can be cleared to disable all interrupts at once
- Each interrupt source can also be individually set to one of two priority levels by setting or clearing a bit in IP (Interrupt Priority)
- A low-priority interrupt can be interrupted by high-priority interrupt, but not by another low-priority one

	• A high-priority interrupt cannot be interrupted by any other interrupt source If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced, so within each priority lever there is a second priority structure **External Interrupt** • External interrupts ~INT0 and ~INT1 have two ways of activation • Level-activated • Transition-activated • This depends on bits IT0 and IT1 in TCON • The flags that actually generate these interrupts are bits IE0 and IE1 in TCON • On-chip hardware clears that flag that generated an external interrupt when the service routine is vectored to, but only if the interrupt was transition-activated • When the interrupt is level-activated, then the external requesting source is controlling the request flag, not the on-chip hardware	

TEXT BOOK

I. The 8085 Microprocessor; Architecture, Programming and Interfacing, K. Udaya Kumar and B. S. Umashankar, Pearson Education, 2008