

Q.2 a. Write a note IC's classification. (4)

Answer:

Classification of IC's.
 Linear & Digital
 (Analog)
 Monolithic & ~~Digital~~ Hybrid
Based on level of integration
 SSI, MSI, LSI, VLSI, ASIC etc.
 (Brief explanation) 04

b. Reason out why integrators are preferred over differentiators in analog computers. (2)

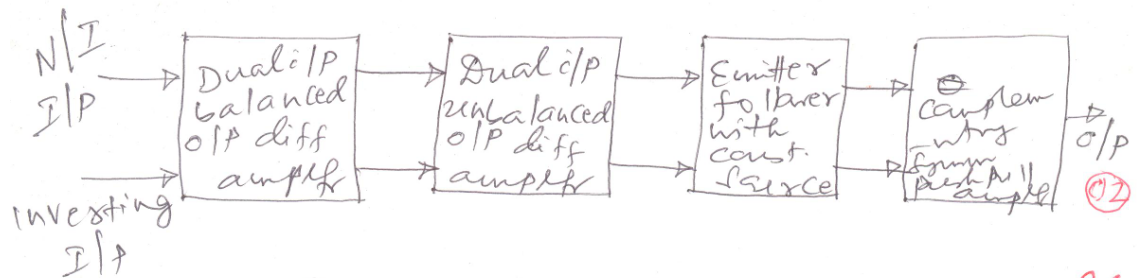
Answer:

The differentiator circuit suffers from the limitations on its stability and noise problems, at high frequencies. Hence differentiators are not preferred in analog computers. 02

c. With the help of a functional block diagram, explain the working of an OPAMP. (6)

Answer:

Functional block diagram of an opamp



Brief explanation 04

- d. An amplifier has a differential gain of 400 and CMRR of 50 dB. If $V_{in1} = 50\text{mV}$, $V_{in2} = 60\text{mV}$ and $V_{noise} = 5\text{mV}$, determine the differential output and common mode output. (4)

Answer:

$$V_o = (V_{i2} - V_{i1}) A_d = (60 - 50) \times 400 \text{ mV} \\ = 4000 \text{ mV}$$

$$\beta = 20 \cdot \log_{10} \frac{A_d}{A_c}$$

$$2.5 = \log \frac{400}{A_c} \Rightarrow A_c = 1.264 \quad 02$$

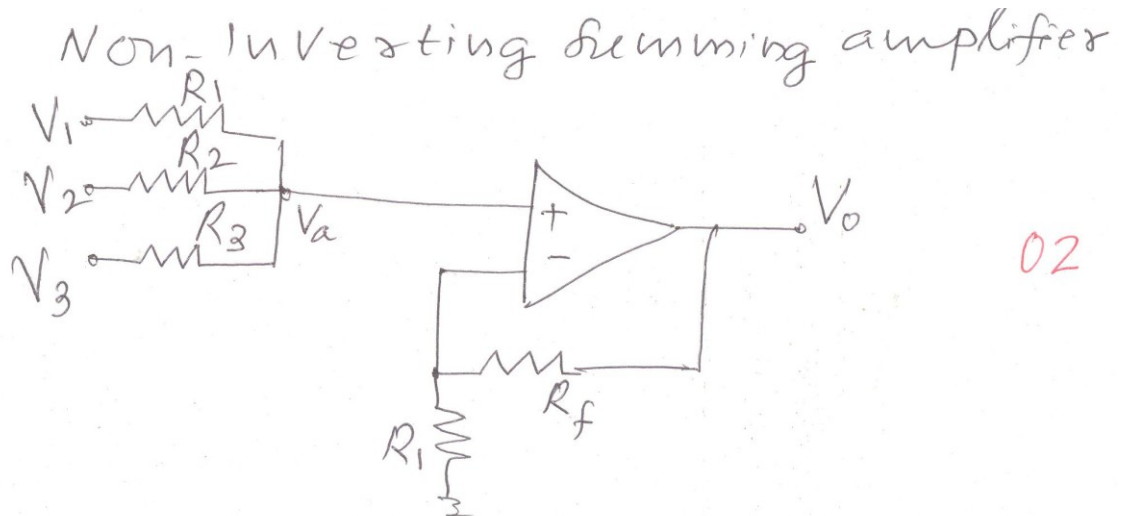
Common Mode output / Noise o/p

$$= (V_{noise}) \times A_c = 5 \text{ mV} \times 1.264$$

$$= 6.32 \text{ mV} \quad 02$$

- Q.3 a. Realize a non-inverting summer using OPAMP. (6)

Answer:



$$\text{Derivation of, } V_o = V_1 + V_2 + V_3 \quad 04$$

b. Discuss about frequency compensation of OPAMPs.

(6)

Answer:

compensation techniques involve reduction of B_{1w} and multiple to single pole. The two methods of compensation are

1. Dominant Pole Compensation
2. Pole Zero

(Brief explanation about both techniques) 06

c. What are the requirements of a good instrumentation amplifier?

(4)

Answer:

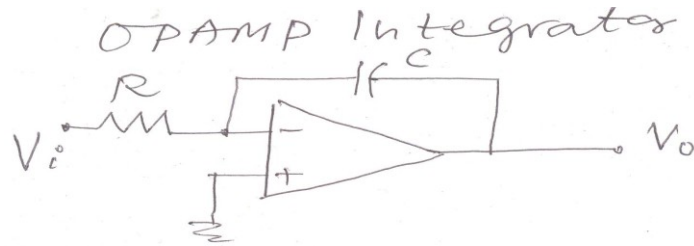
Requirements of a good instrumentation amplifier.

1. Finite, accurate & stable gain
2. Easier gain adjustment
3. High input impedance
4. Low output impedance
5. High CMRR
6. Low power consumption
7. Low thermal & time drifts
8. High slew rate
9. The amplifier must have differential input so that it can be amplified.

04

Q.4 a. With relevant equations show how OPAMP could be used as an integrator. (5)

Answer:

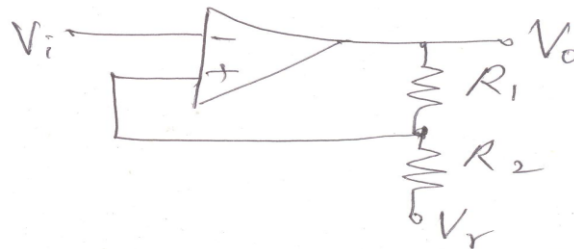


Proof of $V_o = -\frac{1}{RC} \int V_i(t) dt$

b. Design an OPAMP Schmitt trigger for the following specifications. $UTP = 2V$, $LTP = -4V$ and output voltage swings between $\pm 10V$. If the input is $V_i = 5 \sin \omega t$, plot the waveforms of the input and output. (7)

Answer:

OPAMP Schmitt Trigger



$$UTP = V_1 = +V_{o, sat} \frac{R_2}{R_1 + R_2} + V_r \frac{R_1}{R_1 + R_2}$$

$$LTP = V_2 = -V_{o, sat} \frac{R_2}{R_1 + R_2} + V_r \frac{R_1}{R_1 + R_2}$$

$$\text{Hysteresis, } V_H = V_1 - V_2 = 2 - (-4) = 6V$$

$$6 \approx 2V_{o, sat} \frac{R_2}{R_1 + R_2} \Rightarrow \frac{R_2}{R_1 + R_2} = \frac{6}{2 \times 10} = \frac{3}{10}$$

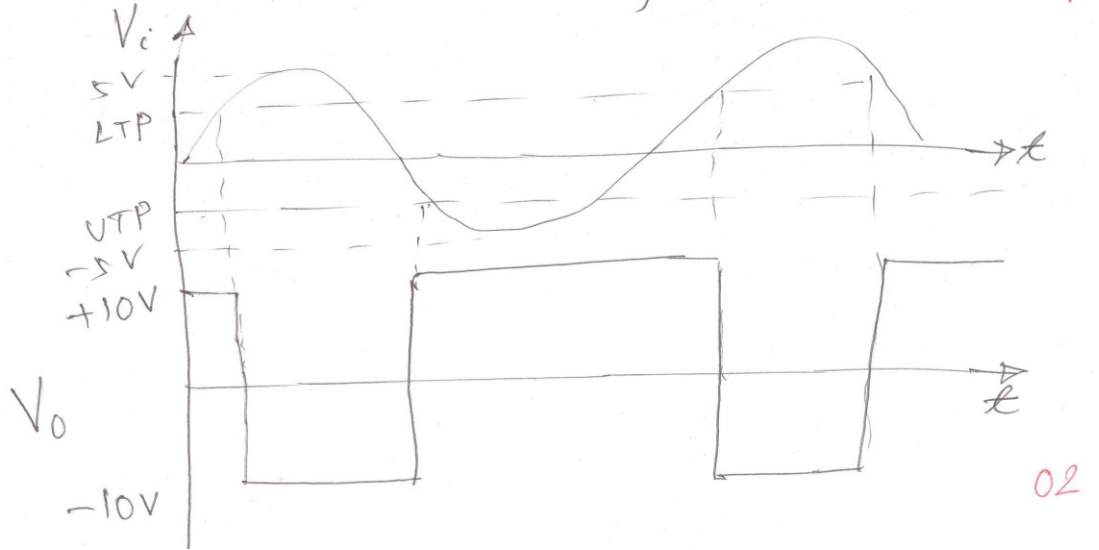
$$\text{or } 3R_1 + 3R_2 = 10R_2 \Rightarrow 3R_1 = 7R_2$$

$$\text{Let } R_1 = 1k, \text{ then } R_2 = \frac{3}{7} \times 1k = 0.428k$$

To find V_{ref} :

$$UTP = V_1 = 2 = V_{0, sat} \frac{R_2}{R_1 + R_2} + V_{ref} \frac{R_1}{R_1 + R_2}$$

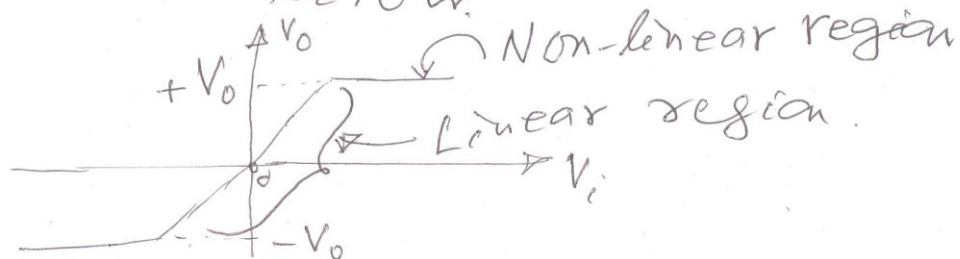
Solving, we get $V_{ref} = 1.42878 \text{ V}$ 04



- c. Differentiate between linear and non-linear operation of OPAMP. Give one example for each. (4)

Answer:

Ideal OPAMP is the ~~linear~~ linear one that the output is directly proportional to the input for all values of the input voltage. The practical OPAMPs have the characteristics shown below.



For a certain range of the input it acts as a linear device otherwise it is a non linear device.

Hence, the OPAMP applications are accordingly classified as linear and non linear.

Example for Linear application:

Adder, subtractor, voltage follower

Example for Non-linear application

comparators, peak detectors.

04

- Q.5 a. Suggest suitable values of resistors and reference voltage for a 4-bit R-2R ladder type DAC, if the resolution required is 0.5 (4)

Answer:

Given $n = 4$, Resolution = 0.5V

Resolution of an n -bit R-2R

$$\text{DAC} = \left(\frac{1}{2^n} \cdot \frac{V_R}{R} \right) R_f$$

Where $V_R = \text{Ref. Voltage}$.

Let $V_R = 10V$

$$\text{Resolution} = \frac{1}{2^n} \times \frac{10}{R} \cdot R_f = 0.5$$

$$= \frac{1}{16} \times \frac{10}{R} \cdot R_f = 0.5$$

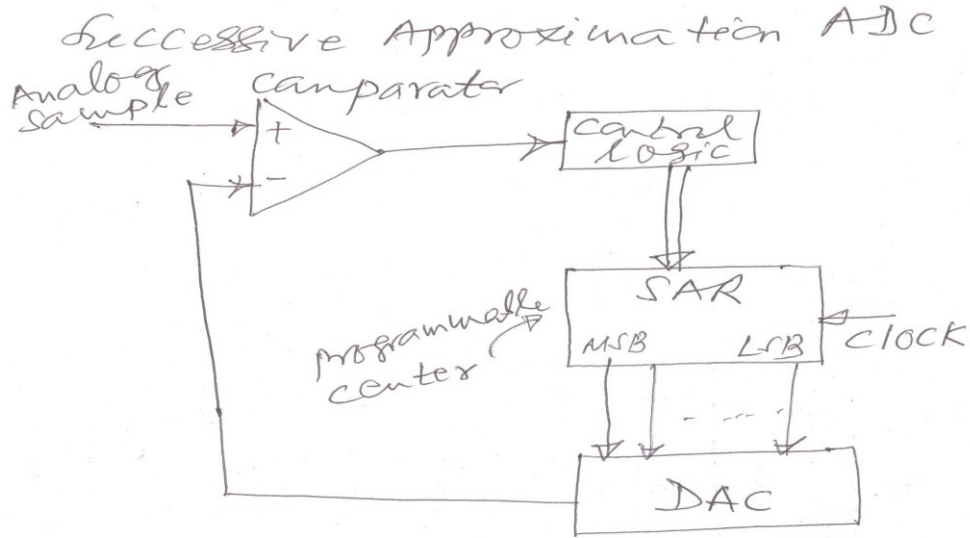
$$\therefore \frac{R}{R_f} = \frac{10}{8} = 1.25$$

If $R_f = 10K$, then $R = 12.5 k\Omega$

04

b. With a neat sketch, explain the working of a successive approximation ADC(6)

Answer:



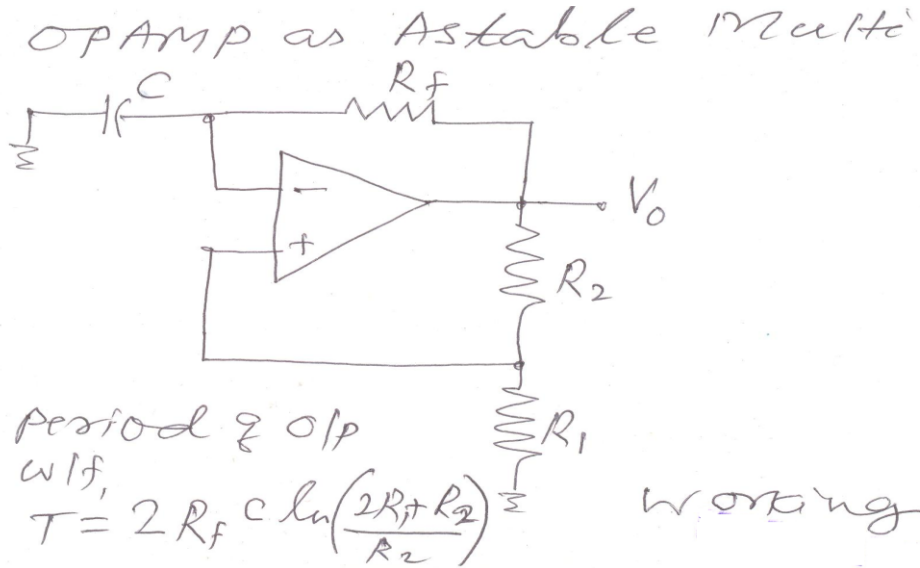
02

Working.

04

c. Discuss how OPAMP could be used as a free running oscillator. (6)

Answer:



02

Working

04

Q.6 a. Discuss the advantages and limitations of digital techniques. (8)
Answer: Refer pages 6 to 8 of Text Book

b. Explain: (8)
(i) BCD code (ii) Alphanumeric codes (8)
Answer: Refer pages 33 to 36 of Text Book

Q.7 a. Perform the following operations:

(i) $(5531)_8 - (3261)_8 + (100)_{10}$

(ii) Find 'x' in $(211)_x = (152)_8$

(4)

Answer:

Convert octal to decimal

(i) $(5531)_8 = (2909)_{10}$

$(3261)_8 = (1713)_{10}$

$(5531)_8 - (3261)_8 + (100)_{10} =$

$= (2909)_{10} - (1713)_{10} + (100) = (1292)_{10}$

02

(ii) $(211)_x = (152)_8$

$2x^2 + x + 1 = 1 \times 8^2 + 5 \times 8 + 2 \times 8^0$
 $= 106$

Solving $x = 7$

02

b. Minimize the following logic function using K-map and implement it using logic gates

$Y(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 7, 8, 9, 10, 11, 12, 14)$

(6)

Answer:

$Y(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 7, 8, 9, 10, 11, 12, 14)$

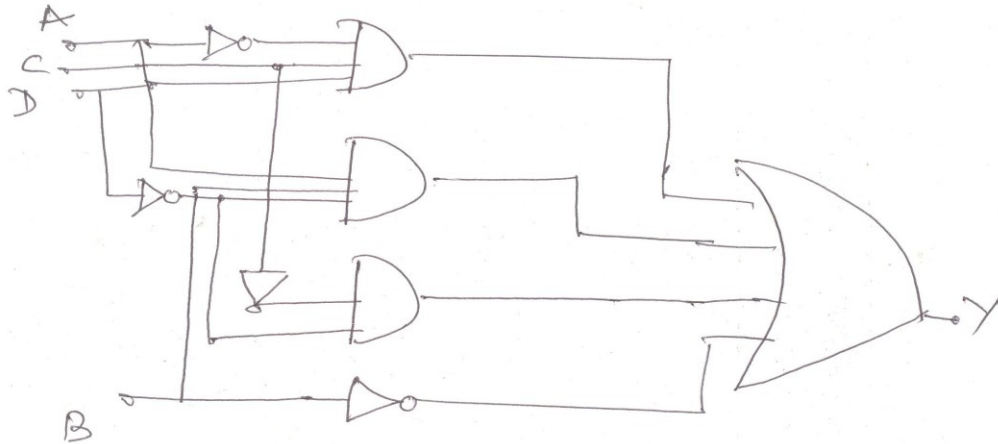
The K-map representation is below

	AB	00	01	11	10
CD	00	1	1	1	1
	01	1			
	11	1	1		
	10	1		1	1

$$\begin{aligned}
 Y &= \bar{B} + \bar{C}\bar{D} + \bar{A}C\bar{D} + AB\bar{D} \\
 &= \bar{A}C\bar{D} + A\bar{D} + \bar{C}\bar{D} + \bar{B}
 \end{aligned}$$

04

The realization is



02

c. Realize a full subtractor using two half subtractors.

(6)

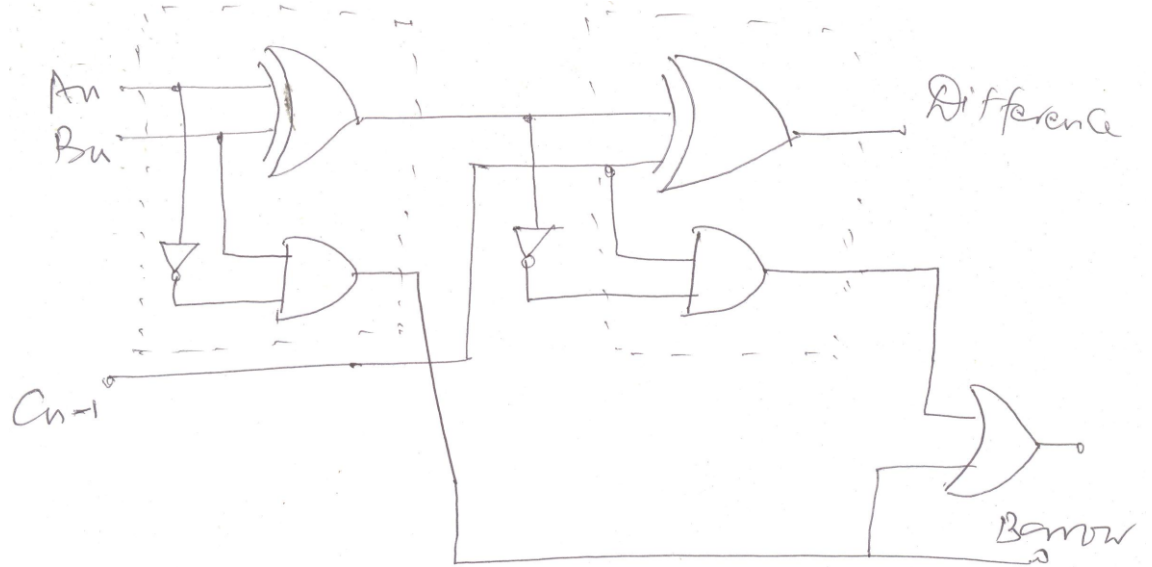
Answer:

Full subtractor from half subtractors
The general equations are:

$$D_{n+1} = A_n \oplus B_n, \quad C_{n+1} = \bar{A}_n \cdot B_n$$

↑ Difference, ↑ carry.

The circuit is as below,



(with proper realization eqns)

06

Q.8 a. Implement a half adder using multiplexers.

(6)

Answer:

Truth table for a half adder

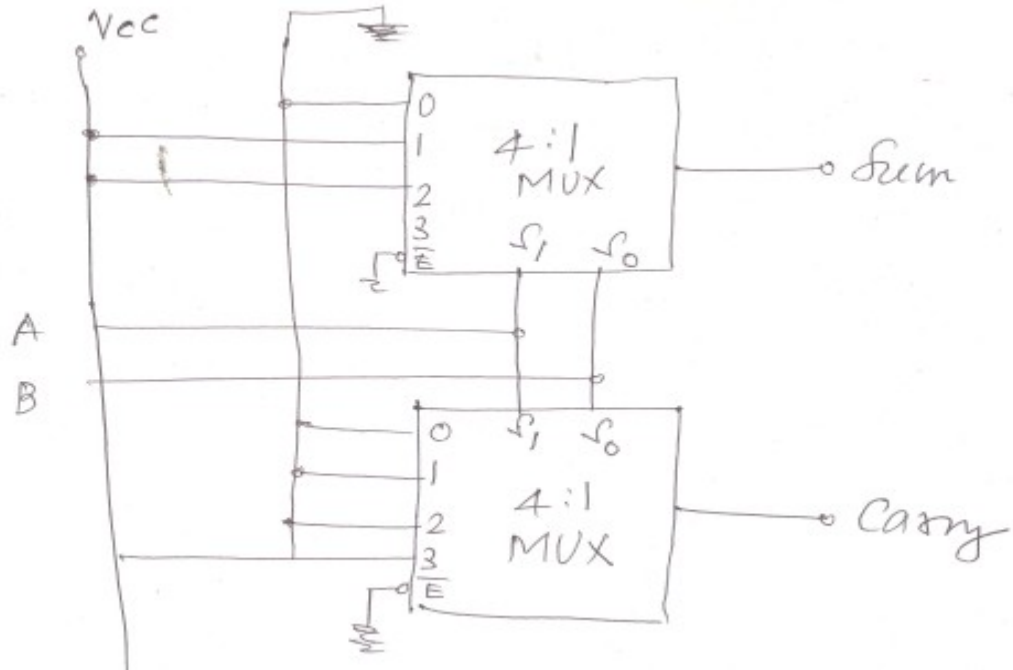
Inputs		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{Sum} = \sum m(1, 2)$$

$$\text{Carry} = \sum m(3)$$

circuit is shown next page

Using two 4:1 MUX

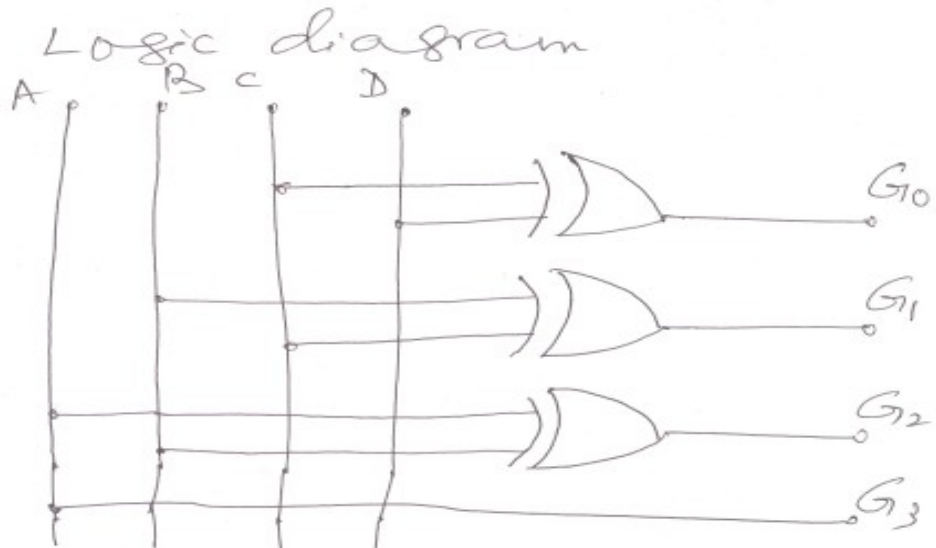


06

- b. Design an edge-triggered J-K flip-flop using NAND, OR gates. Explain its operation for positive edge triggering. (10)

Answer:

Design of Binary to Gray Converter
 Truth table 02
 Simplification of Boolean equations. 06



02

Q.9 a. What is race around condition and how it is eliminated?

(4)

Answer:

Race around condition

explanation

02

Remedy: Master slave flip flop

02

b. Compare synchronous and asynchronous counters. Find the maximum frequency of a clock pulse at which the 4-bit ripple counter operates reliably. Assume delay of the flip-flops as 40 ns and the pulse width of strobe signal is 25 ns. (6)

Answer:

In ripple (asynchronous counters), output of one flip flop is connected to the clock input of the next stage. Hence the delay accumulates. Hence speed is less.

In synchronous counters, clock is applied to all the flip flops of the counter simultaneously and hence increases the speed of operation.

Synchronous counters are faster

03

Problem:

$$N=4, t_d = 40 \text{ ns}, T_s = 25 \text{ ns.}$$

$$f \leq \frac{1}{N(t_d) + T_s}$$

$$\leq \frac{1}{4(40 \times 10^{-9}) + 25 \times 10^{-9}}$$

$$\leq 5.4 \text{ MHz}$$

$$\therefore f_{\max} = 5.4 \text{ MHz.}$$

03

c. Discuss how shift registers could be used for the following applications:

- (i) SIPO
- (ii) Ring Counter
- (iii) Sequence generator

(6)

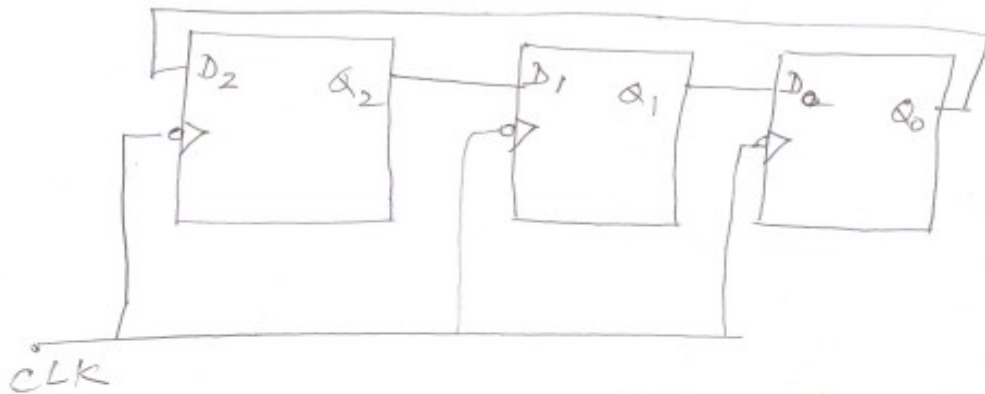
Answer:

S/P Converter

The SIPO shift register is used to convert serial data in parallel form. Consider the size of the word is 8 bits. The 8-bit SIPO shift register receives the data bit by bit with clock pulse. At the end of 8th clock pulse, the 8-bit data is available over the eight output lines of the shift register.

02

(ii) Ring Counter

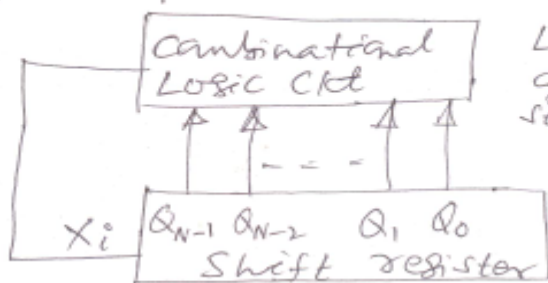


It is a SIPO shift register configuration. output Q_0 of the last flip flop is connected to the D_1 of the first flip flop.

CLK	X_i	Q_2	Q_1	Q_0
0	0	1	0	0
1	1	0	0	0
2	0	1	0	0

02

(iii) Sequence Generator



Logic Ckt that generates a defined sequence generator. These sequences are used in communication.

02

TEXT BOOKS

- I. Linear Integrated Circuits, Revised Second Edition, D Roy Choudhury, Shail B. Jain, New Age International Publishers
- II. Digital Systems – Principles and Applications, Ninth Edition, Ronald J Tocci, Neal S Widmer and Gregory L. Moss, Pearson Education, 2008