Solution	Marks
Q.2 a. Derive & Explain Maximum Power Transform theorem. **Answer:**	**Marking Scheme is available at the end.**

In many practical situations, a circuit is designed to provide power to a load. While for electric utilities, minimizing power losses in the process of transmission and distribution is critical for efficiency and economic reasons, there are other applications in areas such as communications where it is desirable to maximize the power delivered to a load. We now address the problem of delivering the maximum power to a load when given a system with known internal losses. It should be noted that this will result in significant internal losses greater than or equal to the power delivered to the load.

The Thevenin equivalent is useful in finding the maximum power a linear circuit can deliver to a load. We assume that we can adjust the load resistance R_L. If the entire circuit is replaced by its Thevenin equivalent except for the load, as shown in Fig. 4.48, the power delivered to the load is

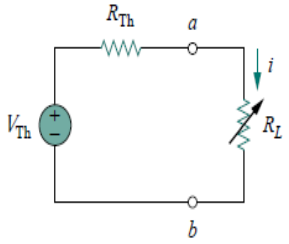


Figure 4.48 The circuit used for maximum power transfer.

$$p = i^2 R_L = \left(\frac{V_{Th}}{R_{Th} + R_L}\right)^2 R_L \qquad (4.21)$$

For a given circuit, V_{Th} and R_{Th} are fixed. By varying the load resistance R_L, the power delivered to the load varies as sketched in Fig. 4.49. We notice from Fig. 4.49 that the power is small for small or large values of R_L but maximum for some value of R_L between 0 and ∞. We now want to show that this maximum power occurs when R_L is equal to R_{Th}. This is known as the *maximum power theorem*.

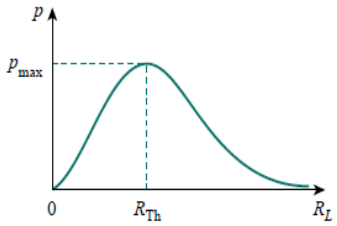


Figure 4.49 Power delivered to the load as a function of R_L.

> Maximum power is transferred to the load when the load resistance equals the Thevenin resistance as seen from the load ($R_L = R_{Th}$).

To prove the maximum power transfer theorem, we differentiate p in Eq. (4.21) with respect to R_L and set the result equal to zero. We obtain

$$\frac{dp}{dR_L} = V_{Th}^2 \left[\frac{(R_{Th} + R_L)^2 - 2R_L(R_{Th} + R_L)}{(R_{Th} + R_L)^4}\right]$$

$$= V_{Th}^2 \left[\frac{(R_{Th} + R_L - 2R_L)}{(R_{Th} + R_L)^3}\right] = 0$$

This implies that

$$0 = (R_{\text{Th}} + R_L - 2R_L) = (R_{\text{Th}} - R_L) \tag{4.22}$$

which yields

$$\boxed{R_L = R_{\text{Th}}} \tag{4.23}$$

showing that the maximum power transfer takes place when the load resistance R_L equals the Thevenin resistance R_{Th}. We can readily confirm that Eq. (4.23) gives the maximum power by showing that $d^2p/dR_L^2 < 0$.

The source and load are said to be *matched* when $R_L = R_{\text{Th}}$.

The maximum power transferred is obtained by substituting Eq. (4.23) into Eq. (4.21), for

$$\boxed{p_{\max} = \frac{V_{\text{Th}}^2}{4R_{\text{Th}}}} \tag{4.24}$$

Equation (4.24) applies only when $R_L = R_{\text{Th}}$. When $R_L \neq R_{\text{Th}}$, we compute the power delivered to the load using Eq. (4.21).

Q.2 b. Find i_o in the circuit in Fig. using superposition Theorem.

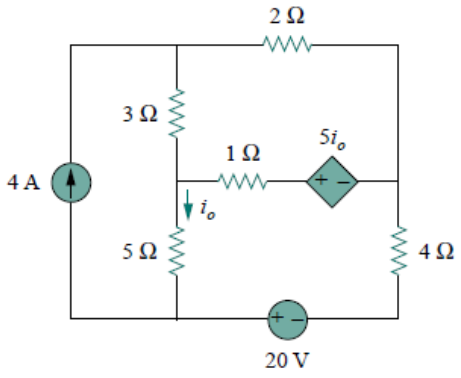


Fig.2

Answer:

The circuit in Fig. 4.9 involves a dependent source, which must be left intact. We let

$$i_o = i_o' + i_o'' \tag{4.4.1}$$

where i_o' and i_o'' are due to the 4-A current source and 20-V voltage source respectively. To obtain i_o', we turn off the 20-V source so that we have the circuit in Fig. 4.10(a). We apply mesh analysis in order to obtain i_o'. For loop 1,

$$i_1 = 4 \text{ A} \tag{4.4.2}$$

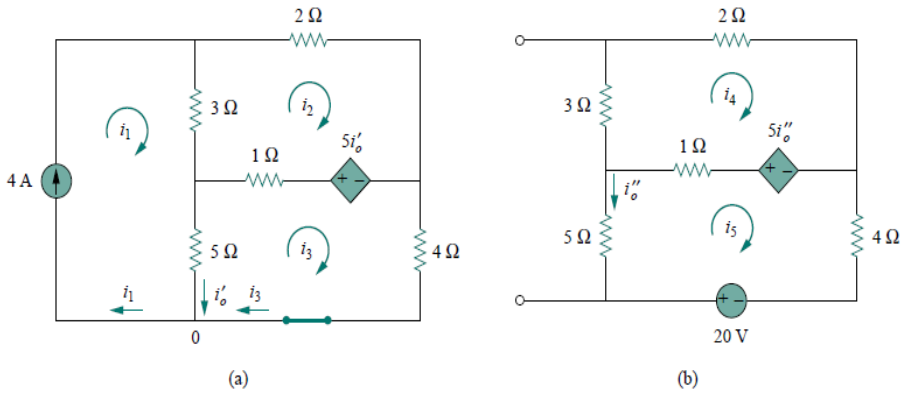


Figure 4.10 For Example 4.4: Applying superposition to (a) obtain i'_0, (b) obtain i''_0.

For loop 2,

$$-3i_1 + 6i_2 - 1i_3 - 5i'_o = 0 \qquad (4.4.3)$$

For loop 3,

$$-5i_1 - 1i_2 + 10i_3 + 5i'_o = 0 \qquad (4.4.4)$$

But at node 0,

$$i_3 = i_1 - i'_o = 4 - i'_o \qquad (4.4.5)$$

Substituting Eqs. (4.4.2) and (4.4.5) into Eqs. (4.4.3) and (4.4.4) gives two simultaneous equations

$$3i_2 - 2i'_o = 8 \qquad (4.4.6)$$

$$i_2 + 5i'_o = 20 \qquad (4.4.7)$$

which can be solved to get

$$i'_o = \frac{52}{17}\ \text{A} \qquad (4.4.8)$$

To obtain i''_o, we turn off the 4-A current source so that the circuit becomes that shown in Fig. 4.10(b). For loop 4, KVL gives

$$6i_4 - i_5 - 5i''_o = 0 \qquad (4.4.9)$$

and for loop 5,

$$-i_4 + 10i_5 - 20 + 5i''_o = 0 \qquad (4.4.10)$$

But $i_5 = -i''_o$. Substituting this in Eqs. (4.4.9) and (4.4.10) gives

$$6i_4 - 4i''_o = 0 \qquad (4.4.11)$$

$$i_4 + 5i''_o = -20 \qquad (4.4.12)$$

which we solve to get

$$i_o'' = -\frac{60}{17}\ \text{A} \qquad (4.4.13)$$

Now substituting Eqs. (4.4.8) and (4.4.13) into Eq. (4.4.1) gives

$$i_o = -\frac{8}{17} = -0.4706\ \text{A}$$

Q.3 a. Explain Zener diode as a voltage regulator.

Answer: page 23, Chapter 1, Electronic Devices & Circuits By I. J. NAGRATH

DC power in electronic circuits is provided by rectifiers (which convert ac to dc; to be discussed in Section 1.14) whose dc voltage increases as load reduces. To counteract this voltage rise and so as to achieve a nearly constant load voltage, a series resistance R_S and a shunt connected Zener diode are used as shown in the circuit diagram of Figure 1.28. As the load (current) reduces, the source (rectifier output) voltage V_S rises and so does the load voltage $V_L > V_Z$) which causes the Zener diode current I_Z to increase which in turn increases the voltage drop in R_S counteracting rise in V_S. This achieves a load voltage regulation which is much smaller than the supply (V_S) voltage regulation.

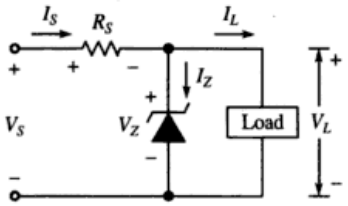


FIGURE 1.28 Circuit with Zener diode.

Q.3 b. A Bridge rectifier uses four identical diodes of forward resistance of 5 Ω each. It is supplied from a transformer with output voltage of 20 volt (rms) and secondary winding resistance of 10 Ω. Calculate
(i) Output dc voltage at a dc load current of 100 m Amp.
(ii) percentage regulation for a full load dc current of 200 m Amp.
(iii) RMS value of output voltage at a dc load current of 200 m Amp.
(iv) RMS value of ac component of voltage in part (iii).

Answer:

(a) $V_{dc}(100\ \text{mA}) = \frac{2V_m}{\pi} - I_{dc}(R_S + 2R_F) = \frac{2\sqrt{2}\times 20}{\pi} - 100\times 10^{-3}\times(10+10)$
$= 16\ \text{V}$

(b) $V_{dc}\ (200\ \text{mA}) = \frac{2\sqrt{2}\times 20}{\pi} - 200\times 10^{-3}\times(10+10) = 14\ \text{V}\ (= V_{L\,dc})$

$R_L = \frac{V_{dc}}{I_{dc}} = \frac{14}{200\times 10^{-3}} = 70\ \Omega$

$\%\ \text{Regulation} = \left(\frac{2R_F + R_S}{R_L}\right)\times 100 = \left(\frac{10+10}{70}\right)\times 100 = 28.57$

(c) $I_m = \frac{\pi I_{dc}}{2} = \frac{\pi\times 200}{2} = 314\ \text{mA}$

$I_{L\,rms} = \frac{314}{\sqrt{2}} = 222\ \text{mA}$

$V_{L\,rms} = I_{L\,rms}\times R_L = 0.222\times 70 = 15.5\ \text{V}$

(d) $(V_{L\,rms})^2 = (V_{L\,ac\,rms})^2 + (V_{L\,dc})^2$
Substituting values, we get

$V_{L\,ac\,rms} = 6.65\ \text{V}$

Q.4 a. Explain the need of biasing in Transistor circuit and describe self bias technique.

Answer:

SELF BIAS OR EMITTER BIAS CIRCUIT:

In the fixed bias circuit, since I_C increases with temperature, and I_B is fixed, operating point changes. In collector to base bias circuit, though I_C changes with temperature, I_B also changes to keep operating point fixed. But since β changes with temp. and I_C depends on β, the assumption has to be made that $\beta R_C >> R_B$ to make I_C independent of β. But if in one circuit, R_C is small, the above assumption will not hold good. [In transformer coupled circuits R_C will be small].

So collector to base circuit is as bad as fixed bias circuit. A circuit which can be used even if there is zero DC resistance in series with the collector terminal, is the ***Self Bias on Emitter Bias Circuit***. The circuit is as shown. This circuit is also known as ***Voltage Divider Bias or Universal Bias Circuit.***

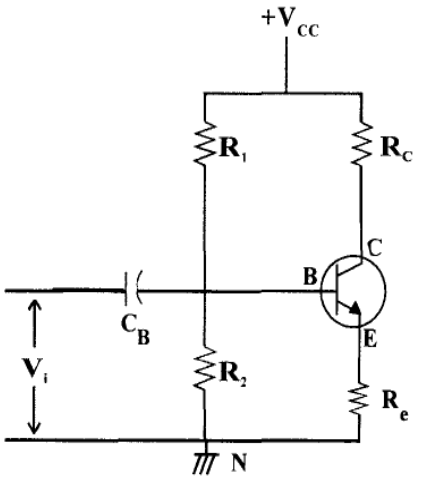


Fig 5.7 Self Bias circuit.

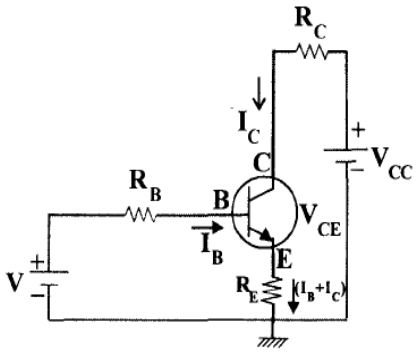


Fig 5.8 Thevenin's equivalent.

The current in the emitter lead causes a voltage drop across R_e in such a direction, that it forward biases the emitter-base junction. It is NPN transistor emitter is *n-type*. Negative polarity should be at the emitter. If I_C increases due to increase in I_{CO} with temperature the current in R_C also increases.

$$I = I_C + I_B;\ V_{BE} = V_{BN} - V_{EN}$$

As I_B increases, I_C also increases.

So current I or emitter current increases. Therefore IR_e drop increases. Since the polarity of this voltage is to reverse bias the E – B junction, I_B decrease. Therefore I_C will increase less than it would have been, had there been no self biasing resistor.

[The voltage drop across R_C provides the self bias for the emitter]. Hence stability is good.

With reference to Fig. 5.8, it is NPN transistor. So the conventional current is flowing out of the transistor, from the emitter. That is why the symbol is with arrow mark pointing outwards. So emitter point is at positive with respect to N. Hence the drop $(I_B + I_C) R_C$ has the polarity such as to reverse bias or to oppose the forward bias voltage V_{BE} junction. R_B can be regarded as parallel combination of R_1 and R_2.

STABILITY FACTOR'S FOR SELF BIAS CIRCUIT:

S is calculated assuming that no AC signal is impressed and only DC voltages are present. In the Fig 5.8, the voltage V is the drop across R_2. Combination acts as a potential divider. So the drop across R_2 which is equal to V, is given by the expression,

$$V = \frac{V_{CC}.R_2}{R_1 + R_2}.$$

R_B is the effective resistance looking back from the base terminal

$$\therefore \quad R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying Kirchhoff's Voltage Law around the base circuit,

$$V = I_B R_B + R_e (I_B + I_C) + V_{BE}$$

Assuming V_{BE} to be independent of I_C, differentiating I_B with respect to I_C, to get 'S'.

$$I_B, R_B + I_B R_e = + V - V_{BE} - I_C \times R_e$$

$$I_B (R_B + R_e) = V - V_{BE} - I_C \times R_e$$

$$\therefore \quad I_B = \frac{(V - V_{BE} - I_C R_e)}{(R_B + R_e)}$$

$$\frac{\partial I_B}{\partial I_C} = - \frac{R_e}{R_e + R_B}$$

The expression for stability factor $S = \dfrac{1+\beta}{1-\beta\left(\dfrac{\partial I_B}{\partial I_C}\right)}$

$$\therefore \quad S = \frac{1+\beta}{1+\beta\left(\dfrac{R_e}{R_e + R_B}\right)}$$

If $\dfrac{R_B}{R_e}$ is very small, $S \simeq 1$.

The fixed bias circuit, collector to base bias circuit and Emitter bias circuits provide stabilisation of I_C against variations in I_{CO}. But I_C also varies with V_{BE} and β. ***V_{BE} decreases at the rate of 2.5 mV/°C for both Germanium and Silicon transistors***. Because, with the increase in T, the potential barrier is reduced and more number of carriers can move from one side (p) to the other side (n). β also increases side with temperature. Hence I_C changes.

Q.4 b. For the Darlington pair circuit of fig. 3, $\beta_1 = \beta_2 = 30$. Find the value of R_1. If $R_1 = R_2$.

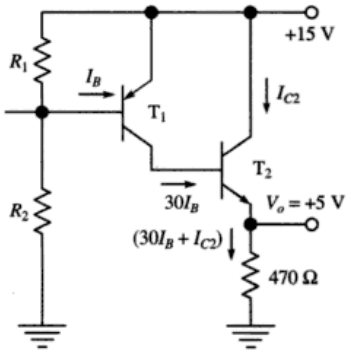


Fig.3

Answer:

According to figure the base emitter loops of the two transistors

$$R_1 = R_2;\ V_{BB} = \frac{15}{2} = 7.5\ \text{V}$$

$$R_B = R_1 \| R_2 = \frac{R_1}{2}$$

$$7.5 = \left(\frac{R_1}{2}\right) I_B + 0.7 \times 2 + (30I_B + I_{C2}) \times 0.47$$

$$I_{C2} = 30 \times (30) I_B = 900 I_B$$

$$7.5 = \left(\frac{R_1}{2}\right) I_B + 1.4 + (30 + 900) \times 0.47 I_B$$

$$\left(\frac{R_1}{2}\right) I_B + 437 I_B = 6.1 \qquad \text{(i)}$$

Output voltage is given as

$$0.47 \times 930 I_B = 5 \qquad \text{(ii)}$$

or $$I_B = \frac{5}{0.47 \times 930} = 0.0114\ \text{mA}$$

Substituting the value of I_B in Eq. (i)

$$\frac{R_1}{2} \times 0.0114 + 437 \times 0.0114 = 6.1$$

or $$R_1 = \frac{6.1 - 4.98}{0.0114} \times 2 = 196\ \text{k}\Omega$$

Q.5 a. For the emitter follower circuit of fig.4 the BJT has the following parameters:
g_m=35ms, β=125,

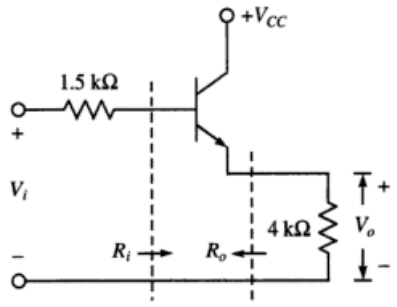


Fig.4

(i) Draw the low frequency small signal model of this circuit.
(ii) Determine R_i & R_o.
(iii) Evaluate the transfer function V_O/V_i.

Answer:

$$r_\pi = \frac{\beta}{g_m} = \frac{125}{35} = 3.57 \text{ k}\Omega$$

(a) The small-signal model is drawn in Figure 3.67

$$R_i = r_\pi + (1+\beta)R_E = 3.57 + 126 \times 4$$
$$= 508 \text{ k}\Omega\text{; high}$$

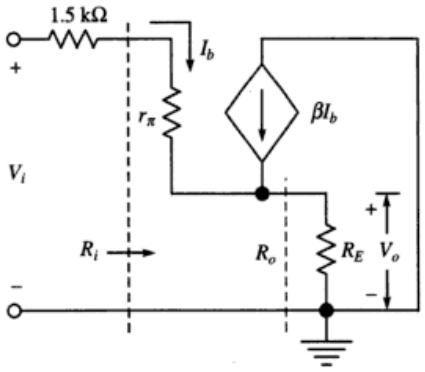


FIGURE
small-signal model.

(b) $R_o = \dfrac{V_o}{I_{SC}}$

$V_o = (1+\beta) R_E I_b$

$I_b = \dfrac{V_i}{1.5 + r_\pi + (1+\beta) R_E}$

$V_o = (1+\beta) R_E \times \dfrac{V_i}{1.5 + r_\pi + (1+\beta) R_E}$

Short-circuiting output, $I_b = \dfrac{V_i}{(1.5 + r_\pi)}$

$$I_{SC} = \frac{(1+\beta)V_i}{(1.5+r_\pi)}$$

$$R_o = \frac{V_o}{I_{SC}} = \frac{(1+\beta)R_E}{1.5 + r_\pi + (1+\beta)R_E} \times \frac{(1.5+r_\pi)}{(1+\beta)}$$

or $$R_o = \frac{(1.5+r_\pi)R_E}{(1.5+r_\pi) + (1+\beta)R_E}$$

Substituting values,

$$R_o = \frac{(1.5+3.57)\times 4}{(1.5+3.57)+(1+125)\times 4} = 0.0398 \text{ k}\Omega \text{ or } 39.8\ \Omega\text{; low}$$

(c) $$\frac{V_o}{V_i} = \frac{(1+\beta)R_E}{1.5 + r_\pi + (1+\beta)R_E} = \frac{126 \times 4}{1.5 + 3.57 + 126 \times 4} = 0.99$$

Voltage gain is close to unity as it is an emitter–follower circuit.

Q.5 b. Draw and explain Common Emitter configuration

Answer:

COMMON-EMITTER CONFIGURATION:

The most frequently encountered transistor configuration appears in Fig. 3.13 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit. Both are shown in Fig. 3.14.

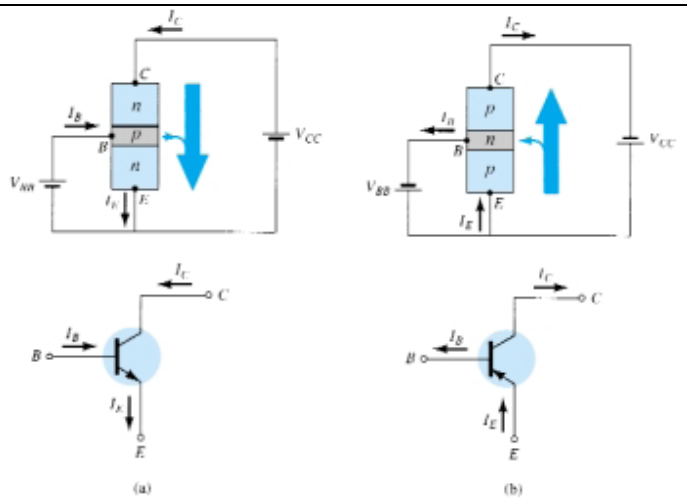


Figure 3.13 Notation and symbols used with the common-emitter configuration: (a) *npn* transistor; (b) *pnp* transistor.

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is, $IE = IC + IB$ and $IC = \alpha\ IE$. For the common-emitter configuration the output characteristics are a plot of the output current (IC) versus output voltage (VCE) for a range of values of input current (IB). The input characteristics are a plot of the input current (IB) versus the input voltage (VBE) for a range of values of output voltage (VCE).

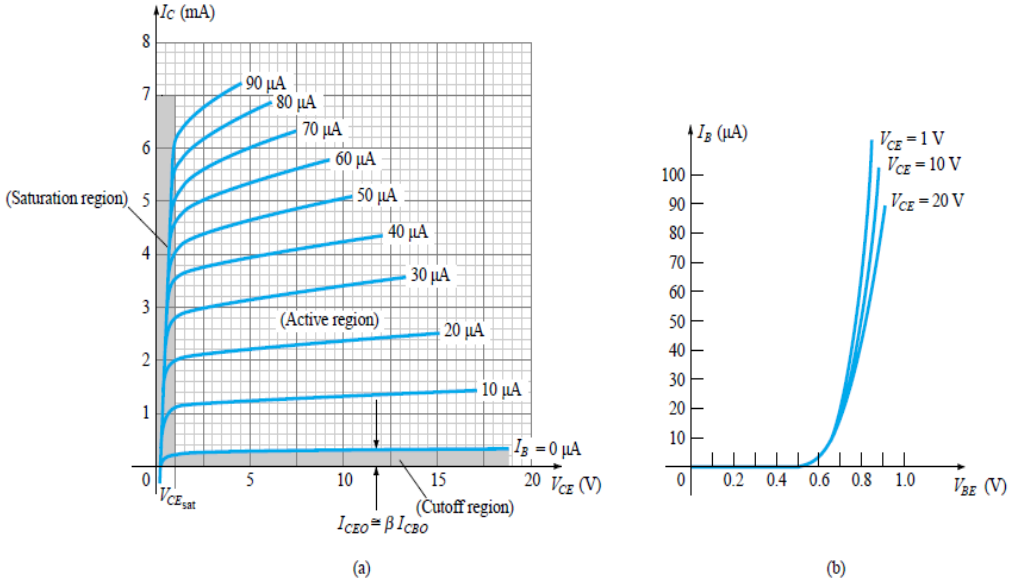


Figure 3.14 Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

Note that on the characteristics of Fig. 3.14 the magnitude of IB is in microamperes, compared to milliamperes of IC. Consider also that the curves of IB are not as

horizontal as those obtained for *IE* in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current. The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for *IB* are nearly straight and equally spaced. In Fig. 3.14a this region exists to the right of the vertical dashed line at *VCE*sat and above the curve for *IB* equal to zero. The region to the left of *VCE*sat is called the saturation region.

In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification. The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.14 that *IC* is not equal to zero when *IB* is zero. For the common-base configuration, when the input current *IE* was equal to zero, the collector current was equal only to the reverse saturation current *ICO*, so that the curve *IE* =0 and the voltage axis were, for all practical purposes, one.

The reason for this difference in collector characteristics can be derived through the proper manipulation of Eqs. (3.3) and (3.6). That is,

Eq. (3.6): $I_C = \alpha I_E + I_{CBO}$

Substitution gives Eq. (3.3): $I_C = \alpha(I_C + I_B) + I_{CBO}$

Rearranging yields

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha} \qquad (3.8)$$

Beta (β)

In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B} \qquad (3.10)$$

where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for α, β certainly reveals the relative magnitude of one current to the other. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

On specification sheets β_{dc} is usually included as h_{FE} with the h derived from an ac *h*ybrid equivalent circuit to be introduced in Chapter 7. The subscripts *FE* are derived from *f*orward-current amplification and common-*e*mitter configuration, respectively.

For ac situations an ac beta has been defined as follows:

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \qquad (3.11)$$

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C/I_B$ we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \qquad (3.12a)$$

or

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \qquad (3.12b)$$

In addition, recall that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

but using an equivalence of

$$\frac{1}{1 - \alpha} = \beta + 1$$

derived from the above, we find that

$$I_{CEO} = (\beta + 1)I_{CBO}$$

or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \qquad (3.13)$$

as indicated on Fig. 3.14a. Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

$$\boxed{I_C = \beta I_B} \qquad (31.4)$$

and since

$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$

we have

$$\boxed{I_E = (\beta + 1)I_B} \qquad (3.15)$$

Both of the equations above play a major role in the analysis in Chapter 4.

Q.6 a. Write down the effect of coupling capacitor in low frequency analysis.

Answer:

Effect of Coupling Capacitors

While analyzing the role of coupling capacitors, we assume that the bypass capacitors act as effective short-circuits.

The mid-frequency models (resistive) of Figures 4.14(a) and (b) are modified as in Figures 4.22(a) and (b) by including the coupling capacitors (C_{C1} and C_{C2}). Being analogous to each other, the circuit analysis for FET and BJT amplifiers can proceed simultaneously.

In the case of BJT circuit, it is assumed that $R_B >> r_\pi$ and so R_B is not included in Figure 4.22(b). If R_B is not high then $r'_\pi = r_\pi \| R_B$.

From the input circuit of Figure 4.22(a) (FET), it immediately follows that (circuit acts as a voltage divider).

$$\bar{V}_s = \left\{\frac{R_G}{(R_s + R_G) - j/(\omega C_{C1})}\right\}\bar{V}_s = \left\{\frac{R_G/(R_s + R_G)}{1 - j/[\omega C_{C_1}(R_s + R_G)]}\right\}\bar{V}_s = \frac{A_{V01}}{1 - j(\omega_{11}/\omega)}\bar{V}_s \qquad (4.9)$$

where, $A_{V01} = \dfrac{R_G}{R_s + R_G}$

= mid-frequency voltage gain of input circuit (C_{C1}, short-circuited) (4.10)

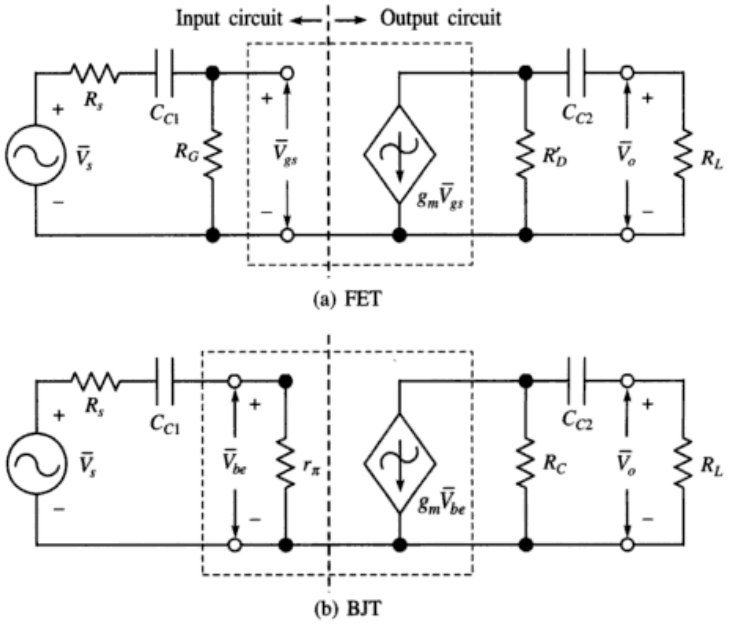


FIGURE 4.22 Low-frequency amplifier circuits including effects of coupling capacitors.

$$\omega_{11} = \frac{1}{C_{C1}(R_s + r_\pi)} = \text{corner frequency (input circuit) (FET)} \quad (4.11)$$

Similarly, for the input circuit of Figure 4.22(b) (BJT)

$$V_{be} = \frac{A_{V01}}{1 - j(\omega_{11}/\omega)} \bar{V}_s \quad (4.12)$$

where, $A_{V01} = \dfrac{r_\pi}{R_s + r_\pi}$

$= \text{mid-frequency voltage gain of input circuit } (C_{C1}, \text{ short-circuited})$ (4.13)

$$\omega_{11} = \frac{1}{C_{C1}(R_s + r_\pi)} = \text{corner frequency (input circuit) (BJT)} \quad (4.14)$$

Consider now the output circuit of FET and BJT amplifiers redrawn in Figure 4.23(a) and (b) respectively along with their Thevenin equivalents. It immediately follows that for FET circuit (Figure 4.23(a)) that

$$\bar{V}_o = \left[\frac{-g_m R'_D R_L}{(R'_D + R_L) - j/(\omega C_{C2})}\right] \bar{V}_{gs} = \left\{\frac{-g_m R_o}{1 - j/[\omega C_{C2}(R'_D + R_L)]}\right\} \bar{V}_{gs} = \frac{A_{V02}}{1 - j(\omega_{12}/\omega)} \bar{V}_{gs} \quad (4.15)$$

where, $A_{V02} = -g_m R_o = \text{mid-frequency voltage gain of output circuit}$

$(C_{C2}, \text{ short-circuited}); R_o = R'_D \| R_L$ (4.16)

$$\omega_{12} = \frac{1}{C_{C2}(R'_D + R_L)} = \text{corner frequency (output circuit) (FET)} \quad (4.17)$$

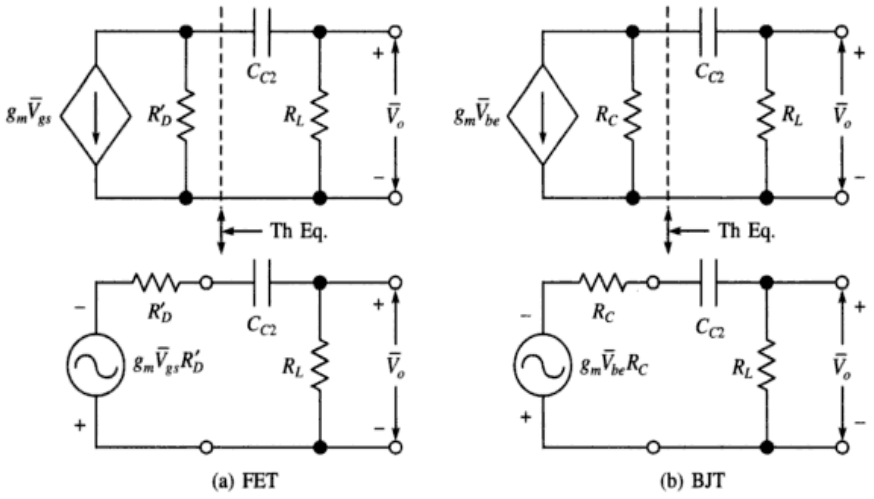


FIGURE 4.23 Thevenin equivalents of the output circuits

Similarly, for the output circuit of Figure 4.23(b) (BJT)

$$\bar{V}_o = \frac{A_{V02}}{1 - j(\omega_{12}/\omega)} \bar{V}_{be} \quad (4.18)$$

where, $A_{V02} = -g_m R_o = \text{mid-frequency voltage gain of output circuit}$

(C_{C2} short-circuited); $R_o = R_C \| R_L$ (4.19)

$$\omega_{12} = \frac{1}{C_{C2}(R_C + R_L)} = \text{corner frequency (output circuit) (BJT)} \quad (4.20)$$

We are now ready to obtain the expressions for the overall voltage gain.

FET: Substituting from $\bar{V}_{gs}$ from Eq. (4.9) in Eq. (4.15)

$$\bar{A}_{VL} = \frac{\bar{V}_o}{\bar{V}_s} = \frac{A_{V0}}{[1 - j(\omega_{11}/\omega)][1 - j(\omega_{12}/\omega)]} \quad (4.21)$$

where,
$$A_{V0} = A_{V01}A_{V02} = -\left(\frac{R_G}{R_s + R_G} g_m R_o\right) \quad (4.22a)$$

$$\approx -g_m R_o;\ R_G >> R_s;\ R_o = R'_D \| R_L \quad (4.22b)$$

= mid-frequency voltage gain; see Eq. (4.6)

BJT: It easily follows that $\bar{A}_{VL}$ as expressed in Eq. (4.21) applies with

$$A_{V0} = A_{V01}A_{V02} = -\left(\frac{r_\pi}{R_s + r_\pi}\right) g_m R_o;\ R_o = R_C \| R_L \quad (4.23a)$$

$$= -\beta\left(\frac{R_o}{R_s + r_\pi}\right);\ \beta = r_\pi g_m \quad (4.23b)$$

= mid-frequency voltage gain; see Eq. (4.8)

In case it is desired to consider the effect of R_B, in all the above relationships for BJT, replace

$$r'_\pi \Rightarrow (R_B \| r_\pi)$$

Equation (4.21) is the expression of low-frequency gain (complex number) for FET/ BJT single-stage amplifier (without consideration to the effect of the bypass capacitor). This expression has two corner frequencies (ω_{11} arising out of input circuit and ω_{12} arising out of output circuit). Its Bode plot (dB–log ω) is sketched in Figure 4.24 assuming $\omega_{11} > \omega_{12}$, i.e., $\omega_{11} = \omega_L$ is the lower cut-off frequency.

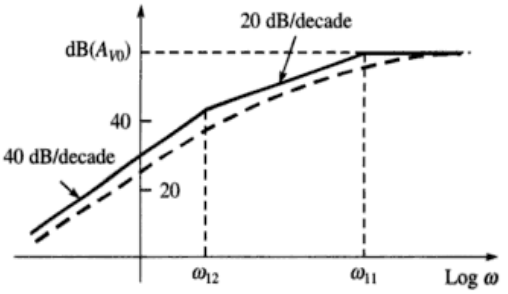


FIGURE 4.24 Bode plot—low-frequency region.

However, in the frequency response curve presented in Figure 4.6, only one low-frequency cut-off was assumed.

Q.6 b. Explain the frequency response and linear circuit model of single stage RC Coupled amplifier.

Answer:
Single stage RC Coupled amplifier:

Frequency Response (Typical)

Typical voltage gain of an RC-coupled amplifier as well as its phase angle are plotted against the frequency in Figure 4.6 wherein the frequency scale is logarithmic as the frequency range to be covered is very wide. In the *mid-frequency* range, the series capacitors (coupling capacitors) act as short-circuit and the shunt capacitors (device model parameters) act as open-circuit, so the voltage gain in this range of frequencies is substantially constant. The frequency response curve falls off in low-frequency range because of the increasing impedance ($1/\omega C$) of the coupling capacitors and the response also falls off in the high-frequency range because of the decreasing impedance of the shunt capacitors. In simple amplifiers considered here the frequency response (plotted against low-frequency) is symmetric. The low- and high-frequencies (f_L and f_H) at which the gain falls down to $A_1 = A_2 = A_{V0}/\sqrt{2}$, where A_{V0} = mid-frequency gain, are known as *cut-off frequencies* or *half power frequencies*. The phase angle of the gain at these frequencies is $\pm 45°$. The frequency range f_L to f_H is known as the *bandwidth* of the amplifier. The frequency spectrum of the signal must lie in this band for faithful reproduction of the amplified signal keeping distortion to acceptable levels.

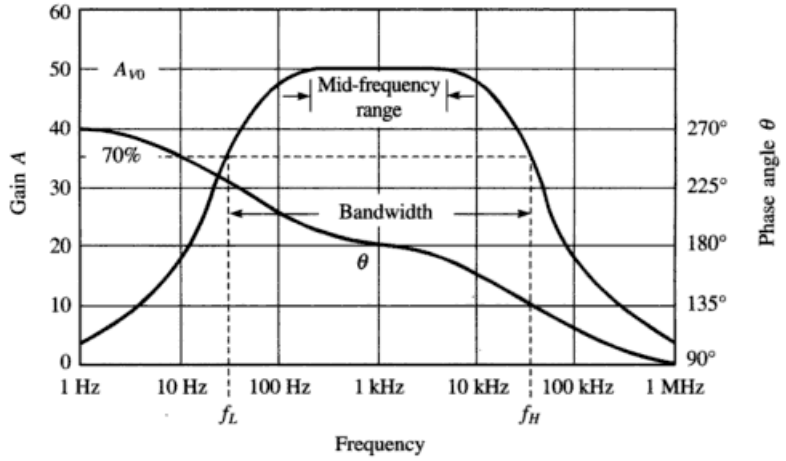


FIGURE 4.6 Frequency response of an RC-coupled single-stage amplifier.

The General Amplifier

The circuit of Figure 4.7 is the general representation of a single-stage amplifier. It is a two-port network wherein the input signal comes from a source which may be a phono pick-up or a preceding amplifier stage, and is characterized by an open-circuit voltage V_s and a Thevenin impedance Z_s. The amplifier has input and output impedances Z_i and Z_o respectively and a dependent source (controlled by input current or voltage). The load of the amplifier represented by impedance Z_L would usually be the following amplifier stage.

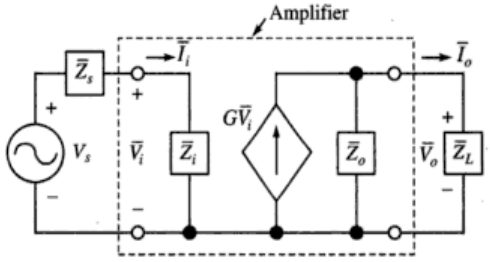
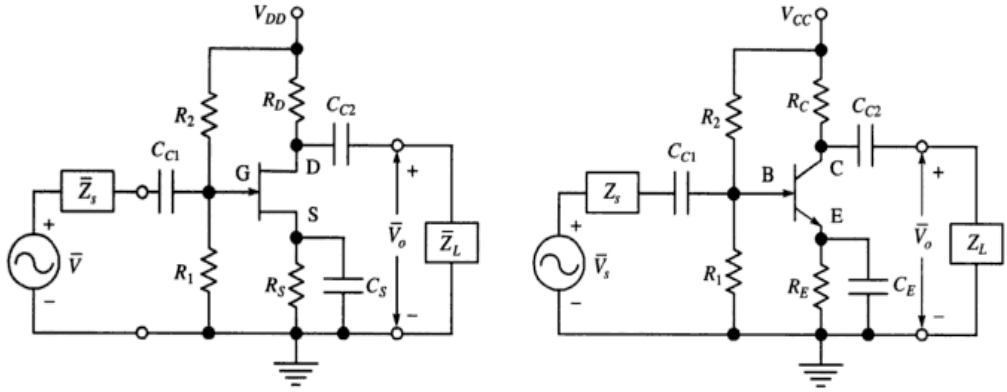


FIGURE 4.7 The general single-stage amplifier.

Typical Amplifier Circuits

FET and BJT single-stage RC-coupled amplifier circuits using potential divider biasing are drawn in Figures 4.8(a) and (b). These circuits are linked to input–output through coupling capacitors (C_{C1} and C_{C2}). The biasing resistors, R_S for the FET circuit and R_E for the BJT circuit have bypass capacitors C_S and C_E connected across these respectively. In the mid-frequency and high-frequency regions, the bypass capacitor offers low impedance ($1/C\omega$) and effectively short-circuits the biasing resistor so that no ac voltage drop occurs across it. Such a voltage drop would otherwise cause negative feedback in the circuit reducing the amplifier gain as would happen in low-frequency region when $1/C\omega$ increases as the frequency reduces (see Figure 4.1).

The input is regarded as a voltage source $\bar{V}_s$ with a Thevenin impedance $\bar{Z}_s$. The load usually comprises R_L and C_L in parallel as presented by the next stage of amplification.



(a) FET (b) BJT

FIGURE 4.8 Single-stage RC-coupled amplifier.

Small-Signal Model

As already elaborated in Chapter 3 in the small-signal model of the amplifier circuits of Figures 4.8(a) and (b), the battery would act as a short-circuit so that R_1 and R_2 would appear in parallel (for FET circuit $R_G = R_1 \| R_2$ and for BJT circuit $R_B = R_1 \| R_2$) and the battery end of R_D/R_C would be grounded. It shall be assumed that bypassing capacitors are such as to effectively short-circuit the biasing resistors so that S-end of FET and E-end of BJT get effectively connected to ground (as shown in Figures 4.9(a) and (b)) respectively. The effect of by-pass capacitor will be considered at a later stage in this chapter.

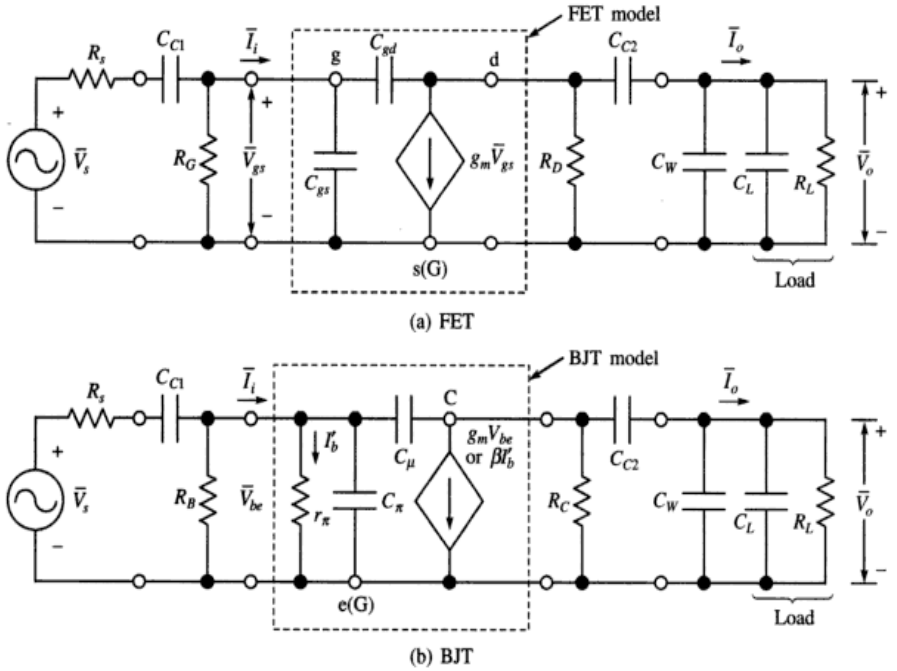


FIGURE 4.9 Linear circuit model of RC-coupled amplifiers.

The small-signal model of FET has been presented in Figure 3.7. Combining it with the argument advanced above leads to the small-signal model of the FET RC-coupled amplifier of Figure 4.9(a). Further the capacitance C_W accounts for the entire capacitance at the output end; this affects the amplifier gain at high-frequencies. C_L is the load capacitance.

To complete the model of the BJT amplifier, we make use of the circuit model of BJT as in Figure 3.6 by making suitable approximations. The base spreading resistance r_x with a very small series effect (about 100–150 Ω) can be ignored. The shunt resistance r_μ is very high as it is the resistance offered by the reversed biased collector base junction and therefore can be regarded as open circuit. Also the base width modulation resistance r_o, being much larger than R_C (of the amplifier circuit, Figure 4.9(b)), can be considered open circuit. Capacitance C_W is added in shunt to account for the entire stray capacitance at the output end. With these approximations, the circuit model of the BJT as in Figure 4.9(b) immediately follows.

It is easily seen from the circuit models of the two kinds of amplifiers that these are similar and, therefore, their analysis can be carried out simultaneously.

In an FET circuit model of Figure 4.9(a), it may be necessary to consider r_d which can be combined with R_D so that $R_D \| r_d = R'_D$. Also for the BJT circuit of Figure 4.9(b) r_o (when need to be considered) can be combined with R_C as $R_C \| r_o = R'_C$. However, in the low-frequency region, when bypass capacitances are effective in the circuit model with R_S in the source leg of an FET and R_E in the emitter leg, such parallel combination cannot be used and therefore the circuit must be analyzed properly.

Q.7 a. Derive the expression for the frequency of Wein Bridge Oscillators.

Answer:

WIEN BRIDGE OSCILLATOR

In this circuit, a balanced bridge is used as the feedback network. The active element is an operational amplifier. It employs lead-lag Network. Frequency *fo* can be varied

in the ratio of 10 :1 compared to 3 : 1 in other oscillator circuits.
External voltage V 0' is applied betweeen 3 and 4, as shown in Fig.8.16.

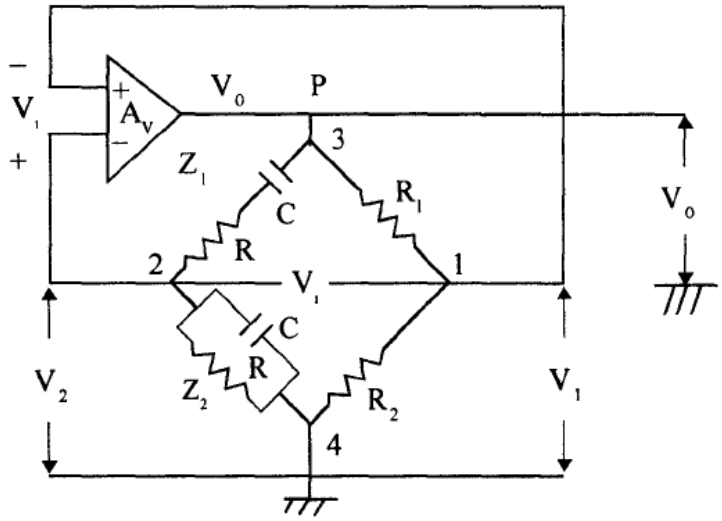


Fig. 8.16 Wien bridge oscillator circuit.

EXPRESSION FOR FREQUENCY:

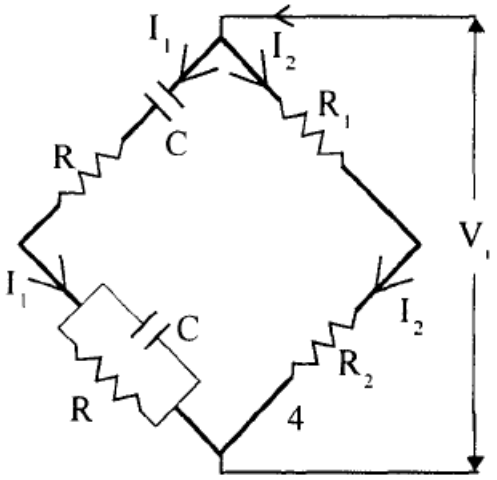


Fig. Wien Bridge oscillator circuit.

$$I_1 = \frac{\left(R + \frac{1}{j\omega c}\right)}{I_1\left(\frac{R}{1 + j\omega cR}\right)} = \frac{I_2 R_1}{I_2 R_L}$$

$$R_1 = \frac{\left(R_2 R + \frac{R_2}{j\omega C}\right)(1 + j\omega CR)}{R};$$

$$R_1 R = \left(R_2 R + \frac{R_2}{jwC}\right)(1 + jwCR)$$

$$R_2 \cdot R + \frac{R_2}{j\omega C} = \left(\frac{R_1 R}{1 + j\omega CR}\right)$$

$$[(R\,R_2)(j\omega C) + R_2]\,R_2\,j\omega CR - \omega^2 C^2 R^2 R_2 = R_1 R\,j\omega C$$

$$(R_1 R_2)(j\omega C) + R_2 + R_2\,j\omega CR - \omega^2 c^2 R^2 R_2 = R_1 R\,j\omega C$$

Equating imaginary parts,

$$R_1 R_2\,\omega C + R_2\,\omega CR = R_1 R\omega C$$

Equating real parts,

$$A = 1 + \frac{R_1}{R_2} + \frac{C_1}{C_2},\quad R_2 = \omega^2 C^2 R^2 R_2$$

$$\therefore \quad \omega^2 = \frac{1}{C^2 R^2} \quad \text{or} \quad \boxed{f = \frac{1}{2\pi RC}}$$

$$R_1 = \frac{R_2 . R}{R} + \frac{R_2}{j\omega CR} + j\omega CRR_2 + R_2$$

$$2R_2 = R_1 \quad \text{or} \quad \boxed{\frac{R_2}{R_1 + R_2} = \frac{1}{3}}$$

So the minimum gain of the amplifier must be 3.

$$\frac{-R_2}{\omega CR} = \omega CRR_2$$

$$\omega^2 = \frac{1}{(RC)^2}\ ; \quad \text{or} \quad \boxed{f = \frac{1}{2\pi RC}}$$

This is the frequency at which the circuit oscillates. Continuous variation of frequency is accomplished by using the capacitors 'C'.

Q.7 b. Deduce the Barkausen Criterion for the generation of sustained oscillations. How are the oscillations initiated?

Answer:

BARKHAUSEN CRITERION:

We make an asssumption that the circuit operates only in the linear region, and the amplifier feedback network contains reactive elements. For a sinusoidal wave form, if $X_i = X_f'$, the amplitude, phase and frequency of X_i and X_f' be identical. ***The frequency of a sinusoidal oscillator is determined by the condition that loop gain, Phase shift is zero at that frequency.***

For oscillator circuits positive feedback must be there i.e., V_f must be in phase with V_i to get added to V_i. When active device BJT or FET gives 180^0 phase shift, the feedback network must produce another 180^0 phase shift so that net phase shift is 0^0 or 360^0 and V_f is in phase with V_i to make it positive feedback.

Oscillations will not be sustained if, at the oscillator frequency the magnitude of the product of the transfer gain of the amplifier and of β are less than unity.

The conditions $-A\beta = 1$ is called ***Barkhausen criterion***

i.e. $|\beta A| = 1$ and phase of $-A\beta = 0$.

But $A_f = \frac{A}{1+\beta A}$. If $\beta A = -1$, than $A_f \to \infty$.

which implies that, there exists an output voltage even in the absence of an externally applied voltage.

A 1-V signal appearing initially at the input terminals will, after a trip around the loop and back to the input terminals, appear there, with an amplitude larger than 1V. This larger voltage will then reappear as a still larger voltage and so on. So if $|\beta A|$ is larger than1, the amplitude of oscillations will continue to increase without limit. But practically, to limit the increase of amplitude of oscillations, nonlinearity ability of the circuit will be set in. Though a circuit has been designed for $|\beta A| = 1$, since circuit components and transistor change characteristics with age, temperature, voltage etc. $|\beta A|$ will become larger or smaller than 1. If $\beta A < 1$, the oscillations will stop. If $\beta A > 1$, the amplitude practically will increase. So, to achieve a sinusoidal osciallation practically $|\beta A| > 1$ to 5%, so that with incidental variations in transistor circuit parameters, $|\beta A|$ shall not fall below unity.

Q.8 a. Explain the circuit operation & transfer characteristics of Class B Amplifier.

Answer:

Class B amplifier: ***Figure*** 14.5 shows a class B output stage. It consists of a complementary pair of transistors (an ***npn*** and a ***pnp)*** connected in such a way that both cannot conduct simultaneously.

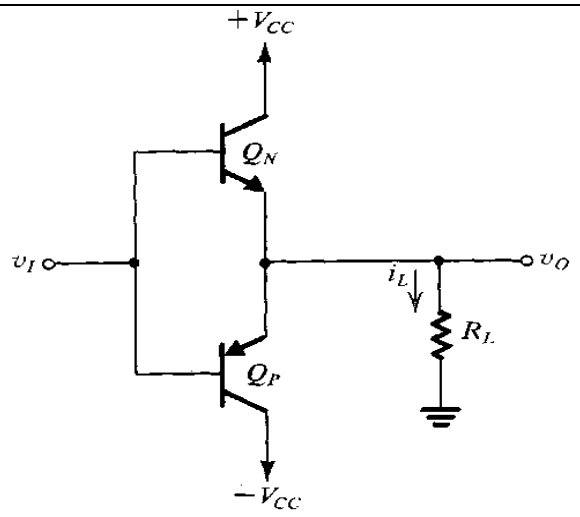


FIGURE 14.5 A class B output stage.

Circuit Operation

When the input voltage *v1* is zero, both transistors are cut off and the output voltage *v0* is zero. As *vt* goes positive and exceeds about 0.5 V, *QN* conducts and operates as an emitter follower. In this case *v0* follows w7'(i.e., *v0= vr~ vBEN)* and *QN* supplies the load current. Meanwhile, the emitter-base junction of *QP* will be reverse-biased by the *VBE* of *QN,* which is approximately 0.7 V. Thus *QP* will be cut off. If the input goes negative by more than about 0.5 V, *QP* turns on and acts as an emitter follower. Again *v0* follows *vI* (i.e., *v0 = v1 + vEBP),* but in this case *QP* supplies the load current and *QN* will b e cut off. We conclude that the transistors in the class B stage of Fig. 14.5 are biased at zero current and conduct only when the input signal is present. The circuit operates in a **push-pull** fashion: *QN pushes* (sources) current into the load when *v,* is positive, and *QP pulls* (sinks) current from the load when *v,* is negative.

14.3.2 Transfer Characteristic

A sketch of the transfer characteristic of the class B stage is shown in Fig. 14.6. Note that there exists a range of ***vj*** centered around zero where both transistors are cut off and *v0* is zero. This **dead band** results in t he **crossover distortion** illustrated in Fig. 14.7 for the case of an input sine wave. The effect of crossover distortion will be most pronounced when the amplitude of the input signal is small. Crossover distortion in audio power amplifiers gives rise to unpleasant sounds.

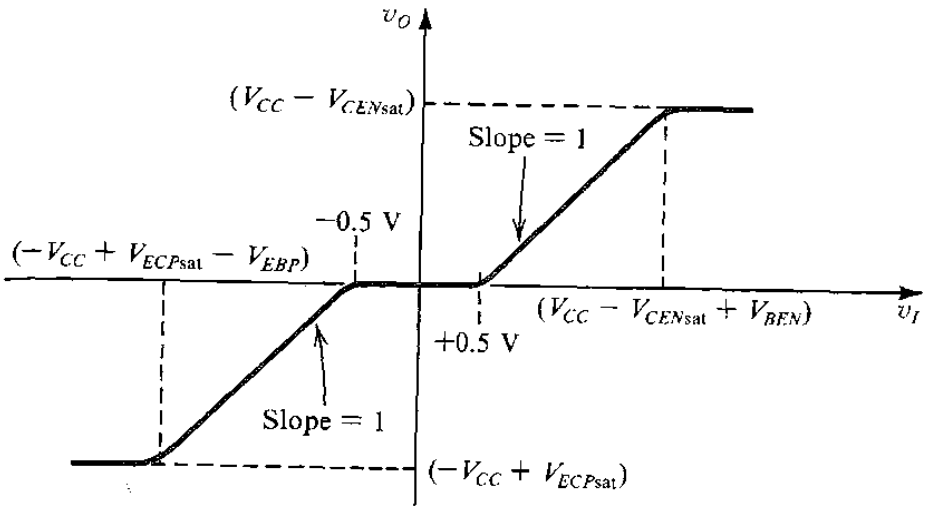


FIGURE 14.6 Transfer characteristic for the class B output stage in Fig. 14.5.

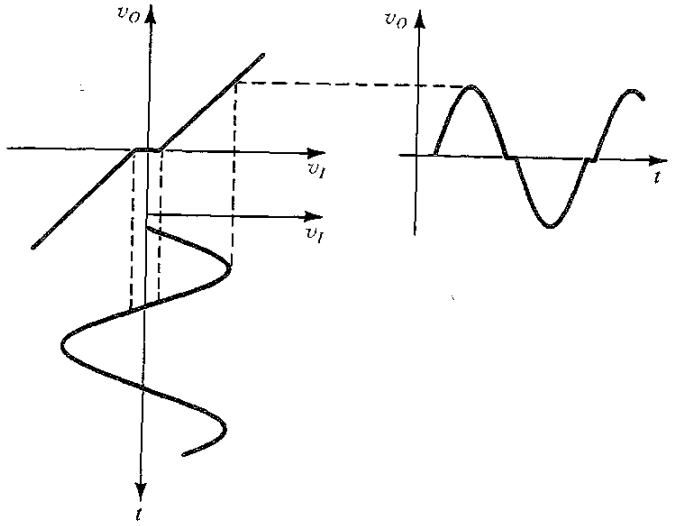


FIGURE 14.7 Illustrating how the dead band in the class B transfer characteristic results in crossover distortion.

Q.8 b. Design a class B output stage to deliver an average power of 20 W to an 8-Q load. The power supply is to be selected such that *Vcc* is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including short-circuit protection circuitry. Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

Answer:

Design a class B output stage to deliver an average power of 20 W to an 8-Q load. The power supply is to be selected such that *Vcc* is about 5 V greater than the peak output voltage. This avoids transistor saturation and the associated nonlinear distortion, and allows for including short-circuit protection circuitry. Determine the supply voltage required, the peak current drawn from each supply, the total supply power, and the power-conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$

$$\hat{V}_o = \sqrt{2P_L R_L}$$
$$= \sqrt{2 \times 20 \times 8} = 17.9 \text{ V}$$

Therefore we select *Vcc* = 23 V. The peak current drawn from each supply is

$$\hat{I}_o = \frac{\hat{V}_o}{R_L} = \frac{17.9}{8} = 2.24 \text{ A}$$

The average power drawn from each supply is

$$P_{S+} = P_{S-} = \frac{1}{\pi} \times 2.24 \times 23 = 16.4 \text{ W}$$

for a total supply power of 32.8 W. The power-conversion efficiency is

$$\eta = \frac{P_L}{P_S} = \frac{20}{32.8} \times 100 = 61\%$$

The maximum power dissipated in each transistor is given by

$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L}$$

$$= \frac{(23)^2}{\pi^2 \times 8} = 6.7 \text{ W}$$

Q.9 a. Briefly explain various steps of IC fabrication.

Answer:

The basic IC fabrication steps are as follows. Some of these steps may be carried out many times, in different combinations and under different processing conditions during a complete fabrication run.

Wafer Preparation

The starting material for modern integrated circuits is very-high-purity silicon. The material is grown as a single-crystal ingot. It takes the form of a steel gray solid cylinder 10 cm to 30 cm in diameter (Fig. A . 1) and can be 1 m to 2 m in length. This crystal is then sawed (like a loaf of bread) to produce circular wafers that are

400 tan to 600 *pm* thick (a micrometer or micron is a millionth of a meter). The surface of the wafer is then polished to a mirror finish using chemical and mechanical polishing (CMP) techniques. Semiconductor manufacturers usually purchase ready-made silicon wafers from a supplier and rarely start their process at the ingot stage. The basic electrical and mechanical properties of the wafer depend on the orientation of the crystaline planes, as well as the concentration and type of impurities present. These variables are strictly controlled during crystal growth. Controlled amounts of impurities can be added to the pure silicon in a process known as doping. This allows the alteration of the electrical properties of the silicon, in particular its resistivity. It is also possible to control the conduction-carrier type, either holes (in *p-type* silicon) or electrons (in n-type silicon), that is responsible for electrical conduction. If a large number of impurity atoms is added, then the silicon is said to be heavily doped (e.g., concentration > 1 0 1 8 atoms/cm3). When designating the relative doping concentrations in semiconductor device structures, it is common to use + and - symbols. A heavily doped (low-resistivity) w-type silicon wafer would be referred to as *n*+ material, while a lightly doped region may be referred to as *n*- The ability to control the type of impurity and the doping concentration in the silicon permits the formation of diodes, transistors, and resistors in flexible integrated-circuit form.

Oxidation:

Oxidation refers to the chemical process of silicon reacting with oxygen to form silicon dioxide (S i 0 2) . To speed up the reaction, it is necessary to use special high-temperature (e.g., 1000-1200°C) ultraclean furnaces. To avoid the introduction of even small quantities of contaminants (which could significantly alter the electrical properties of the silicon), it is necessary to maintain a clean environment. This is true for all processing steps involved in the fabrication of an integrated circuit. Specially filtered air is circulated in the processing area, and all personnel must wear special lint-free clothing. The oxygen used in the reaction can be introduced either as a high-purity gas (in a process referred to as a "dry oxidation") or as steam (for "wet oxidation"). In general, wet oxidation has a faster growth rate, but dry oxidation gives better electrical characteristics. In either case, the thermally grown oxide layer has excellent electrical insulation properties. The dielectric strength for S i 0 2 is approximately 107 V/cm. It has a dielectric constant of about 3.9 and can be used to form excellent capacitors. As noted, silicon dioxide serves as an effective mask against many impurities, allowing the introduction of dopants into the silicon only in regions that are not covered with oxide. This masking property is one of the essential enablers of mass fabrication of VLSI devices. Silicon dioxide is a thin transparent film, and the silicon surface is highly reflective. If white light is shone on an oxidized wafer, constructive and destructive interference will cause certain colors to be reflected. The wavelengths of the reflected light depend on the thickness of the oxide layer. In fact, by categorizing the color of the wafer surface, one can deduce the thickness of the oxide layer. The same principle is used by sophisticated optical inferometers to measure film thickness. On a processed wafer, there will be regions with different oxide thicknesses. The corresponding colors can be quite vivid, and thickness variations are immediately obvious when a finished wafer is viewed with the naked eye

Diffusion

Diffusion is the process by which atoms move from a high-concentration region to a low-concentration region through the semiconductor crystal. The diffusion process is very much like a drop of ink dispersing through a glass of water except that it occurs much more slowly in solids. In fabrication, diffusion is a method by which to introduce impurity atoms (dopants) into silicon to change its resistivity. The rate at which dopants diffuse in silicon is a strong function of temperature. Thus, for speed, diffusion of impurities is usually carried out at high temperatures (1000-1200°C) to obtain the desired doping profile. When the wafer is cooled to room temperature, the impurities are essentially "frozen" in position. The diffusion process is performed in furnaces similar to those used for oxidation. The depth to which the impurities diffuse depends on both the temperature and the time allocated. The most common impurities used as dopants are boron, phosphorus, and arsenic. Boron is a *p-type* dopant, while phosphorus and arsenic are n-type dopants. These dopants can be effectively masked by thin silicon dioxide layers. By diffusing boron into an n-type substrate, a *pn* junction (diode) is formed. If the doping concentration is heavy enough, the diffused layer can also be used as a conductor.

Ion Implantation:

Ion implantation is another method used to introduce impurity atoms into the semiconductor crystal. An ion implanter produces ions of the desired dopant, accelerates them by an electric field, and allows them to strike the semiconductor surface. The ions become embedded in the crystal lattice. The depth of penetration is related to the energy of the ion beam, which can be controlled by the accelerating-field voltage. The quantity of ions implanted can be controlled by varying the beam current (flow of ions). Since both voltage and current can be accurately measured and controlled, ion implantation results in much more accurate and reproducible impurity profiles than can be obtained by diffusion. In addition, ion implantation can be performed at room temperature. Ion implantation normally is used when accurate control of the doping profile is essential for device operation.

Chemical-Vapor Deposition

Chemical-vapor deposition (CVD) is a process by which gases or vapors are chemically reacted, leading to the formation of solids on a substrate. CVD can be used to deposit various materials on a silicon substrate including S i 0 2 , Si3N4 , and polysilicon. For instance, if silane gas and oxygen are allowed to react above a silicon substrate, the end product, silicon dioxide, will be deposited as a solid film on the silicon wafer surface. The properties of the CVD oxide layer are not as good as those of a thermally grown oxide, but such a layer is sufficient to act as an electrical insulator. 'The advantage of a CVD layer is that the oxide deposits at a fast rate and a low temperature (below 500°C). If silane gas alone is used, then a silicon layer will be deposited on the wafer. If the reaction temperature is high enough (above 1000°C), the layer deposited will be a crystalline layer (assuming that there is an exposed crystalline silicon substrate). Such a layer is called an **epitaxial** layer, and the deposition process is referred to as **epitaxy,** rather than CVD. At lower temperatures, or if the substrate surface is not single-crystal silicon, the atoms will not be able to align in the same crystalline direction. Such a layer is called polycrystalline silicon (poly Si), since it consists of many small crystals of silicon

whose crystalline axes are oriented in random directions. These layers are normally doped very heavily to form highly conductive regions that can be used for electrical interconnections.

Metallization

The purpose of metallization is to interconnect the various components (transistors, capacitors, etc.) to form the desired integrated circuit. Metallization involves the initial deposition of a metal over the entire surface of the silicon. The required interconnection pattern is then selectively etched. The metal layer is normally deposited via a sputtering process. A pure metal disk (e.g., 99.99% aluminum) is placed under an argon (Ar) ion gun inside a vacuum chamber. The wafers are also mounted inside the chamber above the target. The Ar ions will not react with the metal, since Ar is a noble gas. However, their ions are made to physically bombard the target and literally knock metal atoms out of it. These metal atoms will then coat all the surface inside the chamber, including the wafers. The thickness of the metal film can be controlled by the length of time for sputtering, which is normally in the range of 1 to 2 minutes.

Photolithography

The surface geometry of the various integrated-circuit components is defined photographically. First, the wafer surface is coated with a photosensitive layer (called photoresist) using a spin-on technique. After this, a photographic plate with drawn patterns (e.g., a quartz plate with a chromium pattern) will be used to selectively expose the photoresist under ultraviolet (UV) illumination. The exposed areas will become softened (for positive photoresist). The exposed layer can then be removed using a chemical developer, causing the mask pattern to appear on the wafer. Very fine surface geometries can be reproduced accurately by this technique. Photolithography requires some of the most expensive equipment in VLSI fabrication. Currently, we are already approaching the physical limits of the photolithographic process. Deep UV light or electron beam can be used to define patterns with resolution as fine as 50 ran. However, another technological breakthrough will be needed to achieve further geometry downscaiing.

The patterned photoresist layer can be used as an effective masking layer to protect materials below from wet chemical etching or reactive ion etching. Correspondingly, silicon dioxide, silicon nitride, polysilicon, and metal layers can be selectively removed using the appropriate etching methods. After the etching step(s), the photoresist is stripped away, leaving behind a permanent pattern, an image of the photomask, on the wafer surface. To make this process even more challenging, multiple masking layers (there can be more than 20 layers in advanced VLSI fabrication processes) must be aligned precisely on top of previous layers. This must be done with even greater precision than is associated with the minimum dimensions of the masking patterns. This requirement imposes very critical mechanical and optical constraints on the photolithography equipment.

Packaging

A finished silicon wafer may contain several hundred or more finished circuits or chips. Each chip may contain from 10 to 108 or more transistors in a rectangular shape, typically between 1 mm and 10 mm on a side. The circuits are first tested electrically (while still in wafer form) using an automatic probing station. Bad

circuits are marked for later identification. The circuits are then separated from each other (by dicing), and the good circuits (called dies) are mounted in packages (or headers). Examples of such IC packages are given in Fig. A.2. Fine gold wires are normally used to connect the pins of the package to the metallization pattern on the die. Finally, the package is sealed using plastic or epoxy under vacuum or in an inert atmosphere.

Q.9 b. Write short note on Integrated Resistors and Integrated Capacitors.

Answer:

Integrated Resistors:

Resistors in integrated form are not very precise. They can be made from various diffusion regions as shown in Fig. Different diffusion regions have different resistivity. The *n* well is usually used for medium-value resistors, while the *n*+ and *p*+ diffusions are useful for low-value resistors. The actual resistance value can be defined by changing the length and width of diffused regions. The tolerance of the resistor value is very poor (20-50%), but the matching of two similar resistor values is quite good (5%). Thus circuit designers should design circuits that exploit resistor matching and avoid designs that require a specific resistor value.

All diffused resistors are self-isolated by the reversed-biased *pn* junctions. However, a serious drawback for these resistors is that they are accompanied by a substantial parasitic junction capacitance, making them not very useful for high-frequency applications. The reversed-biased *pn* junctions also exhibit a JFET effect, leading to a variation in the resistance value as the applied voltage is changed (a large voltage coefficient is undesirable). Since the mobilities of carriers vary with temperature, diffused resistors also exhibit a significant temperature coefficient. A more useful resistor can be fabricated using the polysilicon layer that is placed on top of the thick-field oxide. The thin polysilicon layer provides better surface area matching and hence more accurate resistor ratios. Furthermore, the poly resistor is physically separated from the substrate, resulting in much lower parasitic capacitance and voltage coefficient.

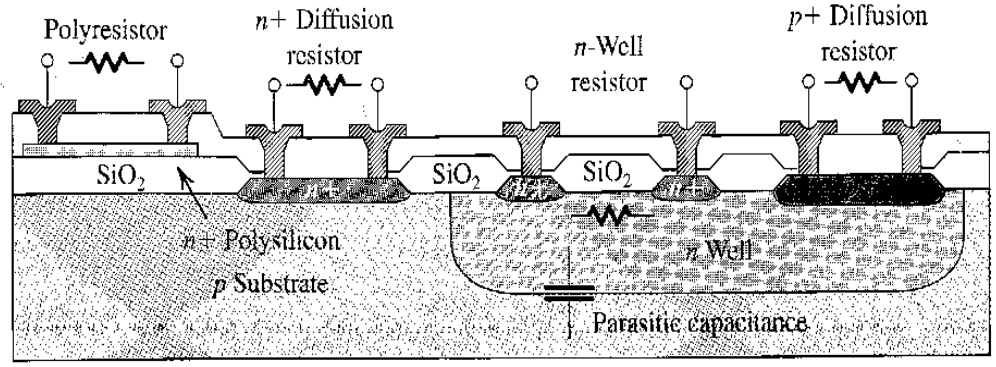


FIGURE: Cross sections of resistors of various types available from a typical n-well

CMOS process.

Integrated Capacitors:

Two types of capacitor structure are available in CMOS processes, MOS and interpoly capacitors (also MIM—metal-insulator-metal). The cross sections of these structures are as shown in Fig. A.6. The MOS gate capacitance, depicted in the center structure, is basically the gate-to-source capacitance of a MOSFET. The capacitance value is dependent on the gate area. The oxide thickness is the same as the gate oxide thickness in the MOSFETs. This capacitor exhibits a large voltage dependence. To eliminate this problem, an additional $n+$ implant is required to form the bottom plate of the capacitors, as shown in the structure on the right. Both these MOS capacitors are physically in contact with the substrate, resulting in a large parasitic *pn* junction capacitance at the bottom plate. The interpoly capacitor exhibits near ideal characteristics but at the expense of the inclusion of a second polysilicon layer to the CMOS process. Since this capacitor is placed on top of the thick-field oxide, parasitic effects are kept to a minimum. A third and less often used capacitor is the junction capacitor. Any *pn* junction under reversed bias produces a depletion region that acts as a dielectric between the *p* and the *n* regions. The capacitance is determined by geometry and doping levels and has a large voltage coefficient. This type of capacitor is often used as a variactor (variable capacitor) for tuning circuits. However, this capacitor works only with reversed-bias voltages. For interpoly and MOS capacitors, the capacitance values can be controlled to within 1%. Practical capacitance values range from 0.5 p F to a few 10s of picofarads. The matching between similar-size capacitors can be within 0.1%. This property is extremely useful for designing precision analog CMOS circuits.

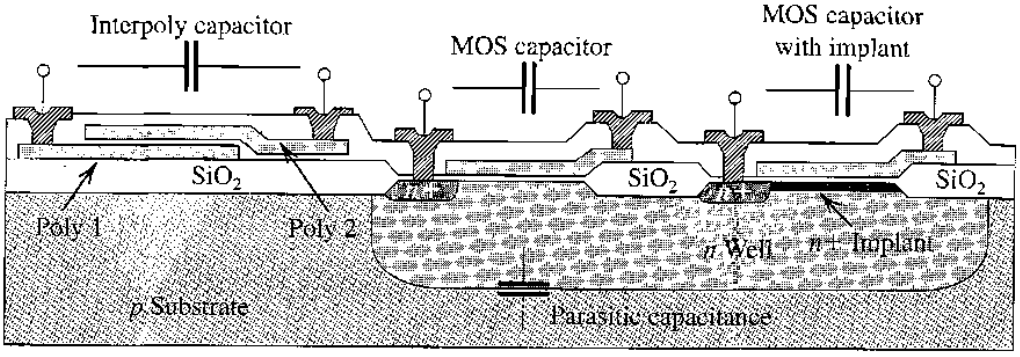


FIGURE Interpoly and MOS capacitors in an n-well CMOS process.

TEXT BOOK

I. Electronic Devices and Circuits, I. J. Nagrath, PHI (2007)