Q.2 a. Discuss the bus structure of a computer system. (4)

Answer:

Ans: A computer bus structure is provided which permits replacement of removable modules during operation of a computer wherein means are provided to precharge signal output lines to within a predetermined range prior to the usage of the signal output lines to carry signals, and further, wherein means are provided to minimize arcing to pins designed to carry the power and signals of a connector. In a specific embodiment, pin length, i.e., separation between male and female components of the connector, are subdivided into long pin length and short pin length. Ground connections and power connections for each voltage level are assigned to the long pin lengths. Signal connections and a second power connection for each voltage level is assigned to the short pin lengths. The precharge/prebias circuit comprises a resistor divider coupled between a power source and ground with a high impedance tap coupled to a designated signal pin, across which is coupled a charging capacitor or equivalent representing the capacitance of the signal line. Bias is applied to the precharge/prebias circuit for a sufficient length of time to precharge the signal line to a desired neutral signal level between expected high and low signal values prior to connection of the short pin to its mate..

Early computer buses were literally parallel electrical buses with multiple connections, but the term is now used for any physical arrangement that provides the same logical functionality as a parallel electrical bus. Modern computer buses can use both parallel and bit-serial connections, and can be wired in either a multidrop (electrical parallel) or daisy chaintopology, or connected by switched hubs, as in the case of USB.

b. How pipelining would improve the performance of CPU justify. (4)

Answer:

Ans: Non-pipeline unit that performs the same operation and takes a time equal to (time taken to complete each task). The total time required for n tasks is n t. The speed up of a pipeline processing over an equivalent non-pipeline processing is defined by the ratio

$$S = nt_n / (k+n-1)t_p$$

As the number of tasks increases, n becomes much larger than k — 1, and K + n — I approaches the value of n, where K is segments of pipeline and Ip is time used to execute n tasks. Under this condition, the speed up becomes.

$$S = t_n / t_p$$

The time it takes to process a task is the same in the pipeline and non pipeline circuits. There if t = kt speed reduces to

$$S = k\, t_p / t_p = k$$

Maximum speed that a pipeline can provide is K, where K is number of segments in pipeline. Speed of pipeline process is improved the performance of C.P.U. To clarify the meaning of improving the performance of C.P.U. through speed up ratio, consider the following numerical example. Let the time it takes to process sub operation in each segment be equal to 20 ns. Assume that the pipeline k 4 segments and executes n 100 tasks in square. The pipeline system will take (k + n — 1) t = (4 + 99) 20 = 2060 ns to complete. Assuming that t = kt = 4 x 20 = 80ns, a non-pipeline system requires nktp = 100 x 80 8080 ns to complete 100 tasks. The speed up ratio is equal to 8000/2060 88. As the number of tasks increase, the

speed up will approach 4, which is equal to the number of segment in pipeline. It we assume that = 60ns, then speed up become=60/3.

c. Difference between control unit and main memory. (4)

Answer:

Ans: CPU is a separate entity from the main memory (known also as "RAM"), although it does work in close liason with RAM. Data and instructions flow between the CPU and RAM in both directions: items from RAM to the CPU may be instructions, such as "add two specific numbers together", or it may be a value itself which is going to be added to another.

But the control unit is the nucleus of the CPU. It is the part of the CPU which coordinates all of the activities going on within the computer, and manages the flow of data as it travels from place to place inside the machine.

There are three main functions of the control unit:

1)It reads & interprets program instructions
2)It oversees and directs the internal operations of the computer's components
3)It controls and manages the flow of programs and data as they travel backwards and forwards between RAM and the CPU.

d. Define Big-endian and Little-endian. (4)

Answer: Page No. 35 of text book

Q.3 a. Register 'A' is having S-bit number 11011001. (6)

Determine the operand and logic micro-operation to be performed in order to change the value in 'A' to.

(i) 01101101

(ii) 11111101

(iii) Starting from an initial value R = 11011101, determine the sequence of binary values in R after a logical shift left, followed by circular shift right, followed by a logical shift right and a circular shift left.

Answer:

Ans. (1) 11011001 A Register
10110100 B Register
01101101 A register after operations.

The selective complement operation complements the bits in register A where there is 1 in the corresponding bit of register B. This does not affect the bit value in A. Where there are 0 in the corresponding bit of register B.

(ii) 11011001 A register
00100100 B register
11111101 A register after operation.

The selective set operation sets the bit in register A to 1. Where there is 1 in corresponding bit of register B. This does not affect the bit value in. A where there are 0 in corresponding bit of register B.

(iii) 11011101 R register
10111010 R register after logical shift left
01011101 R register after circular shift right
00101110 R register after logical shift right
01011100 R register after circular shift left.

b. Briefly explain instruction format. (4)

Answer:

Ans. An instruction contain number of bits in the so that it is being to perform specific operation. Generally an instruction is divided into three fields

Addressing mode: It specifies that how the operands are accessed in an instruction.
Operation code (O):This field specifies the operation that is performed in the operand.
Operand : It specifies the data on which operation is performed.

c. If a Computer has 128 operation codes and 512 k addresses, how many bits would be required for
(i) Single address instruction
(ii) Two address instruction (6)

Answer:

Ans: No. of Op codes = $128 = 2^7$

Size of memory = 512 K = $2^8 \times 2^{10}$ bits.
(a) Size of single address instructions = 7 + 18 = 25 bits.
(b) Size of two address instruction = 7 + 2(18) = 7+36 = 43 bits.

Q.4 a. What do you mean by DMA channel? (4)

Answer:

DMA channel: DMA channel is issued to transfer data between main memory and peripheral device in order to perform the transfer of data. The DMA controller access rs address and data buses.
DMA with help of schematic diagram of controller ontile needs the dual circuits of and e to communicate with - CPU and I/O device. In addition, it nee s an address register; a word count register, and a set of, es The address register and address lines are used rec communication with memory to word count register specifies the no. of word that - must be trEia transfer may be done directly between the device and memory .

b.What is the sequence of steps that will take place when an interrupt occurs? (6)

Answer:

When an interrupt is recognized the following steps are carried out by the processor-

1. Complete the execution of current instruction.
2. Document the stack pointer. SP ← SP-1.
3. Save the program counter content in to stack
PC M SP[ ] ← .
4. Save the contents of processor registers.
5. Send interrupt acknowledgement signal to interrupt controller.
6. Transfer the vector address of the corresponding interrupt to program counter.
7. Disable the interrupt enable FF, so that other interrupt signal can't be recognized till the end of ISR.
8. Go to fetch the first instruction of ISR & execute the ISR.

When the processor came access the return instruction of ISR, it dies the following-

1. activate the interrupt enable FF to allow it to be interrupted.
2. restore contents of processor registers.
3. restore the return address saved in stack in to PC.
4. continue execution of main program.

c. When a DMA module takes control of bus and while it retain control of bus, what does the processor do? (6)

Answer:

Ans. The CPU communicates with the DMA through the address and data buses as with any interface unit. The DMA has its own address, which activates the 1)5 and RS lines. The CPU initializes the DMA through the data bus. Once the DMA receives the start control command, it can start the transfer between peripheral device and the memory. When the peripheral device sends a DMA request, the DMA controller activates the BR line, informing the CPU responds with its HG line, informing the DMA that its buses are disabled. The DMA then puts the current value of its address register into the address bus, initiate the RD or WR signal and sends a DMA acknowledge to the peripheral device. Note that RD and WR lines in DMA controller are bidirectional. The direction of transfer depends on the status of BG line. When BG 0, the RD and WR are input lines allowing the CPU to communicate with internal DMA registers. When BC = 1, the RD and WR are output lines from DMA controller to the random access memory to specify the read or write operation for the data. When the peripheral device receives a DMA acknowledge, it puts a word in the data bus (for write) or receives a word from the data bus (for read). Thus the DMA controls the read or write operations and supplies the address for the memory. The peripheral unit can then communicate with memory through the data bus for direct transfer between the two units while the CPU is momentarily disabled.

Q.5 a. Define interface circuit. Explain the function of an I/O interface. (8)

Answer:

Ans: An I/O interface consists of the circuitry required to connect an I/O device to a computer bus. On one side of the interface, we have bus signals. On the other side, we have a data path with its associated controls to transfer data between the interface and the I/O device – port. We have two types:

Serial port and
Parallel port

A parallel port transfers data in the form of a number of bits (8 or 16) simultaneously to or from the device. A serial port transmits and receives data one bit at a time. Communication with the bus is the same for both formats. The conversion from the parallel to the serial format, and vice versa, takes place inside the interface circuit. In parallel port, the connection between the device and the computer uses a multiple-pin connector and a cable with as many wires. This arrangement is suitable for devices that are physically close to the computer. In serial port, it is much more convenient and cost-effective where longer cables are needed.

b. Describe Peripheral Component Interconnect (PCI) Bus Standards. (8)

Answer: Page No. 261 of text book

Q.6 a. What do you mean by memory hierarchy? Explain cache memory. (6)

Answer:

Ans: Memory is technically any form of electronic storage. Personal computer system have a hierarchical memory structure consisting of auxiliary memory (disks), main memory (DRAM) and cache memory (SRAM). A design objective of computer system architects is to have the memory hierarchy work as through it were entirely comprised of the fastest memory type in the system.

Cache Memory

Cache memory: Active portion of program and data are stored in a fast small memory, the average memory access time can be reduced, thus reducing the execution time of the program. Such a fast small memory is referred to as cache memory. It is placed between the CPU and main memory.

b. Differentiate between direct mapping and associate mapping. (4)

Answer:

Ans. Direct mapping : The direct mapped cache is the simplest form of cache and easiest to check for a hit. There is only one possible place that any memory location can be cached, there is nothing to search. The line either contain the memory information it is looking for or it does not. Associate mapping : Associate cache is content addressable memory. The cache memory does not have its address. Instead this memory is being accessed using its contents. Each line of cache memory will accommodate the address and the contents of the address from the main memory. Always the block of data is being transferred to cache memory instead of transferring the contents of single memory location from main.

c. An 8-bit computer has a 16-bit address bus. The first 15 lines of address are used to select a bank of 32K bytes of memory. The higher order bit of address is used to select a register which receives the contents of the data bus? Explain how this configuration can be used to extend the memory capacity of system to eight banks of 32 K bytes each, for a total of 256 bytes of memory.

(6)

Answer:

Ans. The processor selects the external register with an address 8000 hexadecimal.
Each bank of 32K bytes are selected by address 0000—7 FFF. The processor loads an 8-bit number into the register with a single I and seven 0's. Each output of register selects one of the 8 banks of 32 bytes through 2-chip select input. A memory bank can be changed by changing in number in the register.

Q.7 a. What are the advantages of virtual memory? (4)

Answer:

Ans permit the user to construct program as though a large memory space were available, equal to totality auxiliary memory. Each address that is referenced by CPU goes through an address mapping from so called virtual address to physical address main memory.

There are following advantages we got with virtual memory:

1. Virtual memory helps in improving the processor utilization.
2. Memory allocation is also an important consideration in computer programming due to high cost of main memory.
3. The function of the memory management unit is therefore to translate virtual address to the physical address.
4. Virtual memory enables a program to execute on a computer with less m ain memory when it needs.
5. Virtual memory is generally implemented by demand paging concept In demand paging, pages are only loaded to main memory when they are required.
6. Virtual memory that gives illusion to user that they have main memory equal to capacity of secondary stages media.

The virtual memory is concept of implementation which is transferring the data from secondary stage media to main memory as and when necessary. The data replaced from main memory is written back to secondary storage according to predetermined replacement algorithm. If the data swajd is designated a fixed size. This concept is called paging. If the data is in the main e subroutines or matrices, it is called segmentation. Some operating systems combine segmentation and paging.

b. Define the terms: Seek time, Rotational Delay, Access time. (6)

Answer:

Ans .**Seek time** : Seek time is a time in which the drive can position its read/write ads over any particular data track. Seek time varies for different accesses in tie disk. It is preferred to measure as an average seek time. Seek time is always measured in milliseconds (ms).

Rotational Delay: All drives 1bve rotational delay. The time that elapses between the moment when the read/we heal\settles over the desired data track and the
moment when the first byte of required data appears under the head.

Access time: Access time is simply the sum of the seek time and rotational latency time.

c. Design a half adder as a 2 level AND OR circuit. Implement full adder circuit using 2 half adder. (6)

Answer: Not provided

Q.8 a. Explain the process of carry-save addition of summands. (8)

Answer: Page No. 385 of text book

b. Explain restoring division and non-restoring division process. Also, give the algorithms for the two process. (8)

Answer: Page No. 391-392 of text book

Q.9 a. What do you understand by Fetch cycle, instruction cycle, machine cycle? (6)

Answer:

Ans: **Fetch cycle :** The sequence counter is initialized to 0. The program counter (PC) contains the address the first instruction of a program under execution. The address of first instruction from PC is loaded into the address register (AR) during first clock cycle (To). Then instruction from memory location given by address register is loaded into the instruction register (IR) and the program counter is incremented to the address of next instruction in second clock cycle (TL).

Instruction cycle: A program in computer consists of sequence of instructions. Executing these instructions runs the program in computer. Moreover each instruction
is further divided into sequence of phases. The concept of execution of an instruction through different phases is called instruction cycle. The instruction is divided into sub
phases as specified ahead—

1. First of all an instruction in fetched (accessed) from memory.
2. Then decode that instruction.
3. Decision is made for memory or register or I/O reference instruction. In case

b. With suitable figure, discuss multiple-bus organization. (6)

Answer: Page No.423-424 of text book

c. Write the control sequence for execution of the instruction Add(R3), R1. (4)

Answer: Page No.421 of text book

TEXT BOOK

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