Q.2   **a. Differentiate between Electronics and Power Electronics. What are different devices used in both. Give some applications of Power Electronics.**

Answer:
Electronics and Power Electronics:
Electronics engineering is guided by distortion less production, transmission and reception of data and signals of very low power level, of the order of a few watts, or mill watts, without much consideration to the efficiency. Principles in electronics engineering are based upon physical phenomena in vacuum, gases/vapors and semiconductors.
Power electronics may be defined as a subject that deals with the apparatus and equipment working on the principle of *electronics* but rated at *power* level (i.e from few watts to several thousands of watts) rather than signal level. For example, semiconductor power switches such as thyristors, GTOs etc. work on the principle of electronics (movement of holes and electrons), but have high power ratings. Similarly, diodes, mercury-arc rectifiers and thyratrons (gas-filled triode), high-power level devices, form a part of the subject power electronics; because their working is based on the physical phenomena in gases and vapours, an electronic process.

Devices used:

Diodes, BJTs, Zener diodes, op-amp etc are used in electronics.

SCRs, TRIACs, GTOs, Power diodes, MOSFETs etc are used in Power Electronics.

Applications:

Power electronics is used in controlled converters for variable DC supply, static switches, static relays, cycloconverters for variable frequency ac, speed control of motors, power factor control in ac supply lines (FACT controllers) etc.
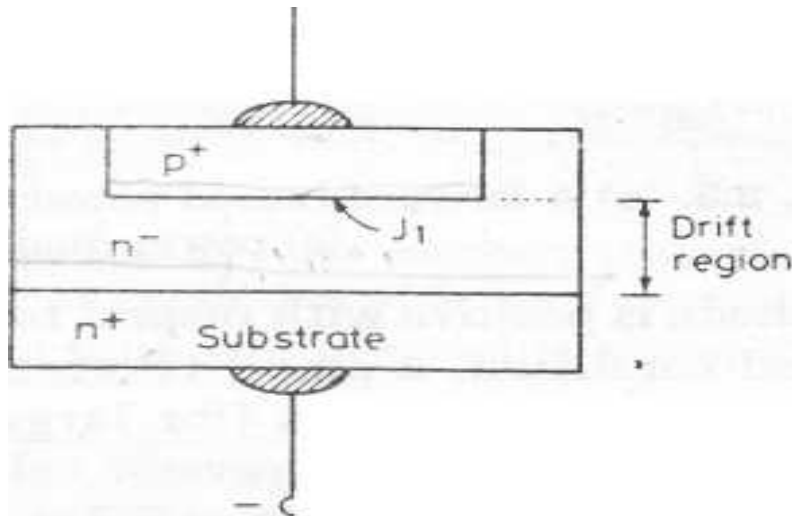
     b.
       (i) How Power diode is different from signal diode.
       (ii) Explain Schottky Diode.

Answer:

(i) Power diodes differ in structure from signal diodes. A signal diode constitutes a simple p-n unction. The Power diodes are made suitable for high-voltage and high-current applications.

The practical realization and the resulting structure of a power diode is shown in above Fig. It consists of heavily doped n^+ substrate. On this substrate, a lightly doped n^- layer is epitexially grown. Now a heavily doped p^+ layer s diffused into n^- layer to form **the anode** of power diode. The function of n^- layer is to absorb the depletion layer of the reverse biased *P-N* junction. The break-down voltage needed in a power diode governs the thickness n^- layer. Greater the breakdown voltage required, more is the n^- layer thickness.

(ii) This class of diodes use metal-to-semiconductor junction instead of *p-n* junction. The metal is usually aluminum and semiconductor is silicon. Therefore, a Schottky diode has aluminum-silicon junction. The silicon is n type.

Since metal does not have any holes, forward current is due to the movement of electrons only. Due to absence of holes, there is no storage charge and no-reverse recovery time. The turn-off delay caused by recombination is avoided. As such, Schottky diode can switch off much faster than *p-n* junction diode.

As compared to *p-n* junction diode a Schottky diode has lower cut-in voltage, higher reverse leakage current and higher operating frequency. Their reverse voltage ratings are limited to about 100 V and forward current ratings vary from 1 A to 300 A. Applications of Schottky diode include high-frequency instrumentation and switching power supplies.
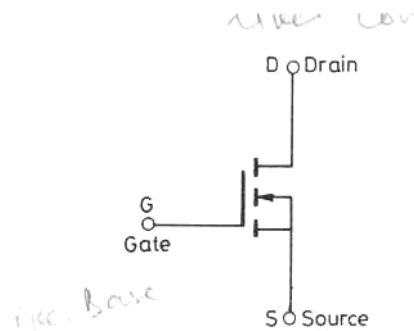
Q.3 **a. Explain the working principle of a Power MOSFET.**

Answer:

A power MOSFET has three terminals called drain (D), source (S) and gate (G). A BJT is a current controlled device whereas a power MOSFET js a voltage-controlled device. the gate circuit impedance in MOSFET is extremely high, of the order of 10^9 ohm.
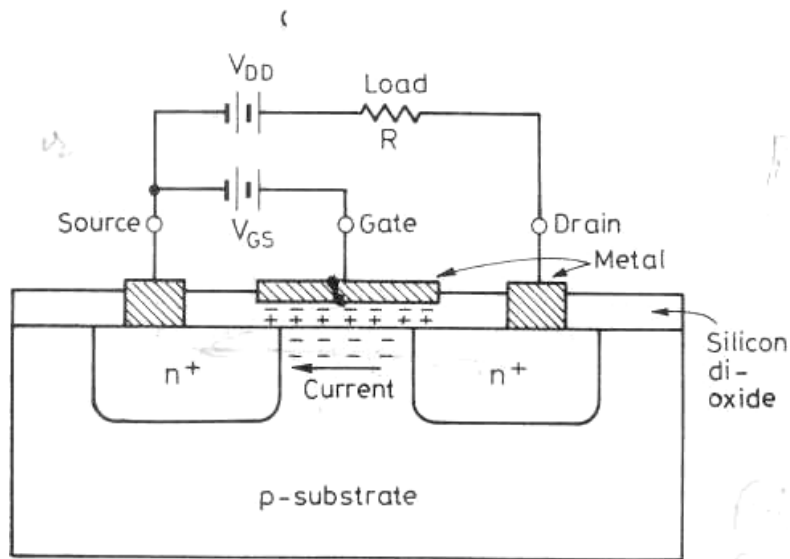
N channel enhancement power MOSFET

Symbol

N channel enhancement MOSFET is more common because of higher mobility of electrons.

A simplified structure of n-channel planar MOSFET of low power rating is shown in above Fig. On p-substrate (or body), two heavily doped n^+ regions are diffused as shown. An insulating layer of silicon dioxide (SiO_2) is grown on the surface. Now this insulating

layer is etched in order to embed metallic source and drain terminals. Note that n^+ regions make contact with source and drain terminals as shown. A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET in between source and drain terminals.

When gate circuit is open, junction between n^+ region below drain and p-substrate is reverse biased by input voltage V_{DD}. Therefore, no current flows from drain to source and load. When gate is made positive with respect to source, an electric field is established as shown in Fig. Eventually, induced negative charges in the p-substrate below SiO_2 layer are: formed thus causing the p layer below gate to become an induced n layer. These negative charges, called electrons, form n-channel between two n^+ regions and current can flow from drain to source. If V_{GS} is made more positive, induced n-channel becomes more deep and therefore more current flows from D to S. This shows that drain current I_D is enhanced by the gradual increase of gate voltage, hence the name enhancement MOSFET.

The main disadvantage of n-channel planar MOSFET is that conducting n-channel in between drain and source gives large on-state resistance. This leads to high power dissipation in n-channel.

The V-I characteristics of power MOSFET is shown below.
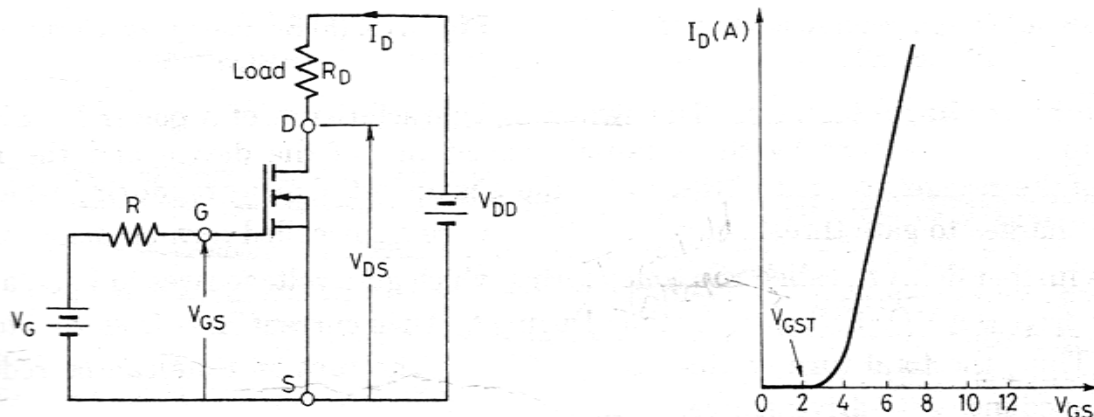
V-I Characteristics

b. Explain the working principle of UJT with corresponding VI characteristics.

Answer:

An UJT is made up of an n-type silicon base to which p-type emitter is embedded. The n-type base is lightly doped whereas *p*-type is heavily doped. An UJT has three terminals, namely the emitter E, base-one B_1 and base-two B_2. Between bases B_1 and B_2, the unijunction behaves like an ordinary resistance.
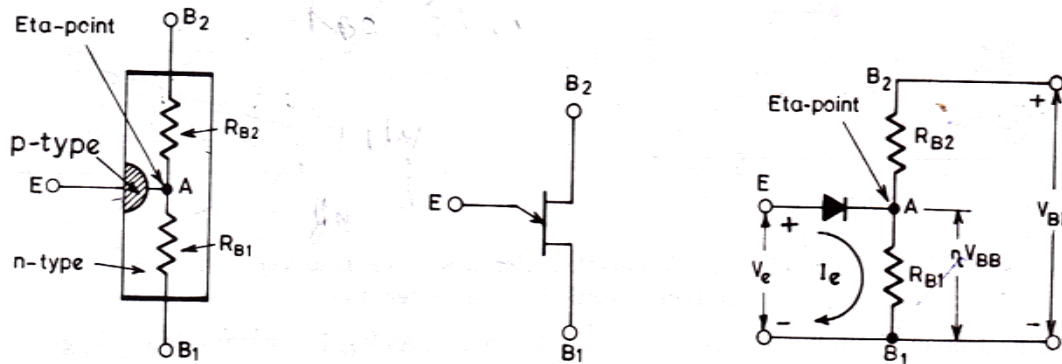

R_{B1} and R_{B2} are the internal resistances respectively from bases B_1 and B_2 to eta point A. When a voltage V_{BB} is applied across the two base terminals B_1 and B_2, the potential of point A with respect to B_x is given by

$$V_{AB1} = \frac{V_{BB}}{R_{B1} + R_{B2}} \cdot R_{B1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \cdot V_{BB} = \eta \, V_{BB}$$

η is called the *intrinsic stand-off ratio.*

Since emitter is nearer to B_2, resistance R_{B2} is less than the resistance R_{B1}. The UJT is usually operated with both B_2 and E biased positive with respect to reference base terminal B_1.

The magnitude of voltage V_e can be varied by regulating external resistance R_E. As long as emitter voltage $V_e < \eta.V_{BB}$, the $E-B_1$ junction is reverse biased and emitter current I_e is negative as shown by curve shown below.
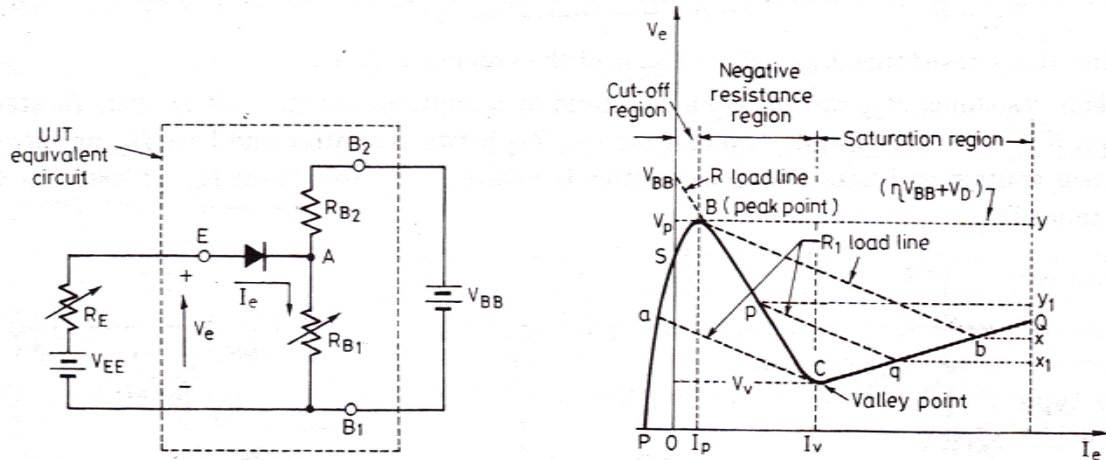
The resistance between E–B_1 junction is very high. At point S, $I_e = 0$, drop across R_E is zero, therefore V_e = source voltage, $V_{EE.}$

The off-state of UJT extends to a point where emitter voltage V_e exceeds V_A, or η.V_{BB}, by diode voltage V_D in E - B_1 junction. So when V_e = η. $V_{BB} + V_D$, point B is reached and E - B_1 junction gets forward biased to allow forward current through the diode.

Point B is called the peak point. By varying R_E, V_e is increased till V_e approaches V_p. At this peak point, $V_e = V_p = $ η.$V_{BB} + V_D$, the p-emitter begins to inject holes from the heavily doped emitter E into the lower base region B_1. As n type base is lightly doped, the holes rarely get any chance to recombine. The lower base region B_1 is, therefore, filled up with additional current carriers (holes). As a result, resistance R_{B1} *of E -B1* junction decreases. The fall in R_{B1} causes potential of eta point A to drop.

This drop in V_A, in turn, causes V_e (= V_A + V_D) to fall. As V_{EE} is constant, fall in V_e gives rise to more emitter current I_e (= (V_{EE} - V_e)/R_E). This increased I_e injects more holes into region B_1, thereby further reducing the resistance R_{B1} and so on. This *regenerative* effect continues till R_{B1} has dropped to a small value (from about 4 kΩ to around 2 to 25 Ω.). The emitter current is limited by external resistance R_E,

When R_{B1} has dropped to a very small value, indicated by point C in Fig, the UJT has reached 'on' state. At point C, entire base region B_1 is saturated and resistance R_{B1} cannot decrease any more. This point C is called the *valley point*. After valley point is reached, an increase in V_e is accompanied by an increase in I_e. At point Q, V_e is a little more than its valley point voltage V_v. Between points B and C, emitter voltage V_e falls as I_e increases; UJT, therefore, exhibits negative resistance between these two points.

Q.4   **a. Explain protection scheme used for different kinds of protection of an SCR**

Answer:

The SCR has to be protected from different kind of abnormal conditions. For this different devices are used with SCR for its protection. One of the protection scheme for SCR protection is given below. It protects the SCR form following abnormal conditions:
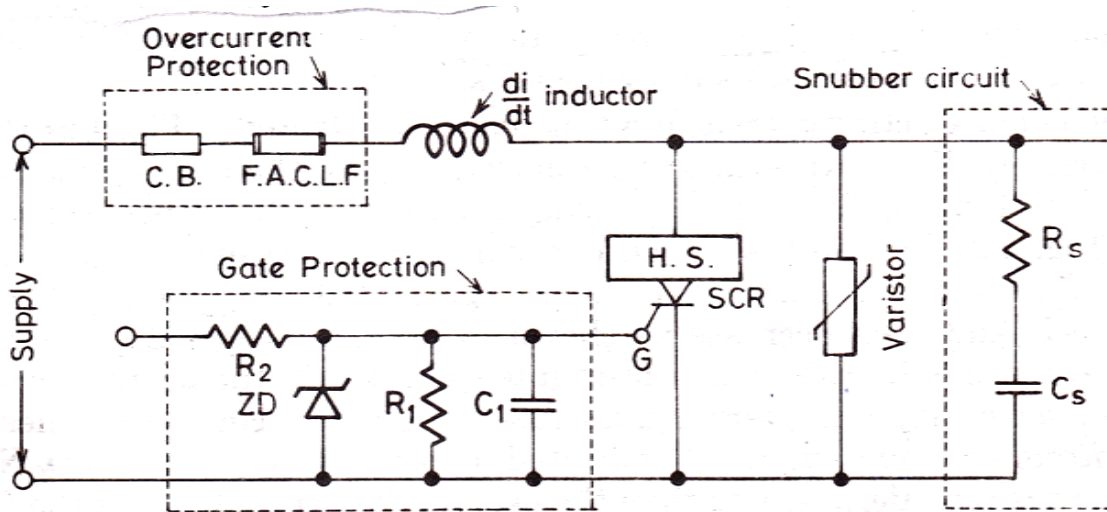
1)   **di/dt protection:**

When the rate of increase of current in an SCR increases beyond a limit, it creates local hot spots in SCR and can damage it. The value of di/dt can be maintained below limits by using small inductor called di/dt inductor. It is connected in series with SCR.

2)   **dv/dt protection:**

If dv/dt is very high, then it can turn on the SCR. To avoid this, snubber circuit is used as shown in the fig above. It consists of a resistor and a capacitor connected in series. Both are connected in parallel with SCR. Due to charging of this capacitor, the voltage builds slowly, across capacitor as well as across SCR. Resistor only limits the discharge current.

3)   **Over voltage protection:**

For over voltage protection, varistors are used. The resistance of varistor abruptly decreases with increase in voltage beyond certain limit. So at high voltage it acts like short circuit, causing fuse to melt.

4) Over current Protection:

Fuses and circuit breakers are used for over current protection, as shown.

5) Gate protection:

Gate should also be protected from over voltage and over current. Resistance R_2 is connected for over current protection and Zener diode ZD is used for over current protection. Capacitor C_1 is used for dv/dt protection of gate. Also shielded gate leads are used for protection against spurious firing.

6) Over heat protection:

Heat sink is used for over heat protection of an SCR.

b. What are different commutation methods used for SCRs. Explain complimentary commutation scheme in detail.

Answer:

The different commutation methods used for SCRs are:

1) Class A or Load commutation.

2) Class B or Resonant pulse commutation.

3) Class C or Complementary commutation.

4) Class D or Impulse commutation.

5) Class E or External pulse commutation.

6) Class F or Line commutation.

Class C or Complementary commutation:

In this type of commutation, a thyristor carrying load current is commutated by transferring its load current to another incoming thyristor.
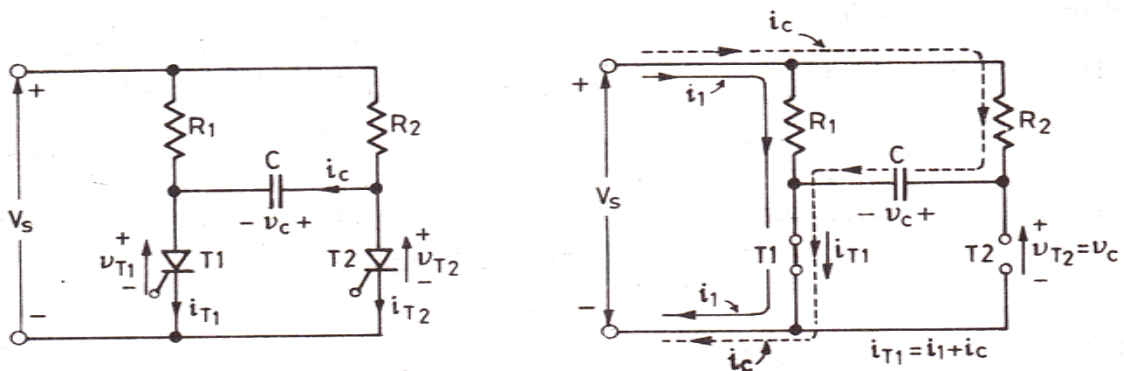
The figure above shows the configuration of Complementary commutation. In this the firing of SCR T1 commutates T2 and subsequently, firing of SCR T2 would turn off T1.

In this figure, capacitor is supposed to be initially uncharged. When Tl is turned on at t = 0, current begins to flow through it. Capacitor C begins charging through R2 from $v_c = 0$. After sometime, when transients are over, $v_c = v_{T2} = V_s$ and i_c decays to zero.

When Tl is to be turned off, T2 is triggered. If T2 is turned on at t_1, then capacitor voltage v_c applies a reverse potential Vs across SCR T1 and turns it off. Now the capacitor C starts charging in reverse direction through R1.

Similarly, at t_3, with the triggering of T1 capacitor voltage Vs applies a sudden reverse bias across T2 to turn it off. On account of this, class-C commutation is also called complementary impulse commutation.

The waveforms for these currents and voltages are shown below.
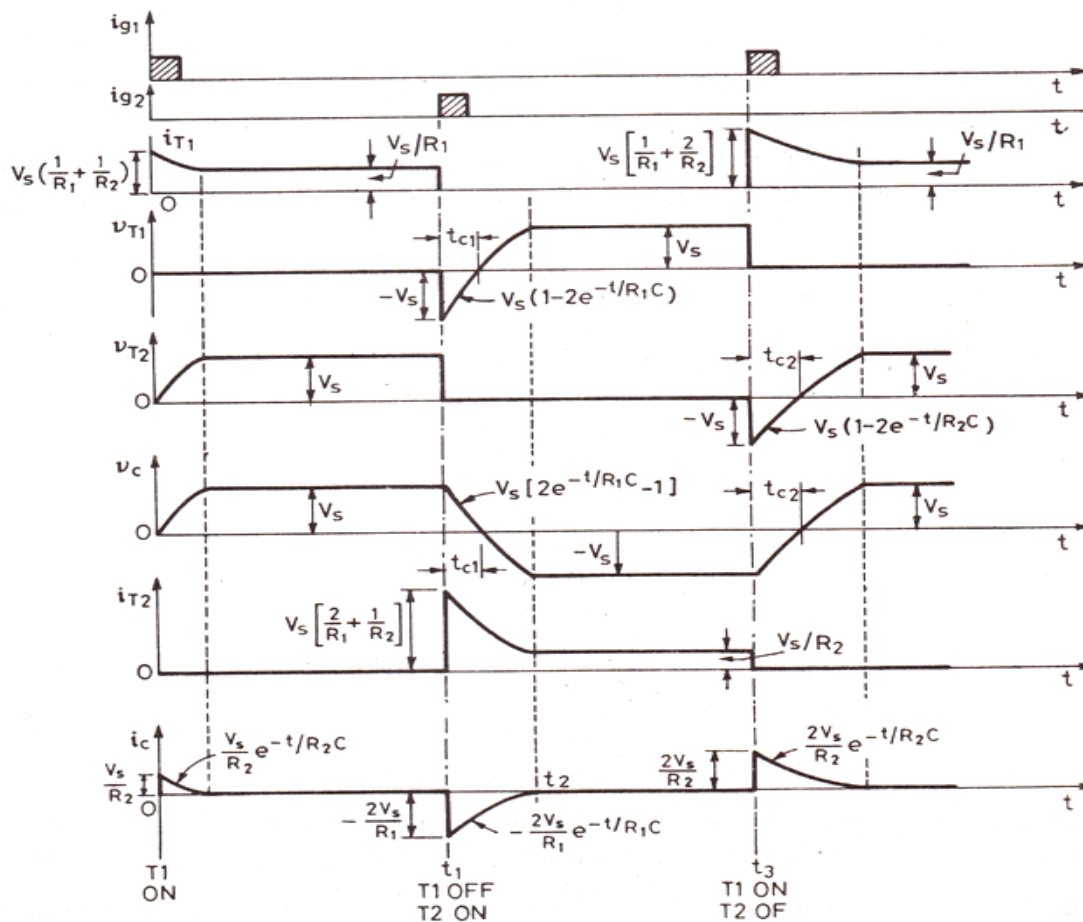
Q.5   **a. Explain the circuit diagram and output waveforms of Single Phase, Full Wave, fully Controlled Bridge Rectifier with Resistive load.**
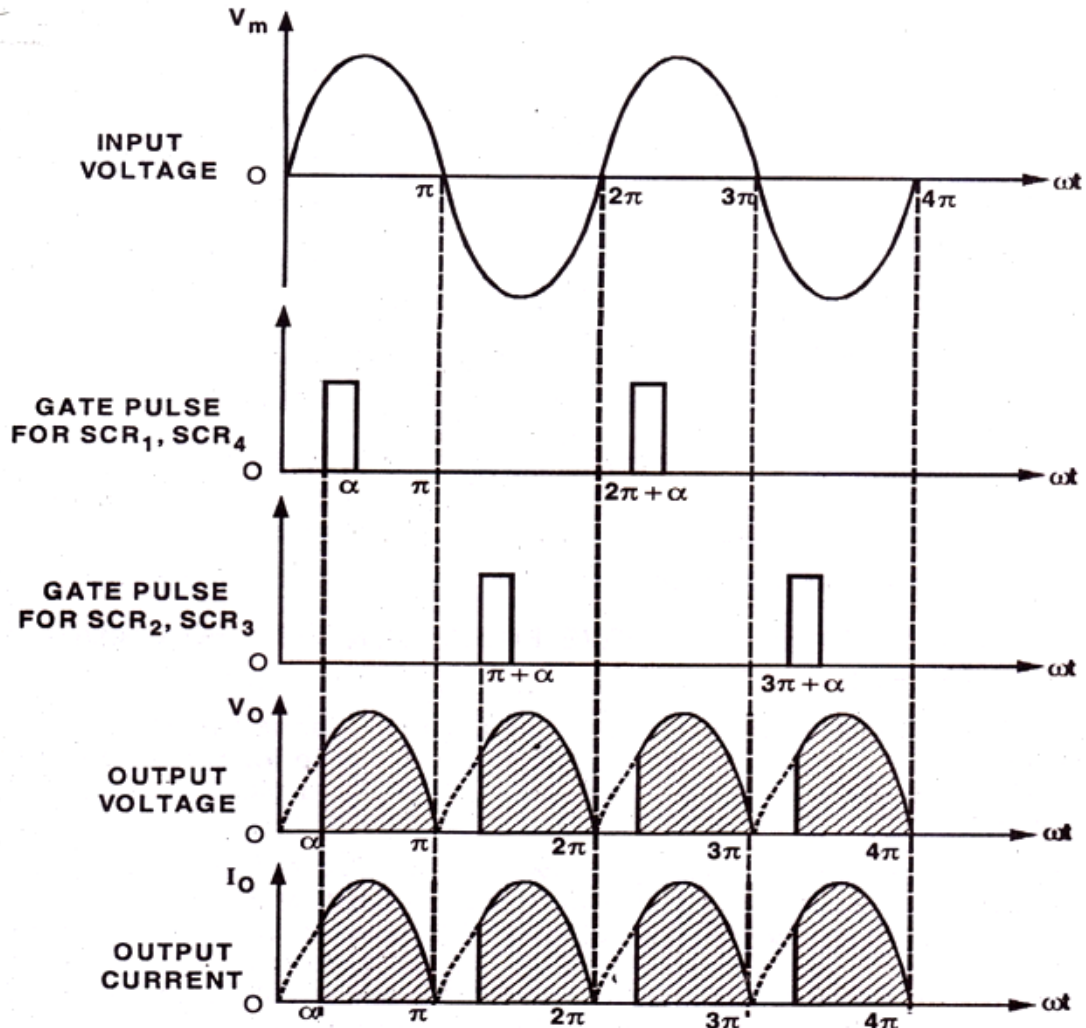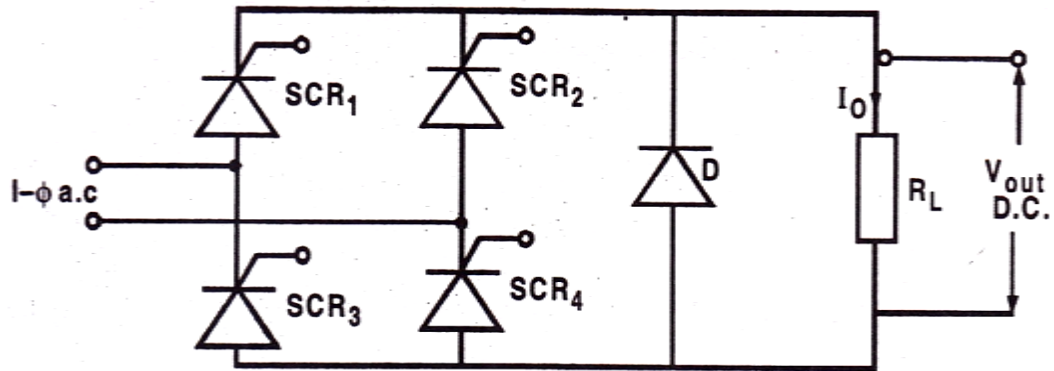
Answer:

Fig. above shows an arrangement for a single phase full wave fully controlled bridge rectifier. In this circuit, four SCRs are used to form the rectifier bridge. In positive half cycle of a.c. input supply, SCR$_1$ and SCR$_4$ are forward biased and conduct the current through load.

During the negative half cycle, SCR$_2$ and SCR$_3$ are forward biased and conduct the current through load. SCR$_1$ & SCR$_4$ in positive half cycle and SCR$_2$ & SCR$_3$ in negative half cycle are fired at some suitable firing angle, to get controlled dc output voltage. With the increase in firing angle, average dc output voltage decreases.

A full wave controlled rectified d.c. output, therefore, will be available across the load. For positive half cycle, SCR$_1$ and SCR$_4$ are responsible for controlling the output. Similarly, for negative half cycle, SCR$_2$ and SCR$_3$ are responsible for controlling the output. So all the four SCRs are involved in controlling both halves of the a.c. input and hence is the name fully controlled rectifier.

The diode D is connected in the circuit to obtain freewheeling action. This will provide a low resistance path to the current due to the stored energy In case of inductive loads. In present case of resistive load, it will not come in to action.

b. What is a dual converter? Explain non circulating current type dual converter.

Answer:

(a)   (b)
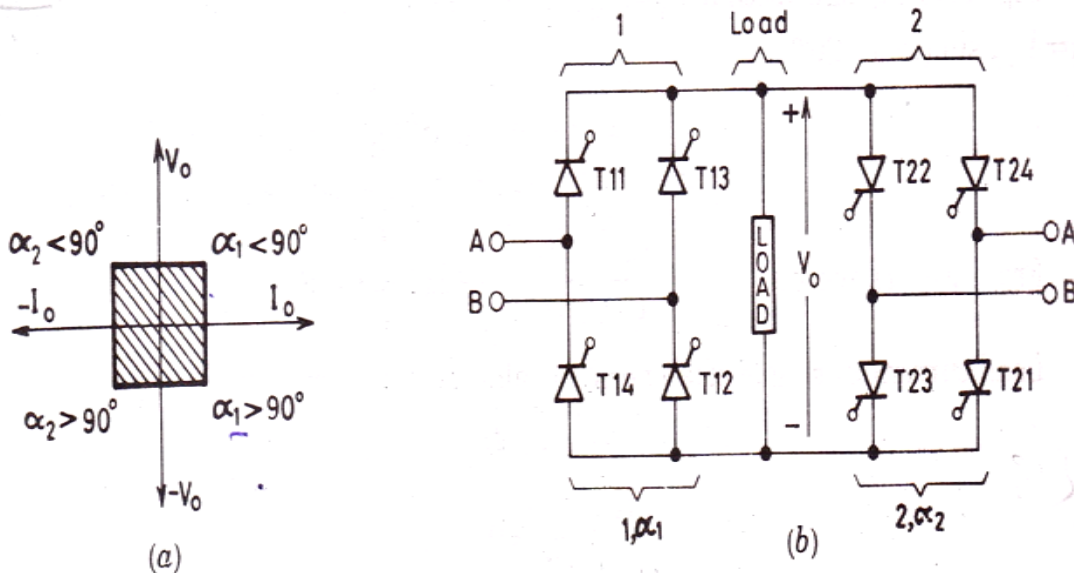
Semi-converters are single quadrant converters. This means that over the entire firing angle range, load voltage and current have only one polarity. In case four quadrant operation is required without any mechanical changeover switch two full converters can be connected back to back to the load circuit. Such an arrangement using two full converters in anti parallel and connected to the same dc load is called a dual converter. There are two modes of a dual converter, one is non-circulating-current mode and the other is circulating-current mode.

Dual Converter without Circulating Current:

With non-circulating current dual converter, only one converter is in operation at a time and it alone carries the entire load current. Only this converter receives the firing pulses from the trigger control. The other converter is blocked from conduction. This is achieved by removing the firing pulses from this converter.

Suppose converters 1 is in operation and is supplying the load current. For blocking convertor 1 and switching on converter 2, first firing pulses to converter 1 are immediately removed. With this, load current would decay to zero and then only converter 2 is made to conduct by applying the firing pulses to it. Now the current in converter 2 would build up through the load in the reverse direction. So long as converter 2 is in operation, converter 1 is idle as firing pulses are withdrawn from it. It should be ensured that during changeover from one converter to the other, the load current must decay to zero. After the outgoing converter has stopped conducting, a delay time of 10 to 20 msec is introduced before the firing pulses are applied to switch on the incoming converter. This time delay ensures reliable commutation of SCRs of the outgoing converter.

Q.6   **a Explain 3ϕ half wave controlled rectifier with R-L load. Draw various waveforms at firing angle of 45 degrees.**

Answer:
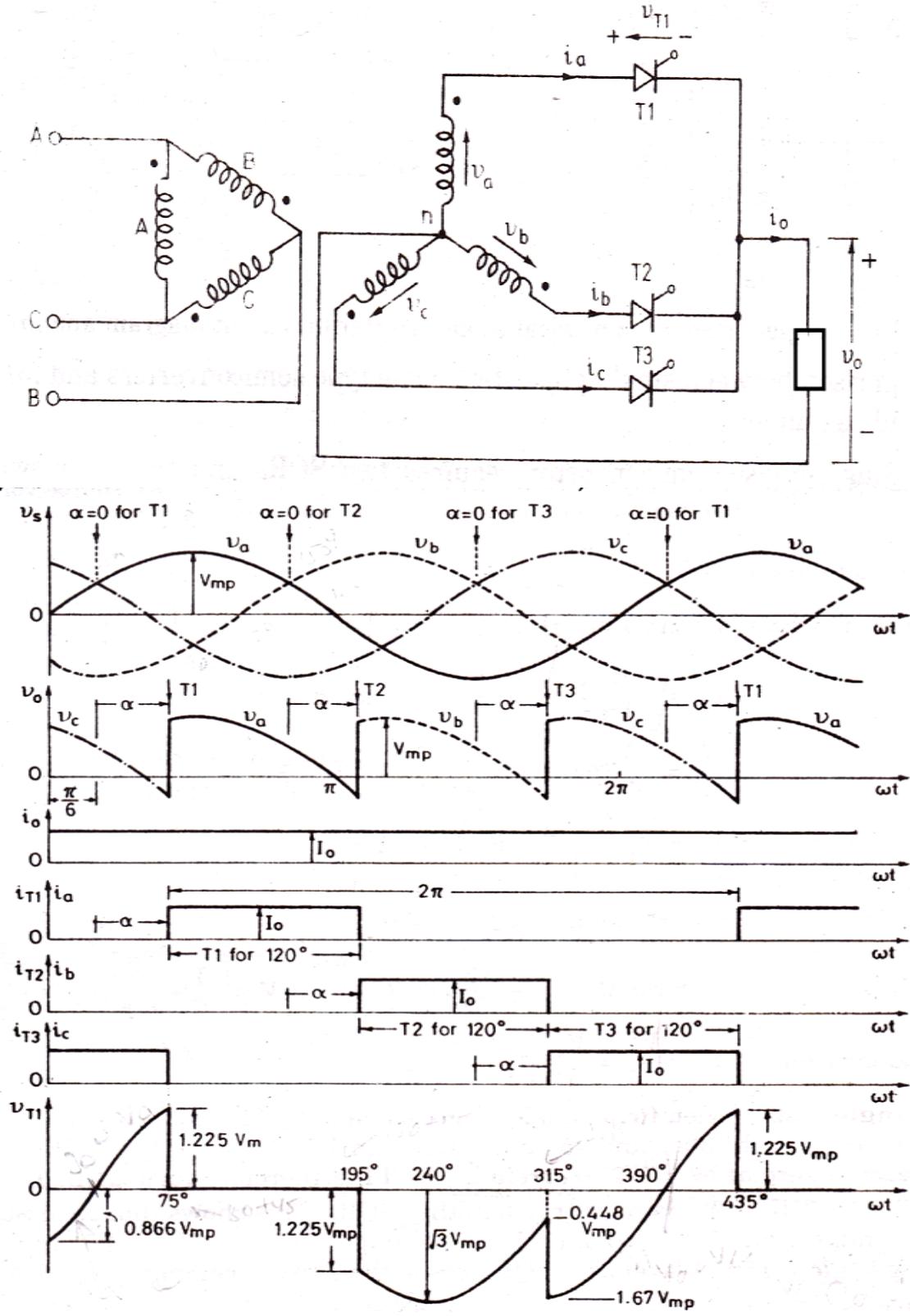
3Ø half wave controlled rectifier:

Power circuit diagram of this converter is shown in Fig above. For resistive load, if firing angle is zero degree, SCR T1 would begin conducting from 30° to 150°, *T2* from 150° to 270° and T3 from 270° to 390° and so on. For zero degree firing angle delay, thyristor behaves as a diode.

3Ø half wave controlled rectifier with R-L Load:

The load inductance *L* is large so that load current is continuous and constant at I_0. For the firing angle of 45°, the various waveforms are shown in fig. given above.

In this, *T1* conducts from 30 + α to 150 + α, *T2* from 150 + α to 270° + α, *T3* from 270° + α to 390° + α and so on. Thus, each SCR conducts for 120°.

At $\omega t = \pi$, phase voltage v_a is zero, but i_{T1} is not zero because of RL load. Therefore, Tl would continue conducting beyond $\omega t = \pi$. As such, $v_0 = v_a$ goes negative beyond $\omega t = \pi$. When T_2 is turned on at $\omega t = 150° + \alpha$, load current shifts from T1 to T2 and a voltage $v_a - v_b = [V_m \sin(150 + \alpha) - V_m \sin(30 + \alpha)]$ appears as reverse bias across T1 to aid its commutation. SCR T2 conducts from (150° + α,) to (270° + α) and so on. The waveform for i_{T1}, i_{T2} and i_{T3} are also shown above.

b. Explain the working principle of a $^{3\phi}$, full wave, half controlled rectifier with circuit diagram and output waveforms.

Answer:
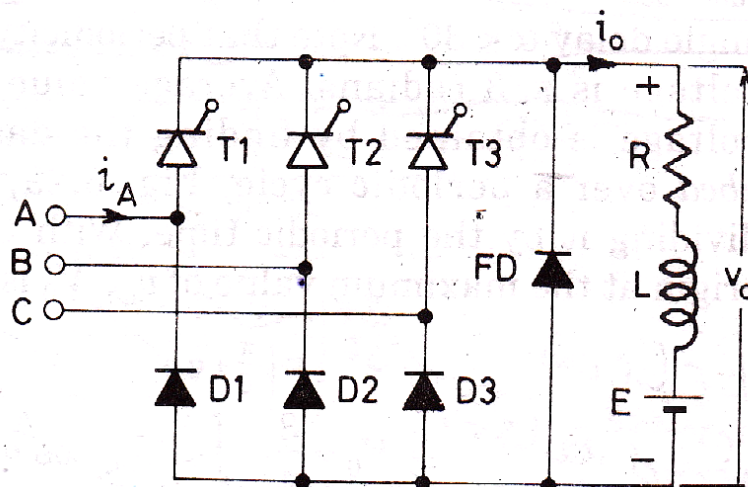
Three-phase balanced supply is given to the three input terminals A, B, C.

The output voltage v_o across the load terminals is controlled by varying the firing angles of SCRs T1, T2 and T3. The diodes Dl, D2 and D3 provide merely a return path for the current to the most negative line terminal.

The semi converter bridge operation for different firing angles is shown in given voltage and current waveforms. The conduction angles for the SCRs, diodes or FD are also shown.
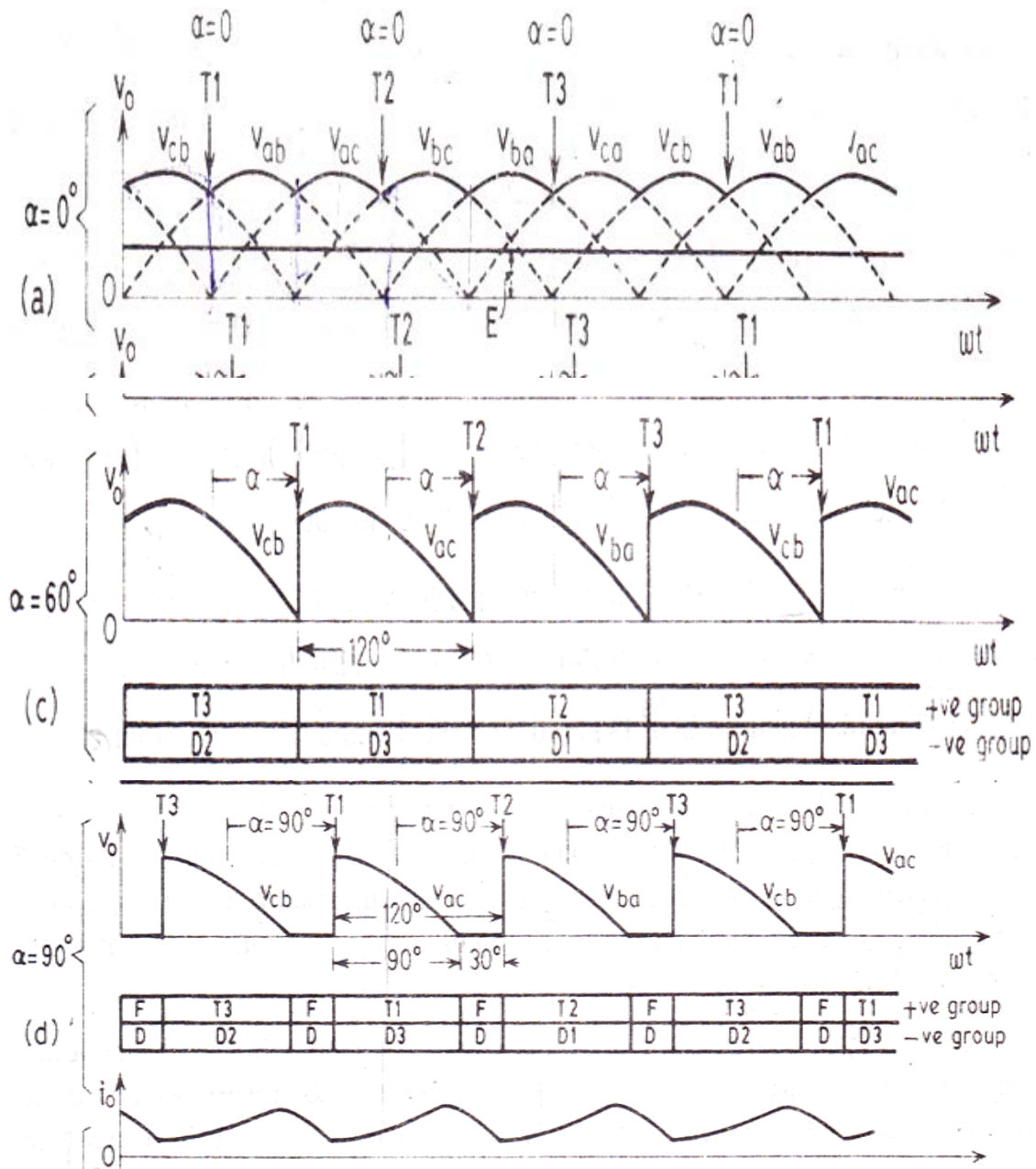
For a firing angle delay of α = 0°, thyristors T1, T2, T3 would behave as diodes and the output voltage of semi converter would be symmetrical six-pulse per cycle as shown.

When the firing angle is delayed to some angle α, the triggering of SCRs T1, T2, T3 is delayed but return diodes Dl, D2, D3 remain unaffected. The load current is continuous and has little ripple. The FD comes into play when output voltage tends to become negative. In this case FD gets forward biased and gives easy path for flow of current, keeping output voltage zero. It happens for a firing angle greater than 60°.

This case is shown above where firing angle is 90°. In conduction angle of SCRs and diodes is seen to be less than 120° for every output pulse. The conduction angle for both positive and negative group elements is 90° and for the remaining 30°, current completes its path through FD as shown. For this period, the output voltage is zero.

Without FD, after load voltage v_0 reaches zero, a diode from negative group would begin to conduct reducing v_0 to zero till next SCR in sequence is triggered, For example, *at* ωt = 120°, $v_0 = v_{cb} = 0$ and without FD, D3 from negative group would start conducting through T3 from ωt = 120° to 150° when SCR T1 is gated. This means that without FD, T3 would conduct for 120° from ωt = 30° to 150°, D2 for 90° from ωt = 30° to 120° and D3 for 30° from ωt = 120° to 150° for this periodic cycle of 120° extending from ωt = 30° to 150°.

In 3 phase semi converter, SCRs are gated at an interval of 120° in a proper sequence. A three-phase semi converter has the unique feature of working as a six-pulse converter for α < 60° and as a three-pulse converter for α > 60°.

Q7 a. Explain the working principle of Bulk-Boost Chopper with the help of circuit diagram and waveforms.

Answer: Page Number 295-298 of Text Book

  b. A step up chopper has input voltage of 220V and output voltage of 660V. If the conducting time of thyristor chopper is 100μSec, compute the pulse width of output voltage. In case the thyristor off period is halved for constant frequency operation, find the average value of new output voltage.

Answer:

For a step up chopper:

Output voltage $V_o = V_s \cdot [1/(1 - \alpha)]$

So $660 = 220 \cdot [1/(1 - \alpha)]$

Or $1 - \alpha = 220/660$

$= 1/3$

Or $\alpha = 1 - 1/3$

$= 2/3$

Now $\alpha = T_{on}/T$

So $T_{on}/(T_{on} + T_{off}) = 2/3$

Now $T_{on} = 100 \mu$ Sec

So $100/(T_{on} + T_{off}) = 2/3$

Or $(T_{on} + T_{off}) = 100 \times 3/2 = 150 \mu$ Sec

So pulse width of output voltage $= T_{off} = 150 - T_{on}$

$= 150 - 100 = 50 \mu$ Sec (Ans)

When off period is halved:

$T_{off} = 50/2 = 25 \mu$ Sec

For constant frequency operation, $T = 150 \mu$ Sec

So $T_{on} = 150 - 25 = 125 \mu$ Sec

$\alpha = T_{on}/T = 125/150$

$= 5/6$

$V_O = 220 \cdot [1/(1 - 5/6)]$

$= 1320$ V (Ans)

Q8. a. What are various methods of pulse width modulation in invertors and explain sinusoidal pulse width modulation.

Answer: Page Number 321-324 of Text Book

b. What are Ideal Current Source Inverters? How they are different from voltage source inverters.

Answer:

**Current Source Inverters Vs. voltage source inverters:**

In voltage-source inverters, input voltage is maintained constant and the amplitude of output voltage does not depend on the load. However, the waveform of load current as well as its magnitude depends upon the nature of the load impedance.

In the current-source inverters (CSIs), input current is constant but adjustable. The amplitude of output current from CSI is independent of the load. However, the magnitude of output voltage and its waveform output from CSI is dependent upon the nature of load impedance.

A CSI does not require any feedback diodes, whereas these are required in a VSI. Commutation circuit is simple, as it contains only capacitors. As power semi-conductors in a CSI have to withstand reverse voltage, devices such as GTOs, power transistors, power MOSFETs cannot be used in a CSI.

Single-phase CSI with Ideal Switches:

A single-phase CSI with ideal thyristors is shown in Fig. below. Here a thyristor is assumed an ideal switch with zero commutation time.
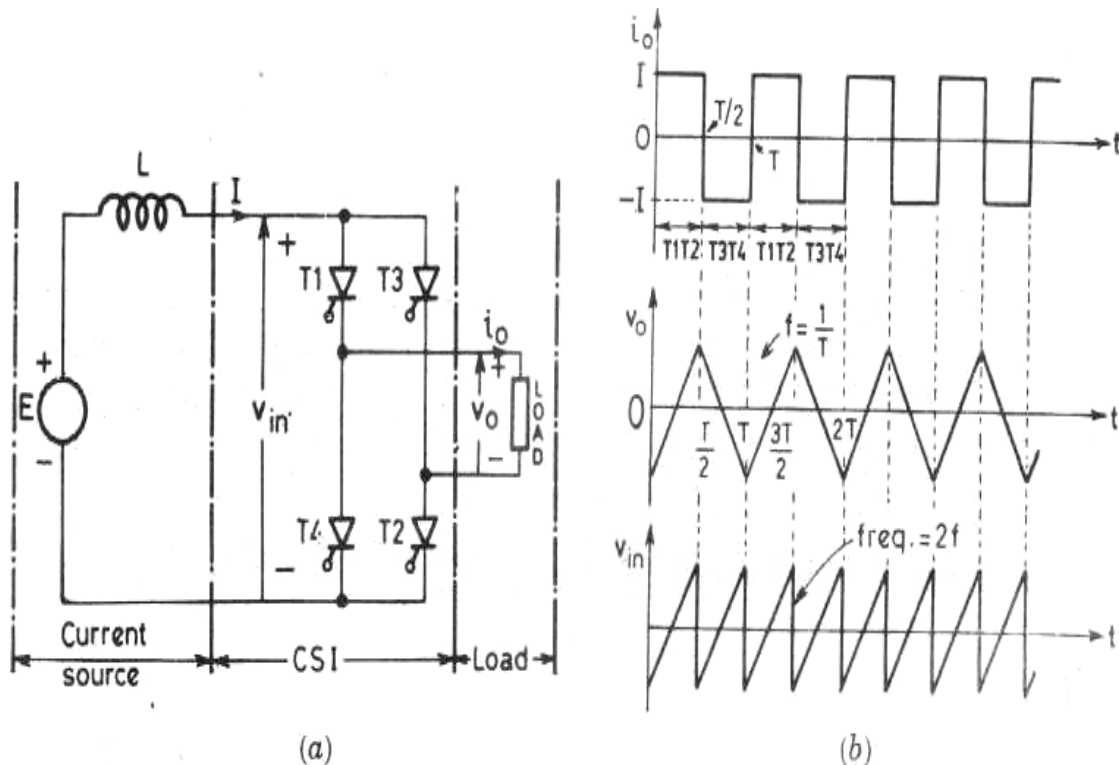
(a) Power circuit diagram and (b) waveforms for an ideal single-phase CSI

The dc input to CSI is obtained from a fixed voltage ac source through a controlled rectifier bridge, or through a diode bridge and a chopper. In order that current input to CSI is almost ripple free, L-filter is used before CSI.

A CSI converts the input dc current to an ac current at its output terminals. The output frequency of ac current depends upon the rate of triggering the SCRs. The amplitude of ac output current can be adjusted by controlling the magnitude of dc input current.

The source consists of a, voltage source E and a *large* inductance *L* in series with it. The function of high-impedance reactor in series with source is to maintain a constant current at the input terminals of CSI. When *T1, T2* are on, *load* current i_0 is positive and equal to I. When T3, T4 are on, load current i_0 is negative and equal to *-I*. The output frequency of i_0 can be varied by controlling the frequency of triggering the thyristor pairs T1, T2 and T3, T4.

The dc current I, input to CSI, is always unidirectional. If average value of v_{in} is positive, power flows from source to load. In case average value of v_{in} is negative, power flows from load to source. *i.e.* regeneration of power takes place.

Q9.   **a. Are solid state relays? How these are different from electromagnetic relays? Explain solid state relays by giving suitable circuit diagrams.**

Answer:

AC and dc static switches can be used as solid state relays (SSRs). Solid state relays have no contacts or moving parts like electromagnetic relays. Solid state relays has fast operation with very little lag as compared to electromagnetic relays. Power losses are also very less in SSRs. These are now being used extensively and are replacing the conventional contact-type electromagnetic relays. SSRs need electrical isolation between control circuit and the load circuit by means of optocouplers or pulse transformers.
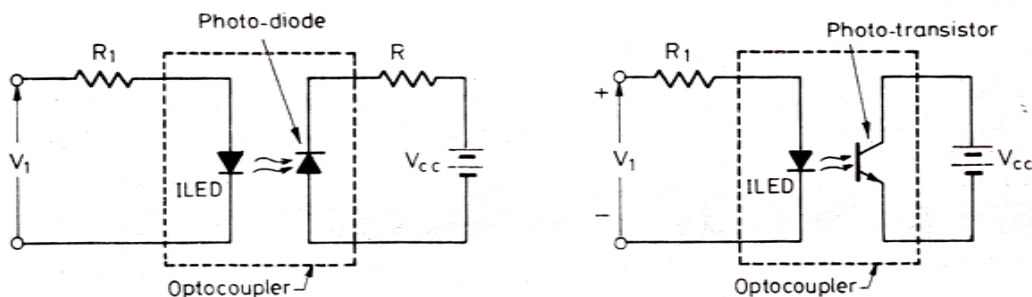
An optocoupler consists of infra-red light emitting diode (ILED) and a photo diode or a photo-transistor. Pulse V_1 applied to ILED will cause it to emit light on to photo-diode which will then to conduct in the reverse direction as shown. Also a short pulse V_1 applied to ILED will throw light on the base of photo-transistor and turn it on.

DC Solid State Relays:

A dc solid state relay using opto-coupler for isolation purposes is shown in Fig. below. When control pulse V_c is applied to ILED, it emits light and turns on the photo-transistor. The current output from the photo-transistor acts as the base current for transistor TR. Consequently TR is turned on and source voltage V_s is applied to load. When control pulse V_c is absent, TR gets turned off and load voltage is zero.
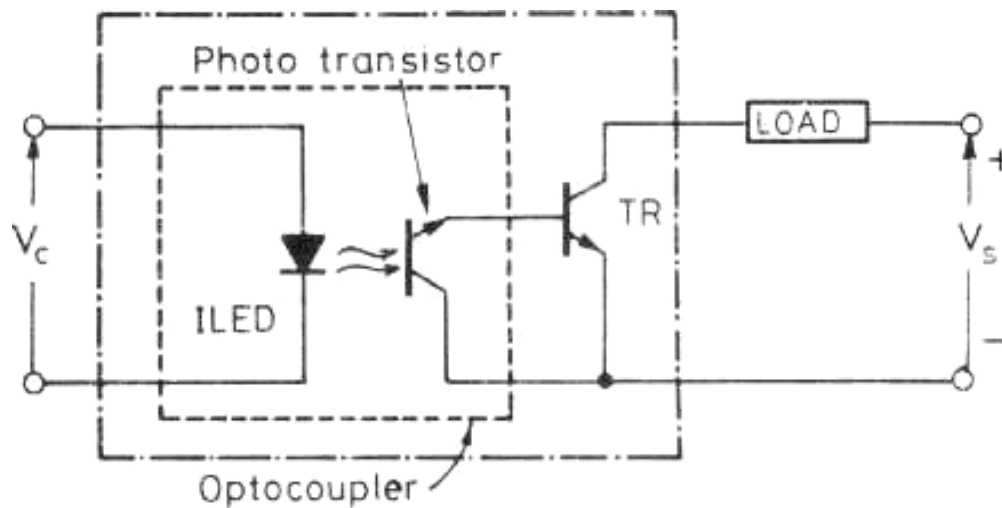
AC Solid State Relays:

Fig. below shows two basic circuits for ac solid-state relays. First fig. uses a pulse transformer for isolation purposes and in second Fig.isolation is provided by an optocoupler. When control signal appears across the primary of pulse transformer, its secondary applies a triggering pulse to turn on the triac, As a result, load circuit is completed through triac, and source voltage is applied to the load.
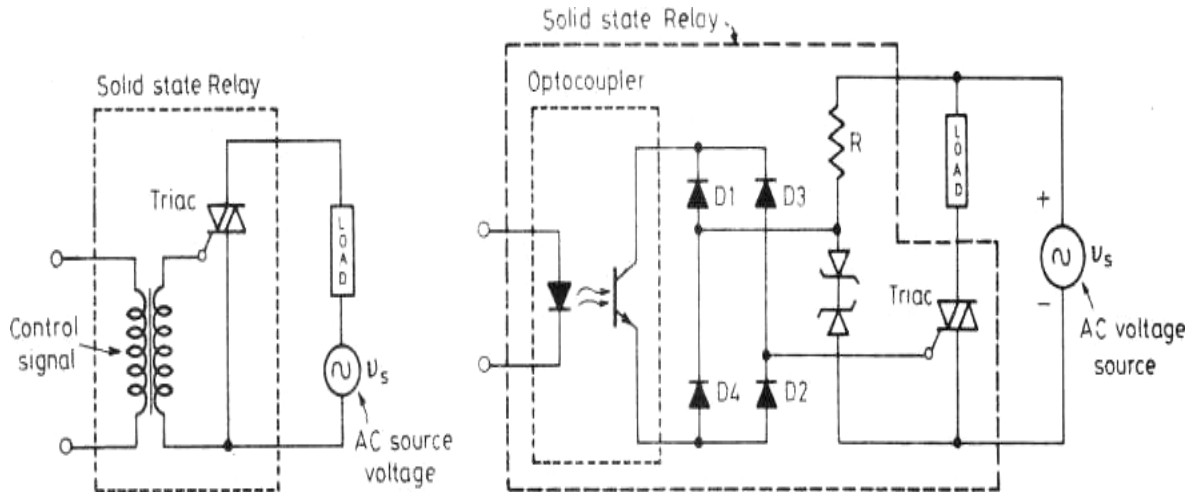
In second Fig., control signal turns on the photo-transistor. If the ac supply has upper terminal positive, the current will flow through R, Dl, photo-transistor, D2, triac gate and source. This current will turn on the triac and load gets energized by source voltage v_s. The function of R is to limit the flow of gate current of triac. If lower terminal of ac supply is positive, the current will flow through triac gate, D3, phototransistor, D4, R and source v_s. Triac gets turned on and source voltage is applied to load.

b. Explain the working of a bridge type single phase to single phase step-up cycloconverter with wave forms.

Answer:

Bridge type single phase to single phase step-up cycloconverter:

(b)

21
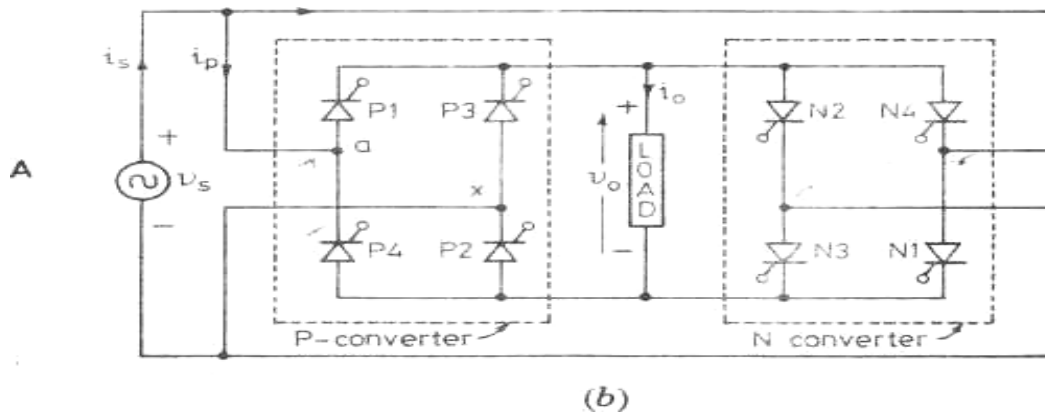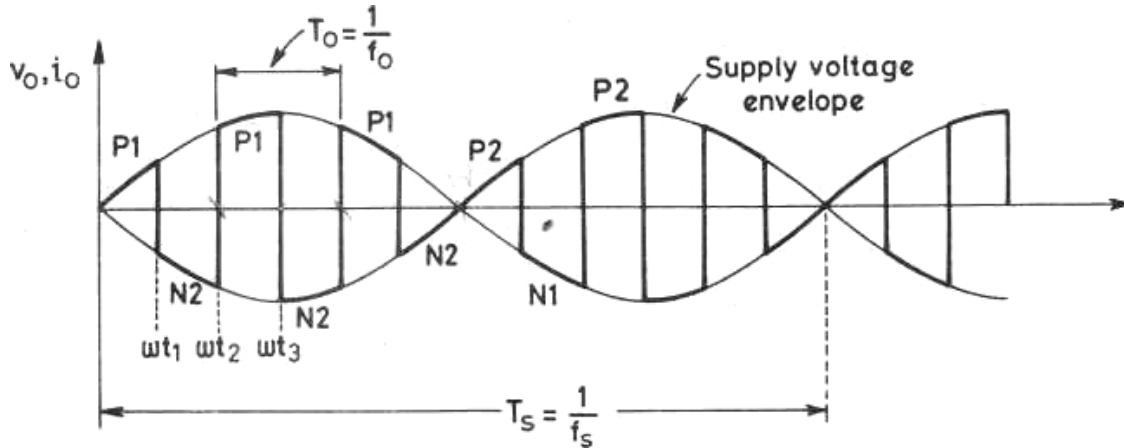
It consists of a total of eight thyristors, P1 to P4, four for positive group and N1 to N4, four for the negative group. When point '*a', as shown in ckt diagram,* is positive with respect to point '*x', as shown* in circuit diagram *i.e.* during the positive half cycle of the output wave, thyristor pairs PI, P2 and Nl, N2 are forward biased from $\omega t = 0°$ to $\omega t = \pi$. When forward biased thyristors PI, P2 are turned on together at $\omega t = 0°$, the load voltage is positive with respect to *x.* Forward-biased thyristors PI, P2 are turned on together at $\omega t = 0°$ so that load voltage is positive. Load voltage now traverses the positive envelope of supply voltage, as shown in output wave.

At ωt_1, pair PI, P2 is force commutated and forward biased pair N1, N2 is turned on. With this, load voltage is goes negative. Load voltage now follows the negative envelope of source voltage. At ωt_2, Nl, N2 are force commutated and PI, P2 are turned on. The load voltage is now positive and follows the positive envelope of source voltage. After $\omega t = \pi$, thyristor pairs P3, P4 and N3, N4 are forward biased, these can therefore be turned on and force commutated from $\omega t = \pi$ to $\omega t = 2\pi$. In this manner, a high-frequency turning-on and force commutation of pairs PI P2, Nl N2 and pairs P3 P4, N3 N4 gives a carrier-frequency modulated output voltage across load terminals, as shown in output wave form.

Text Book

Power Electronics for Technology, First Impression (2006), Ashfaq Ahmed, Purdue University – Calumet, Pearson Education