Q.2 a. Explain the pin diagram of 8085.

Answer: 4.2 of Text Book

b. Explain all the rotate instruction of 8085

Answer: 8.7 of Text Book

Q.3 a. Describe & draw the neat diagram to interface 2K×8 memory chip with 8085 microprocessor

Answer: 11.2 of Text Book

b. Explain peripheral or externally initiated operations in 8085

Answer:

External devices can initiate following operations, for which individual pins on the microprocessor chip is assigned, these operations are:

1. **Reset**

   When reset pin is activated all internal l operations are stopped and the program counter is reset to 0000. Program execution again begins from zero memory address.

2. **Interrupt**

   The microprocessor's operations are interrupted and the microprocessor executes what is called a "**service routine**". This routine "handles" the interrupt, (perform the necessary operations). Then the microprocessor returns to its previous operations and continues

3. **Ready**

   The 8085 has a pin called RDY. This pin is used by external devices to stop the 8085 until they catch up. As long as the RDY pin is low, the 8085 will be in a wait state. This signal is used primarily to synchronize slower peripherals with the microprocessor.

4. **Hold**

   The 8085 has a pin called HOLD. This pin is used by external devices to gain control of the busses. When the HOLD signal is activated by an external device, the 8085 stops executing instructions and stops using the busses. This would allow external devices to control the information on the busses. Example **DMA**.

Q.4 a. Write an assembly language program for addition of two 8 bit numbers and its sum is 16 bits.

Answer:

```
        LXI     H, 2501
        MVI     C, 00
        MOV     A,M
        INX     H
        ADD     M
        JNC     AHEAD
        INR     C
AHEAD:  STA     2503
        MOV     A, C
        STA     2504
        HLT
```

b. Write an assembly language program to find the largest number in a data array.

Answer:

```
        LXI     H, 2500
        MOV     C,M
        INX     H
        MOV     A,M
        DCR     C
LOOP:   INX     H
        CMP     M
        JNC     L1
        MOV     A,M
L1:     DCR     C
        JNZ     LOOP
        STA     2400
        HLT
```

Q.5 a. Describe the action taken by 8085 when INTR is activated.

Answer: 18.4.1 of Text Book

b. Explain EI & DI instruction with example.

Answer: 18.3 of Text Book

Q.6 a. What are the different modes in which 8255 programmable peripheral interface can operate?

Answer: 20.2 of Text Book

b. Write an 8085 ALP to implement a decimal counter using logic controller interface.

Answer: 21.1.3 of Text Book

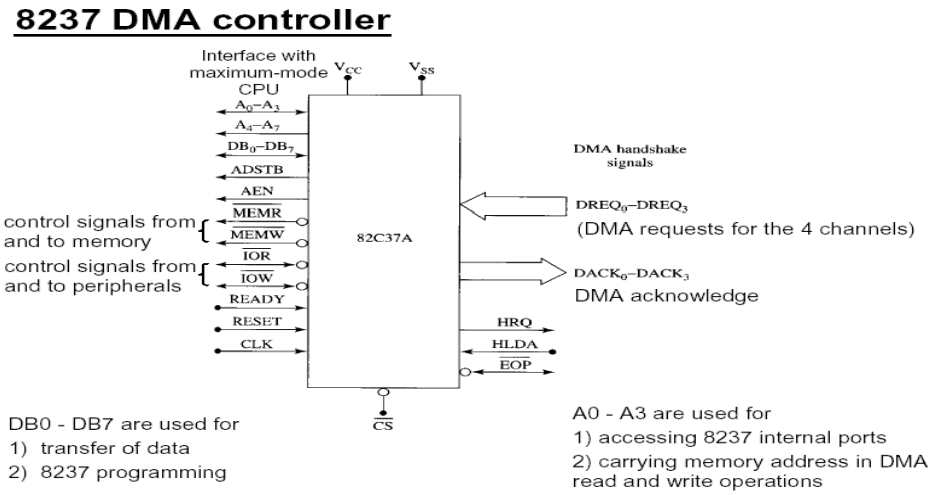
Q7 a. What is meant by DMA? Explain the various DMA modes. Describe in brief the steps that take place during a DMA write cycle.

Answer:

Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.DMA is for **high-speed data transfer** from/to mass storage peripherals, e.g. harddisk drive, magnetic tape, CD-ROM, and sometimes video controllers. For example, a hard disk may boasts a transfer rate of 5 M bytes per second, i.e.1 byte transmission every 200 ns. To make such data transfer via the CPU is
both undesirable and unnecessary.

The basic idea of **DMA** is to transfer *blocks of data* directly between memory and peripherals. The data don't go through the microprocessor but the data bus is occupied. "Normal" transfer of one data byte takes up to 29 clock cycles. The DMA transfer requires only 5 clock cycles.

Nowadays, DMA can transfer data as fast as 60 M byte per second. The transfer rate is limited by the speed of memory and peripheral devices.



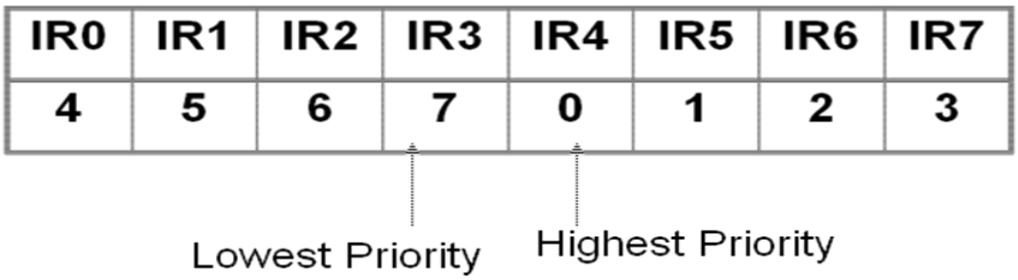
The modes of operation include demand mode, single mode, block mode, and cascade mode. Demand mode transfers data until an external EOP is input or until the DREQ input becomes inactive. Single mode releases the HOLD after each byte of data transferred. Block mode automatically transfers the number of bytes indicated by the count register for the channel. Cascade mode is used when more than one 8237 is present in a system.

b. Explain the different priority modes used in PIC 8259.

Answer:

Commonly used priority modes

1. Fully Nested Mode
   - » This is general-purpose mode in which all IRs are arranged from highest to lowest, with IR0 as the highest and IR7 as the lowest
   - » In addition, any IR can be assigned highest priority in this mode; the priority sequence will then begin at that IR



2. Automatic Rotation Mode
   - » In this mode, a device, after being serviced, receives the lowest priority.
   - » Assuming that the IR2 has just been serviced, it will receive the seventh priority, as shown below:
   - »

IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7
5	6	7	0	1	2	3	4

3. Specific Rotation Mode
   - » This mode is similar to the automatic rotation mode, except that the user can select any IR for the lowest priority, thus fixing all other priorities

Q8. a. Explain the mode-0 operation of the 8253 Timer with example

Answer: 25.4 of Text Book

b. Explain various pins used in 8251.

Answer: 26.6 of Text Book

Q9.a. How stacks are accessed in 8051?

Answer:

If the stack is section of RAM, there must be registers inside the CPU to point to it. The register used to access the stack is called the SP (stack pointer) register. The stack pointer in the 8051 is only 8 bits wide, which means that it can take values of 00 to FFH. When the 8051 is powered up, the SP register contains value 07. This means that RAM location 08 is the first location used for the stack by the 8051. The storing of a CPU register in the stack is called a PUSH, and pulling the contents off the stack back into a CPU register is called a POP. The job of the SP register is very critical when PUSH and POP actions are performed.

b. Write PUSH instruction to push the contents of the registers on stack after the execution of the following set of instructions?

(i) MOV SP, #4FH
(ii) SETB PSW.3
(iii) MOV R0, #25H
(iv) MOV R1, #0CH
(v) MOV R2, #05H
(vi) MOV A, #0CEH

Answer:

The first instruction defines the stack to be from 50H onwards. The second instruction defines the use of register bank 1. Since the register bank 1 has been selected, the addresses of registers R0, R1, and R2 are 8, 9, and 0AH. The address of the A register is 0E0H. Hence the PUSH instructions are

```
PUSH 8
PUSH 9
PUSH 0AH
PUSH 0E0H
```

After the four PUSH instructions, the content of the RAM selected as the stack locations will be

ADDRESS	DATA
50	25H
51	0CH
52	05H
53	CEH

Text Book

The 8085 M-P, Microprocessor Architecture, programming & Interfacing, K.Udaya kumara & B.S.Umashankar, Pearson education, 2008