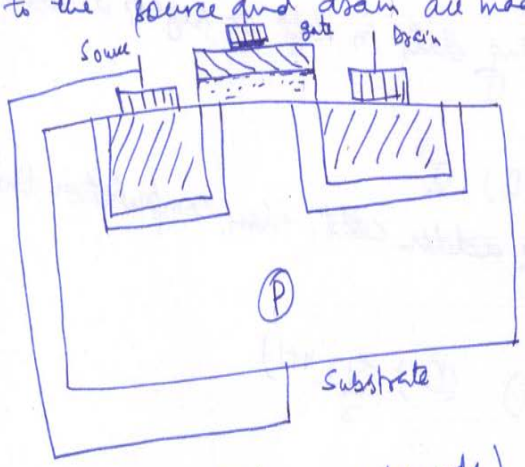
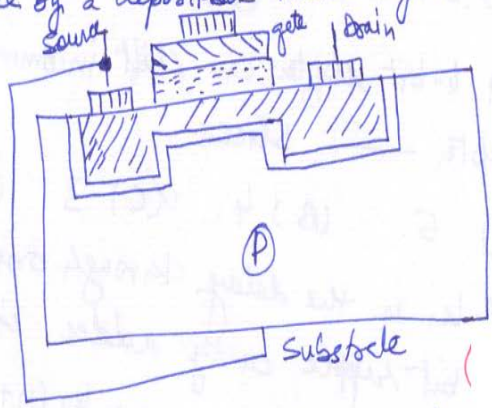
Q2 (a) Explain basic n MOS transistors.

Answer

Basic NMOS transistors:- are formed in p-type substrate of moderate doping. The source and drain regions are formed by diffusion of n type impurities through suitable masks into these areas to give the desired n - impurity concentration and give rise to depletion region which extend mainly in the more lightly doped p region. Thus source and drain are isolated from one another by two diodes. Connections to the source and drain are made by a deposited metal layer.



(NMOS enhancement mode transistor)



(NMOS depletion mode transistor)

The channel may also be established so that it is present under the condition $V_{gs} = 0$ by implementing suitable impurities in the region between source and drain during manufacture and prior to deposit the insulating and gate.

next

Q2 (b) Explain the thermal aspects of processing nMOS and CMOS devices.

Answer: Page Number 17 & 18 from text book

Q3 (a) Derive the relationship between transconductance and output conductance for MOS transistors.

Answer:

Transconductance expresses the relationship between o/p current I_{ds} and i/p voltage V_{gs} and is defined as

$$g_m = \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds}=\text{Constant}}$$

Transit time $\tau = \frac{Q_c}{I_{ds}}$

This change in current

$$\delta I_{ds} = \frac{\delta Q_c}{\tau_{ds}}$$

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

$$\delta I_{ds} = \frac{\delta Q_c V_{ds} \mu}{L^2}$$

$$\delta Q_c = C_g \delta V_{gs}$$

So that $\delta I_{ds} = \frac{C_g \delta V_{gs} \mu V_{ds}}{L^2}$

Now $g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$

In saturation $V_{ds} = V_{gs} - V_t$

$$g_m = \frac{C_g \mu}{L^2}(V_{gs} - V_t)$$

Substitute for $C_g = \frac{\epsilon_{ins} \epsilon_0 WL}{D}$

$$g_m = \frac{\mu \epsilon_{ins} \epsilon_0 W}{D \quad L}(V_{gs} - V_t)$$

or $\boxed{g_m = \beta(V_{gs} - V_t)}$ where $\beta = \frac{\mu \epsilon_{ins} \epsilon_0 W}{D \cdot L}$

Q3 (b) Explain CMOS inverter.

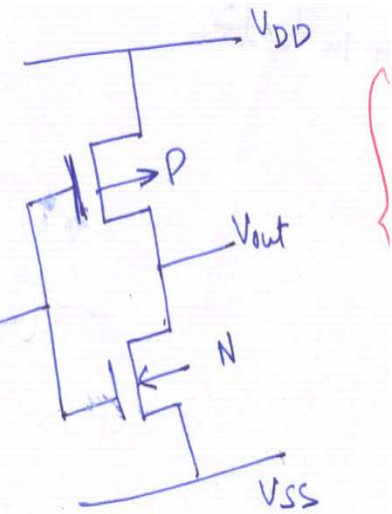
Answer

6. CMOS Inverter :-

The current / voltage relationship for MOS Transistor

$$I_{ds} = k\frac{W}{L}\left(V_{gs} - V_t\right)V_{ds} - \frac{V_{ds}^2}{2}$$

In the resistive region.



$$I_{ds} = k\frac{W}{L}\left(V_{gs} - V_t\right)^2$$ In saturation

In both cases factor k is technology dependent parameter such that

$$k = \frac{\epsilon_{ins}\epsilon_0\mu}{D}$$

The factor W/L is contributed by geometry and it is common

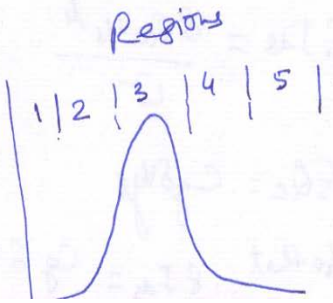
$$\beta = k\frac{W}{L}$$

so that $I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$

$$\beta_n = \frac{\epsilon_{ins}\epsilon_0\mu_n}{D}\frac{W_n}{L_n}$$

$$\beta_p = \frac{\epsilon_{ins}\epsilon\mu_p}{D}\frac{W_p}{L_p}$$

Where W_n & L_n and W_p & L_p are n and p transistor dimensions respectively.



Q3 (c) Explain Bi CMOS Latch up susceptibility.

Answer

BiCMOS Latch-up Susceptibility :-

The benefit of the BiCMOS process is that it produces circuits which are less likely to suffer from Latch up problem. This is due to several factors

- A reduction of substrate resistance
- A reduction of n well resistance
- A reduction of Rs & Rw means that a larger lateral current is necessary to invite latch up and a higher value of holding current is also required.
- The parasitic pnp transistor circuit has its beta reduced owing to the presence of the buried n+ layer. This has the effect of reducing carrier lifetime in the n base region and this contributes the reduction in beta.

Q4 (a) Explain contact cuts in NMOS circuits.

Answer

a- Contact cuts in NMOS:- When contacts between polysilicon and diffusion in NMOS are made, there are three possible approaches (4)

1. Poly. to metal then metal to diff
2. a Buried contact poly. to diff.
3. a butting contact (poly to diff.)

When making connections between metal and either of other two layers the process is quite simple. The 2λ × 2λ contact cut indicates an area in which the oxide is to be removed down to the ~~metal~~ underlying polysilicon or diffusion surface. When deposition of the metal layer takes place the metal is deposited through the contact cut areas onto the underlying area so that contact is made between the layers.

Fig: 3.8 and 3.9 : See page 69 : Basic VLSI design Douglas A. Pucknell

Q4 (b) Write down the double metal MOS process rules.

Answer

b. Double metal MOS Process Rules:—

1. Use the second level metal for global distribution of power buses ie V_{DD} and GND (V_{SS}) and for clock lines.
2. Use the first level metal for local distribution of power and for signal lines.
3. Lay out the two metal layers so that the conductors are mutually orthogonal wherever possible.

Q4 (c) Explain design rules for wires in 2 μm CMOS.

Answer Page numbers 77 from text book

Q5 (a) Calculate the rise time and fall time of a CMOS inverter.

Answer

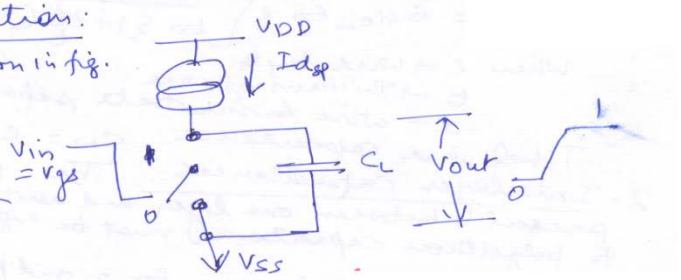
Rise Time Estimation:

The rise time model is shown in fig.

C_L is load capacitor

The saturation current for p-transistor is

$$I_{dsp} = \frac{\beta_p (V_{gs} - |V_{tp}|)^2}{2}$$



$$V_{out} = \frac{I_{dsp}\, t}{C_L}$$

$$t = \frac{2 C_L V_{out}}{\beta_p (V_{gs} - |V_{tp}|)^2}$$

for $t = t_r$ when $V_{out} = +V_{DD}$ so that

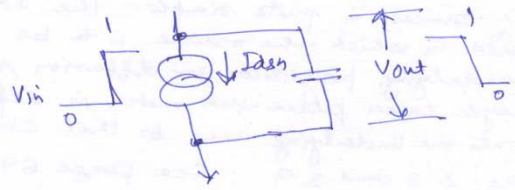
$$\tau_r = \frac{2 V_{DD} C_L}{\beta_p (V_{DD} - |V_{tp}|)^2}$$

If $|V_{tp}| = 0.2 V_{DD}$, then

$$\tau_r = \frac{3 C_L}{\beta_p V_{DD}}$$

Fall time Estimation:—

Discharge C_L through n-transistor. The circuit model is shown in fig.



$$\tau_f = \frac{3L}{\beta_n V_{DD}}$$

Q5 (b) Explain the sources of capacitance which contribute to the overall wiring capacitance.

Answer:

b. There are three sources which contribute to wiring capacitance

1. Fringing Fields
2. Interlayer capacitances
3. Peripheral capacitances.

1. Fringing Fields :- The capacitance due to fringing field effects is major components of the overall capacitance of interconnect wires.

$$C_{ff} = \epsilon_{SiO_2}\,\epsilon_0\, l \left\{ \frac{\pi}{\ln\left\{1+\frac{2d}{t}\left(1+\sqrt{\left(1+\frac{t}{d}\right)}\right)\right\}} - \frac{6}{4d} \right\}$$

Where l → wire length
t → Thickness of wire
d – wire to substrate separate

Total wire capacitance $C_w = C_{area} + C_{ff}$

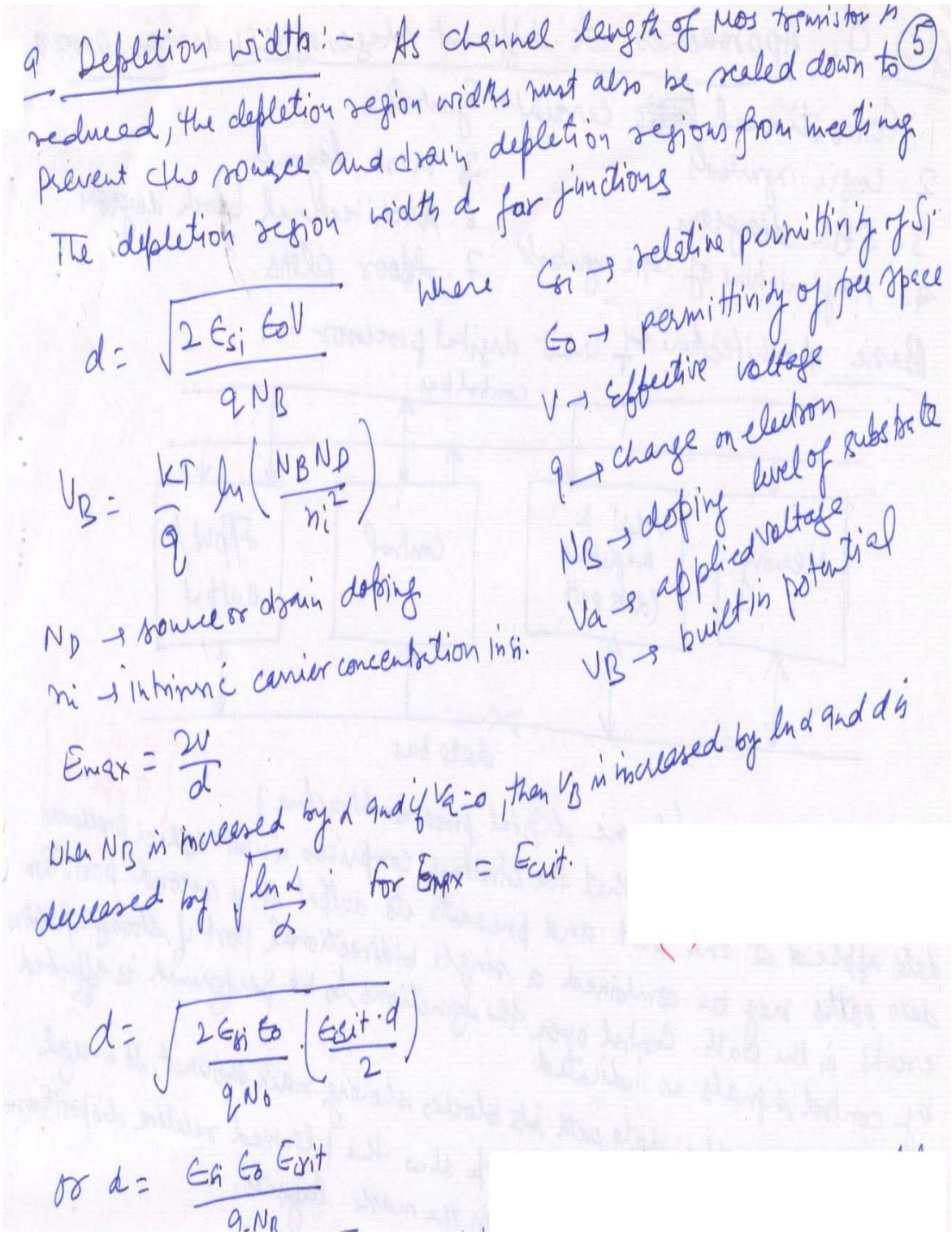
2. Interlayer capacitances : The parallel plate effects are present between one layer and another. For a given area, the metal to polysilicon capacitance must be higher than metal to substrate.

3. Peripheral Capacitance:- For n and p regions formed by a diffusion regions are formed by impurity implant at the surface of silicon. These becomes important as we shrink the device dimensions.

$$C_{total} = C_{area} + C_{periph}$$

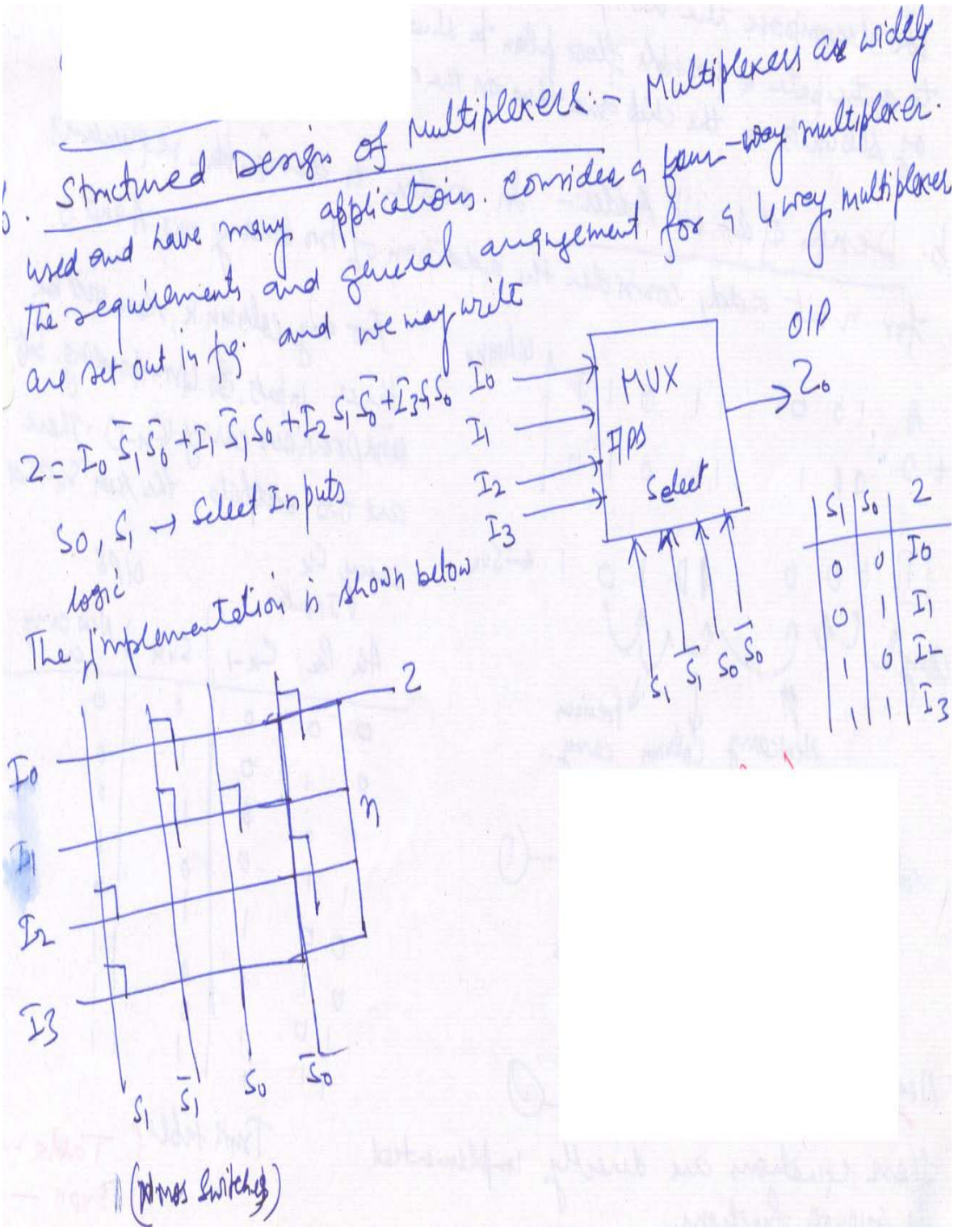
Q6 (a) Derive an expression for depletion width.

Answer:



Q6 (b) Explain the structured design of multiplexer.

Answer:



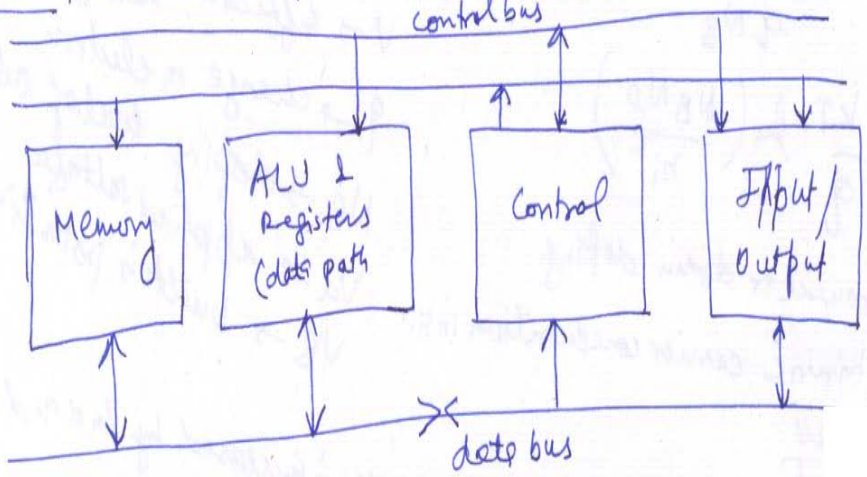
Q7 (a) Where the various approaches used at different stages of VLSI design process? Explain the basic architecture of 4 bit digital processor.

Answer:

6 Approaches at different stages of VLSI design process

1. Conventional circuit symbols
2. Logic symbols
3. Stick diagram
4. Any mixture of logic symbols
5. Mask layouts
6. Architectural block diagram
7. floor plans.

Basic Architecture of 4-bit digital processor



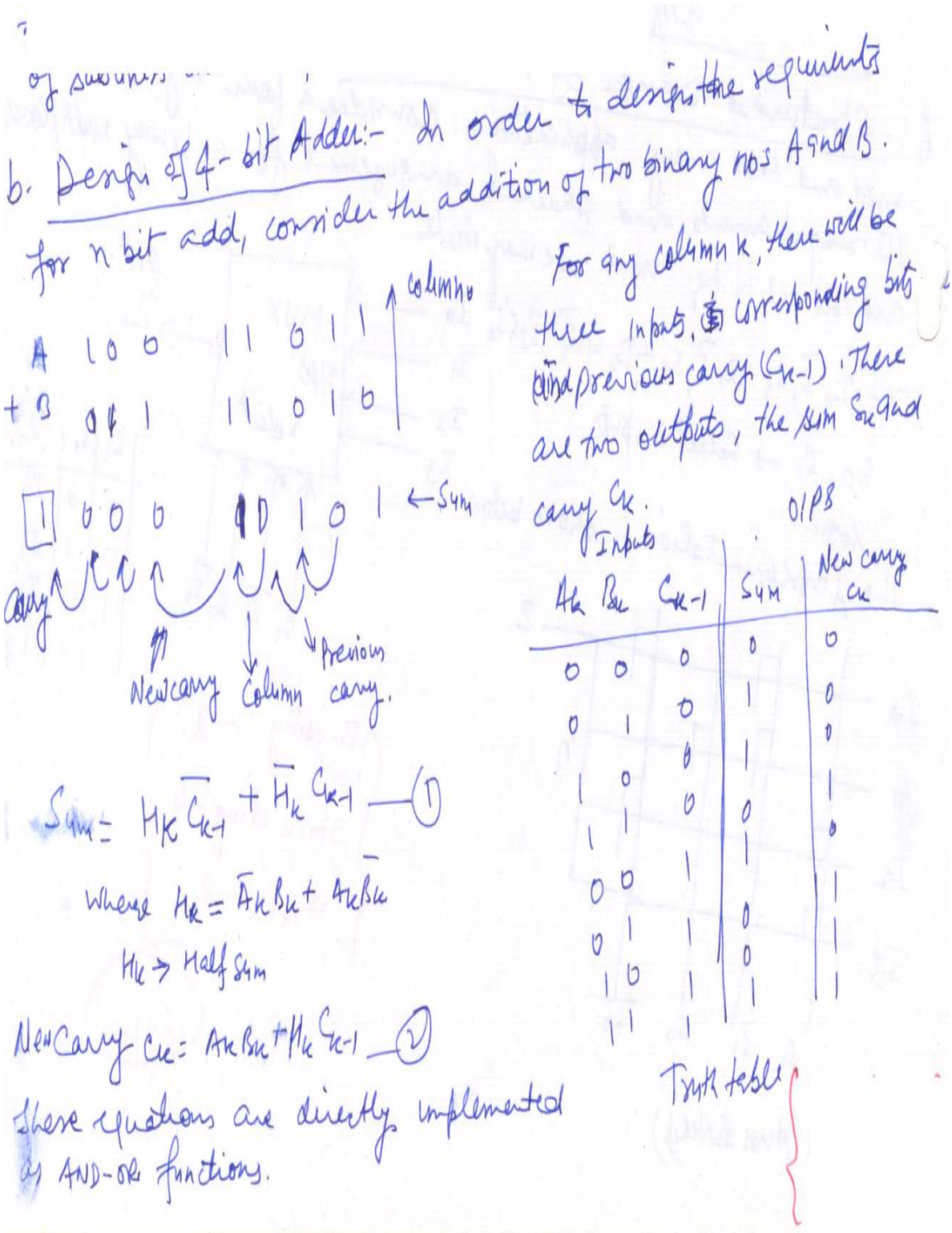
(Basic digital processor structure)

The data path is shown that the structure comprises a unit which processes data applied at one port and presents its output at a second port. Two data paths may be combined a single bidirectional port if storage facilities exists in the path. Control over the functions to be performed is effected by control signals as indicated.

We decompose the data path into blocks showing main subunit. It is useful to anticipate a possible floor plan to show the planned relative dispositions of subunits on the chip and thus on the mask layouts.

Q7 (b) Design a 4 bit adder.

Answer:



Q8 (a) What are the factors considered to make a comparative assessment of the dynamic shift registers?

Answer:

Factors considered to make comparative assesment for the dynamic shift register. (6)

1. Area requirement
2. Estimated dissipation
3. Volatility

1. Area: Consider the case of NMOS design with buried contacts. Allow for sharing of V_{DD} and GND rails between adjacent rows of register cells. The each bit stored will require $22\lambda \times 28\lambda = 1200\lambda^2$

for $\lambda = 2.5\,\mu m$, Area per bit $= 7500\,\mu m^2$

For CMOS $(38\lambda \times 28\lambda) \times 2 = 2100\lambda^2$.

$\lambda = 2.5\,\mu m$ Area per bit $= 13000\,\mu m^2$

2. Dissipation:- In case of CMOS static dissipation is very small, the dynamic power consumption $P_d = m\, C_L V_{DD}^2 f$

Where $m \rightarrow$ duty cycle

$C_L \rightarrow$ effective load capacitance

$f \rightarrow$ Clock frequency.

In NMOS, $Z_{pu} = 4R_s$

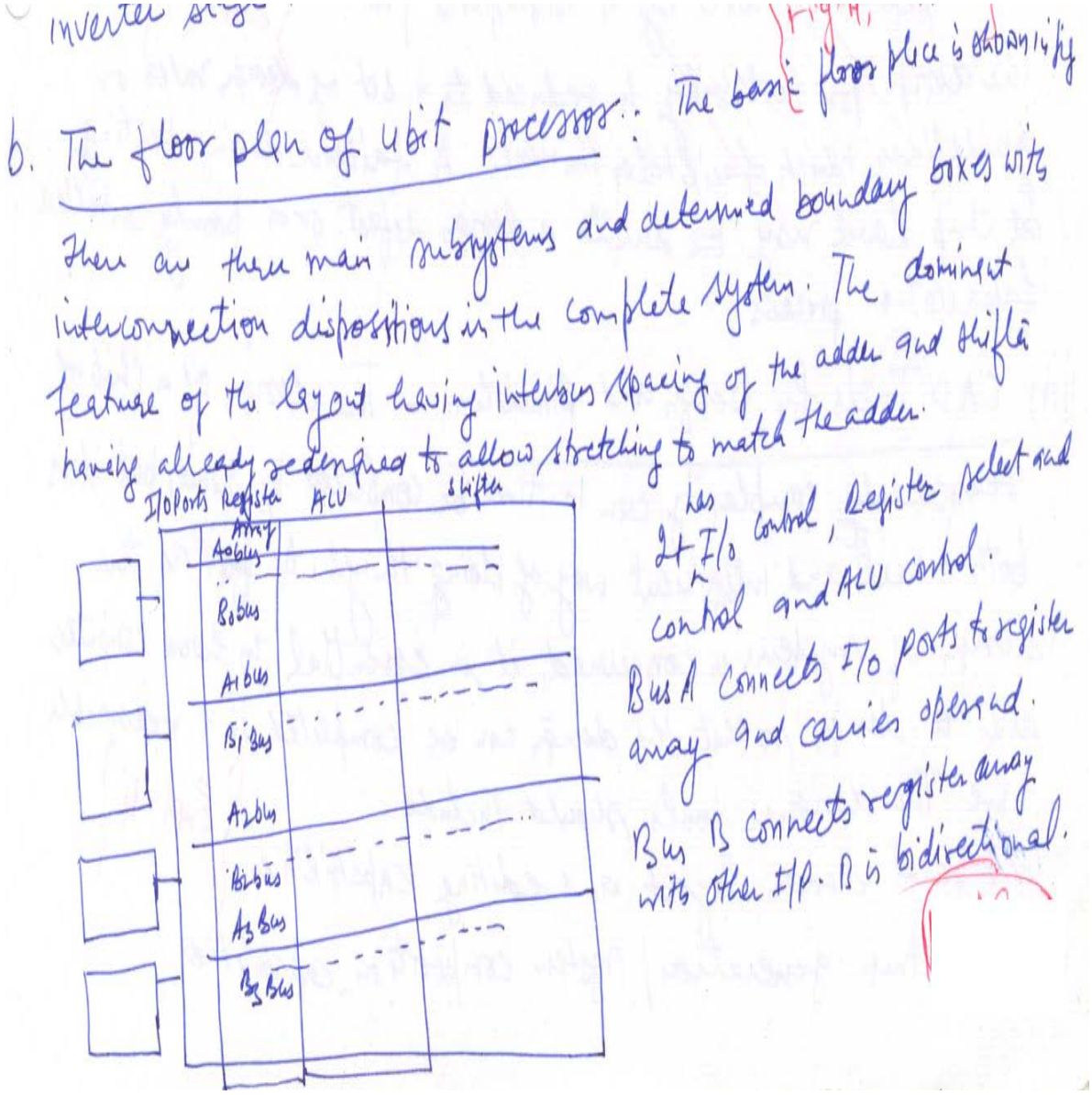
and $Z_{pd} = \frac{1}{2} R_s$

Current $= \frac{V_{DD}}{Z_{pu} + Z_{pd}} \Rightarrow$ The static dissipation / Bit stored $= V_{DD} \times$ Current

3. Volatility:- Data is stored by the charge on the gate capacitor of each inverter stage so that data storage time is limited to 1 msec or less.

Q8 (b) Explain floor plan layout of a 4- bit processor.

Answer:



Q9 Write short note on:

(i) Design Rule Checkers

(ii) CIF code

(iii) CAD Tools for design and simulation

(iv) Signature Analysis in BIST

Answer:

(i) Design Rule checkers:- The cost in time and facility in mask-making and fabricating a chip from those masks is such that all possible errors must be eliminated before checking proceeds. Once a design has been turned into silicon there is little that can be done is check for errors at all stages of design, namely:

1. At the pencil and paper stage of design of leaf-cells.
2. At the leaf-cell level once the layout is complete
3. At subsystem level to check that butting together and wiring up the leaf-cells is correctly done.
4. Once the entire system layout has been completed.

The nature of physical layout verification design rule checking software depend on whether the design rules are absolute or λ based or on whether or not the layout is on a fixed or virtual grid.

(ii) Answer: Page numbers 293 from text book

(iii) Answer:

(iii) CAD Tools for Design and Simulation:- The design of a chip of reasonable complexity can in time be completed by hand, but it is both a hard and inefficient way of doing things. As far as the design of systems is concerned, it is essential to have computer aids to design so that the design can be completed in a reasonable time. The designer tools should include

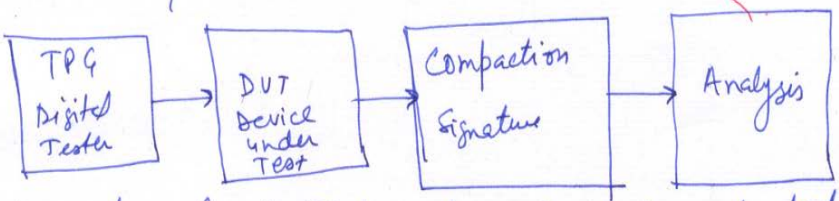
1. Physical design layout and editing capabilities.
2. Structure generation / system composition capabilities.
3. Physical verification: It includes design rule checking, circuit extractors, ratio rule and other static checks and a capability to plot out and/or display for visual checking.
4. Behavioural verification: Simulation at various levels will be required to check out the design before one embarks on the expense of turning out the design in silicon.

(iv) Answer:

(iv) Signature Analysis in BIST

BIST stands for Built in self Test. The BIST techniques aim to effectively integrate automatic test system into the chip design. The test compacting scheme currently used most is called signature analysis. It performs polynomial division that is to say division of the data out of the device under test. This data is represented as a polynomial P(x) which is divided by a characteristics polynomial C(x) to give signature R(x) so that

$$R(x) = P(x)/C(x)$$



The signature for DUT is compared with the expected signature to determine if the DUT is fault free. The difference between the faulty signature and a good signature may also be used to indicate the nature of the fault. Signature analysis has been proved to be a reliable and attractive alternative to full uncompacted testing.

Text Book

Basic VLSI Design, Douglas A. Pucknell & Kamran Eshraghian, PHI, 3rd Edition, 2007