Q.2 a. Classify the integration technology as per the scale of integration. Explain in brief the various steps involved in fabrication of monolithic IC.

Answer:
Scales of Integration (Basic)

Sr. No.	Integration Scale	No. Of Components per chip (approx)
1	SSI (Small Scale Integration)	Up to 99
2	MSI(Medium Scale Integration)	100 - 999
3	LSI (Large Scale Integration)	1000 - 9999
4	VLSI (Very Large Scale Integration)	Above 10,000
	Ultra-Large Scale Integration	More than 1 million

Various steps involved in fabrication of monolithic IC

- **Silicon Substrate Preparation**: It involve the processing steps for growth of pure Si crystal.
- **Deposition:** Films of the various materials are applied on the wafer. For this purpose mostly two kind of processes are used, physical vapor deposition (PVD) and chemical vapor deposition (CVD).
- **Oxidation:** In the oxidation process oxygen (dry oxidation) or H_2O (wet oxidation) molecules convert silicon layers on top of the wafer to silicon dioxide.
- **Photo-Lithography:** The process for pattern definition by applying thin uniform layer of viscous liquid (photo-resist) on the wafer surface. The photo-resist is hardened by baking and than selectively removed by projection of light through a reticle containing mask information.
- **Diffusion:** A diffusion step following ion implantation is used to anneal bombardment-induced lattice defects.
- **Ion Implantation:** Most widely used technique to introduce dopant impurities into semiconductor. The ionized particles are accelerated through an electrical field and targeted at the semiconductor wafer.
- **Etching:** Selectively removing unwanted material from the surface of the wafer. The pattern of the photo-resist is transferred to the wafer by means of etching agents.
- **Chemical Mechanical Polishing:** A planarization technique by applying a chemical slurry with etchant agents to the wafer surface.
- **Metallization Process:** Metallization is the final step in the wafer processing sequence. Metallization is the process by which the components of IC's are interconnected by aluminium conductor. This process produces a thin-film metal layer that will serve as the required conductor pattern for the interconnection of the various components on the chip.

b. Calculate (i) input bias current and (ii) input offset current for the circuit shown in Fig.1. Given that $\beta_1 = 100$ and $\beta_2 = 125$.

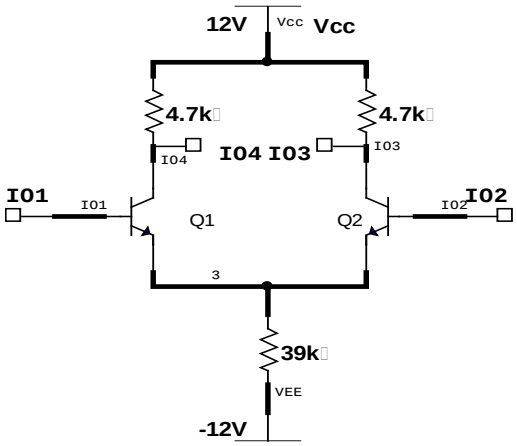


Fig.1

Answer:

Assuming zero input voltage, applying

KVL to i/p loop, (Assume $V_{BE1} = 0.7$ V)

$-V_{BE1} - 39 \times 10^3 I_E + 12 = 0$

$I_E = 289.743$ Ma

$I_{E1} = I_{E2} = I_{E/2} = 289.743\ \mu A / 2 = 144.871\ \mu A$

Hence, $I_{b1} = I_{E1}/\beta 1 = 144.871\ \mu A / 100 = 1.44871\ \mu A$

$I_{b2} = I_{E2}/\beta 2 = 144.871\ \mu A / 125 = 1.15897\ \mu A$

Hence Input bias current = $I_b = (I_{b1} + I_{b2}) / 2 = 1.3038\ \mu A$

Input offset current = $I_{ios} = |I_{b1} - I_{b2}| = 0.28974\ \mu A$

Q.3 a. What are the requirements of Instrumentation Amplifier? Draw 3-op-amp configuration of Instrumentation amplifier and derive the expression for its gain.

Answer:

Requirements of good Instrumentation Amplifier

1. Finite, accurate and stable gain
2. Easier gain adjustment
3. High input impedance
4. Low output impedance
5. High CMRR
6. Low power consumption
7. Low thermal and time drift
8. High slew rate
9. Differential input.

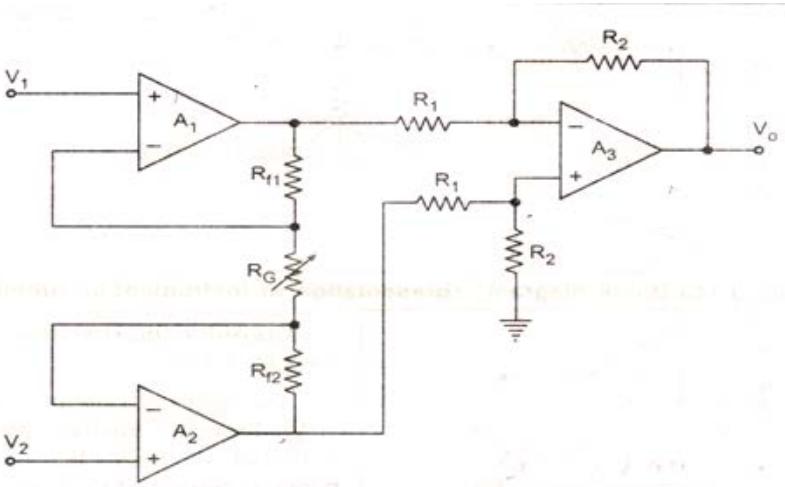


Fig. 3.142 Three op-amp instrumentation amplifier

The op-amps A_1 and A_2 are the noninverting amplifiers forming the input or first stage of the instrumentation amplifier. The op-amp A_3 is the normal difference amplifier forming an output stage of the amplifier.

The block diagram representation of the three op-amp instrumention amplifier is shown in the Fig. 3.143. (See Fig. 3.143 on next page)

3.36.2.1 Analysis of Three Op-amp Instrumentation Amplifier

It can be seen that the output state is a standard basic difference amplifier. So if the output of the op-amp A_1 is V_{o1} and the output of the op-amp A_2 is V_{o2}, we can write,

$$V_o = \frac{R_2}{R_1}(V_{o2} - V_{o1}) \quad \ldots (3.335)$$

Let us find out the expression for V_{o2} and V_{o1} interms of V_1, V_2, R_{f1} and R_{f2} and R_G.

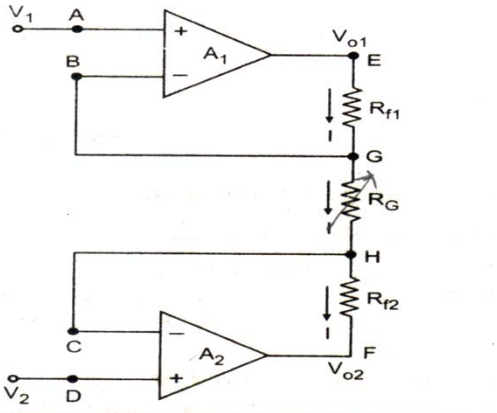


Fig. 3.144

$$I = \frac{V_{o1} - V_{o2}}{R_f + R_g + R_{f2}}$$

Let $R_{f1} = R_{f2} = R_f$

$$\therefore \quad I = \frac{V_{o1} - V_{o2}}{2R_f + R_g}$$

Now from the observation of nodes G and H,

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G}$$

Equating the two equations (3.338) and (3.339),

$$\frac{V_{o1} - V_{o2}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$\therefore \quad \frac{V_{o2} - V_{o1}}{2R_f + R_G} = \frac{V_2 - V_1}{R_G}$$

$$\therefore \quad V_{o2} - V_{o1} = \frac{(2R_f + R_G)(V_2 - V_1)}{R_G}$$

Substituting the $V_{o2} - V_{o1}$, in the equation (3.335),

$$V_o = \frac{R_2}{R_1} \cdot \left[\frac{2R_f + R_G}{R_G}\right](V_2 - V_1)$$

$$\therefore \quad V_o = \frac{R_2}{R_1} \cdot \left(1 + \frac{2R_f}{R_G}\right)(V_2 - V_1)$$

This is the overall gain of the circuit.

b. The input V_i to an op-amp is 0.04 sin 1.13 x 10^5 t is to be amplified to the maximum extent. How much maximum gain required for an op-amp with a slew rate of 0.4 V/ µSec.

Answer:

The given input can be compared with

Vi = Vm sin ωt and Vi = 0.04 sin 1.13 x 10^5 t

Hence, Vm (input) = 0.04 V , ω = 1.13 x 10^5

Now, fm = S / 2π Vm and ω = 2π fm = 1.13 x 10^5 (Where S = Slew Rate)

Hence, fm = 1.13 x 10^5 / 2π

Putting S = 0.04 V / µSec = 0.04/ 10^{-6} V / µSec

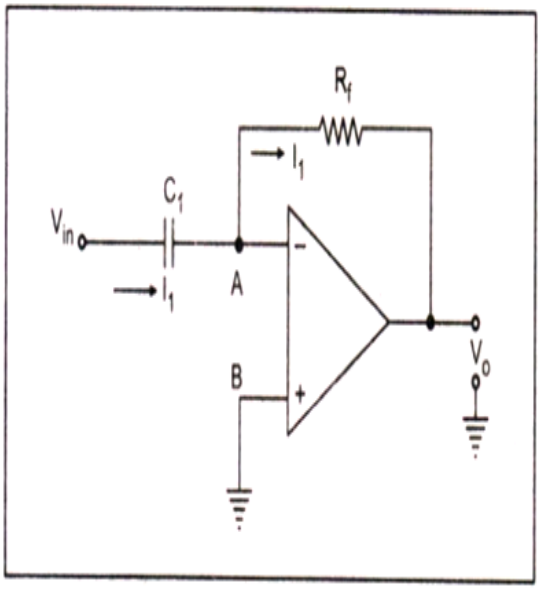
Hence 1.13 x 10^5 / 2π = (0.04/ 10^{-6}) / 2π Vm

Hence Vm = 3.5398 V is the magnitude of output voltage.

Gain = Vm (output) / Vm(input) = 3.5398 / 0.04 = **88.5**

Q.4 a. Draw and explain the ideal differentiator circuit. What are the problems associated with it and how are they eliminated in practical differentiator?

Answer:



The active differentiator circuit can be obtained by exchanging the positions of R and C in the basic active integrator circuit. The op-amp differentiator circuit is shown in the Fig. 3.43.

The node B is grounded. The node A is also at the ground potential hence $V_A = 0$.

3.13.3 Disadvantages of an Ideal Differentiator

The gain of the differentiator increases as frequency increases. Thus at some high frequency, the differentiator may become unstable and break into the oscillations. There is possibility that op-amp may go into the saturation.

Also the input impedance $X_{C1} = (1 / 2\pi f C_1)$ decreases as frequency increases. This makes the circuit very much sensitive to the noise. Thus when such noise gets amplified due to high gain at high frequency, noise may completely override the differentiated output.

Hence the differentiator circuit suffers from the limitations on its stability and noise problems, at high frequencies. These problems can be corrected using some additional parameters in the basic differentiator circuit. Such a differentiator circuit is called **practical differentiator circuit.**

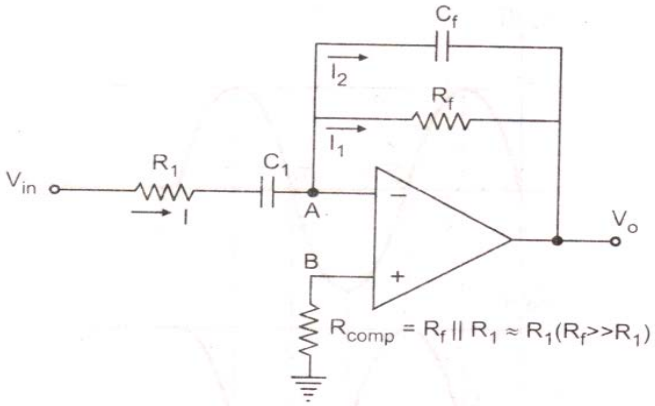


Fig. 3.48 Practical differentiator circuit

b. Explain the operation of the circuit shown in Fig.2. Also draw the waveforms with suitable calculations by assuming $V_{sat} = 0.9V_{CC}$

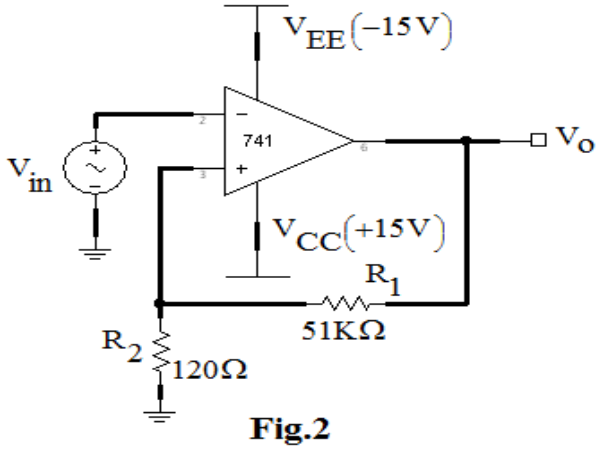


Fig.2

Answer:

3.44.1 Inverting Schmitt Trigger

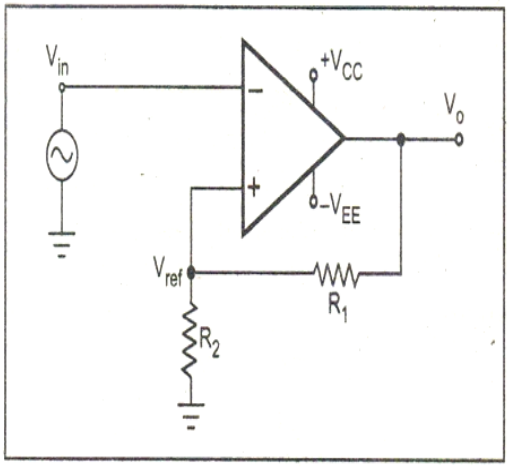


Fig. 3.169 Inverting schmitt trigger

The Fig. 3.169 shows the basic schmitt trigger circuit. As the input is applied to the inverting terminal, it is also called inverting schmitt trigger circuit. The inverting mode produces opposite polarity output. This is fedback to the non-inverting input which is of same polarity as that of output. This ensures positive feedback.

When V_{in} is slightly positive than V_{ref}, the output gets driven into negative saturation at $-V_{sat}$ level.

When V_{in} becomes more negative than $-V_{ref}$, then output gets driven into positive saturation at $+V_{sat}$ level.

Thus output voltage is always at $+V_{sat}$ or $-V_{sat}$ but the voltage at which it changes its state now can be controlled by the resistance R_1 and R_2. Thus V_{ref} can be obtained as per the requirement.

Now R_1 and R_2 forms a potential divider and we can write,

$$+V_{ref} = \frac{V_o}{R_1+R_2} \times R_2 = \frac{+V_{sat}}{R_1+R_2} \times R_2 \quad \text{.... positive saturation}$$

$$-V_{ref} = \frac{V_o}{R_1+R_2} \times R_2 = \frac{-V_{sat}}{R_1+R_2} \times R_2 \quad \text{.... negative saturation}$$

$+V_{ref}$ is for positive saturation when $V_o = +V_{sat}$ and is called **upper threshold voltage** denoted as V_{UT}. $-V_{ref}$ is for negative saturation when $V_o = -V_{sat}$ and is called **lower threshold voltage** denoted as V_{LT}. The values of these threshold voltage levels can be determined and adjusted by selecting proper values of R_1 and R_2.

Thus $$V_{UT} = \frac{+V_{sat}\,R_2}{(R_1+R_2)}$$

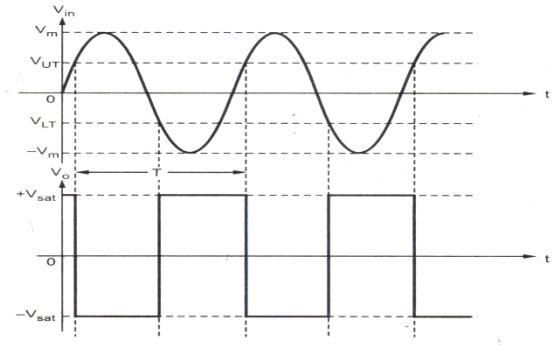
and $$V_{LT} = \frac{-V_{sat}\,R_2}{(R_1+R_2)}$$

The output voltage remains in a given state until the input voltage exceeds the threshold voltage level either positive or negative.

Hysteresis Voltage = $V_{UT} - V_{LT}$

$$\mathbf{V_{HY}} = \frac{+Vsat.R2}{R1+R2} - \frac{-Vsat.R2}{R1+R2}$$

$$\mathbf{V_{HY}} = \frac{2\,Vsat.R2}{R1+R2}$$



In the given problem,

Vcc = +15 V. Hence Vsat = 0.9 Vcc = 0.9 x 15 = 13.5 V

R1= 51 kΩ , R2 = 120 Ω

$\mathbf{V_{UT}} = \frac{+Vsat.R2}{R1+R2} = \frac{+13.5\ X\ 120}{51000\ +120} = \mathbf{0.03169\ V}$ and $\mathbf{V_{LT}} = \frac{-Vsat.R2}{R1+R2} = \frac{-13.5\ X\ 120}{51000\ +120} = \mathbf{-0.03169V}$

Hence, Hysteresis Voltage = V_{HY} = $V_{UT} - V_{LT}$ = 0.03169 V – (- 0.03169V) = 0.06338 V

= 63.38 mV

Q.5 a. State the disadvantages of Binary weighted resistor DAC and advantages of R-2R ladder network DAC. An 8 bit DAC has output voltage range from 0 to 5V, then find its resolution.

Answer:
Disadvantages of Binary weighted resistor DAC-

Drawbacks :

1. Wide range of resistor values are required. For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, 2^3 R, ... and 2^8 R. Therefore, the largest resistor is 128 times the smallest one.
2. This wide range of resistor values has restrictions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across such a large resistor due to the bias current also affects the accuracy. For smaller values of resistors, the loading effect may occur.
3. The finite resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.

All these drawbacks, especially the requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8-bits.

Advantages of R- 2R ladder type DAC

Advantages of R/2R ladder DACs :

1. Easier to build accurately as only two precision metal film resistors are required.
2. Number of bits can be expanded by adding more sections of same R/2R values.
3. In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

- For the given DAC, n= No. Of bits = 8 , V_{oFS} = Full scale output voltage = 5 V

Resolution = V_{oFS} / (2^n – 1) = = 5 V / (2^8 – 1) = 0.0196 V/ LSB = <u>19.6 mV / LSB</u>

b. Explain with suitable circuit diagram and waveforms Astable-multivibrator circuit operation using IC 555.

Answer: Page number 318, 319 & 320 of Text Book - I.

Q.6 a. Compare and contrast serial and parallel data transmission technique

Answer:

Serial Data Transmission

1. Data is transmitted bit by bit in serial fashion
2. Data is transmitted or received in a sequence.
3. Only one conducting wire is required.
4. Thus less hardware (wires) required.
5. Cheaper.
6. It is comparative slower.
7. Data synchronization is required.
8. Useful for long distance data transfer like internet etc.

Parallel Data Transmission

1. Data is transmitted all bits at a time.
2. Data is transmitted or received in a parallel way.
3. Number of conducting wire = no. of bits.
4. Thus more hardware (wires) required.
5. Comparatively costlier.
6. It is comparative faster.
7. Data synchronization is not required as such.
8. Useful for long distance data transfer like internet etc.
9. Useful for short distance data transfer like on chip or on board data transfer etc.

b. A digital system consists of 1024 x 8 bit memory.

(i) How many address lines will it require?

(ii) Specify the range of address in Hex.

(iii) How many total number of bits can be stored in this memory?

Answer:

A digital system consists of 1024 x 8 bit memory.

(i) 2^{10} = 1024 Hence it will require **10 address lines**

(ii) 1024 locations X 8 bits per location = **8192 bits.**

(iii) 0000000000 to 1111111111 i.e. **000 H to 3FF H**

c. Make the following conversion (steps are necessary):

(i) 100011101 to decimal

(ii) $(17735)_8$ to Hex

(iii) $(ABCD)_{16}$ to binary

Answer:

(i) 285 Decimal

(ii) 1FDD Hex

(iii) (1010 1011 1100 1101) binary

Q7 a. State and prove DeMorgan's Theorem.

Answer:

$$\overline{A \cdot B} = \bar{A} + \bar{B} \quad (1.9)$$

and

$$\overline{A + B} = \bar{A} \cdot \bar{B} \quad (1.10)$$

Table 1.9 Truth table to prove De Morgan's theorems

A	B	$\bar{A}$	$\bar{B}$	$\overline{AB}$	$\bar{A} + \bar{B}$	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	1	1	1	1
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	0
1	1	0	0	0	0	0	0

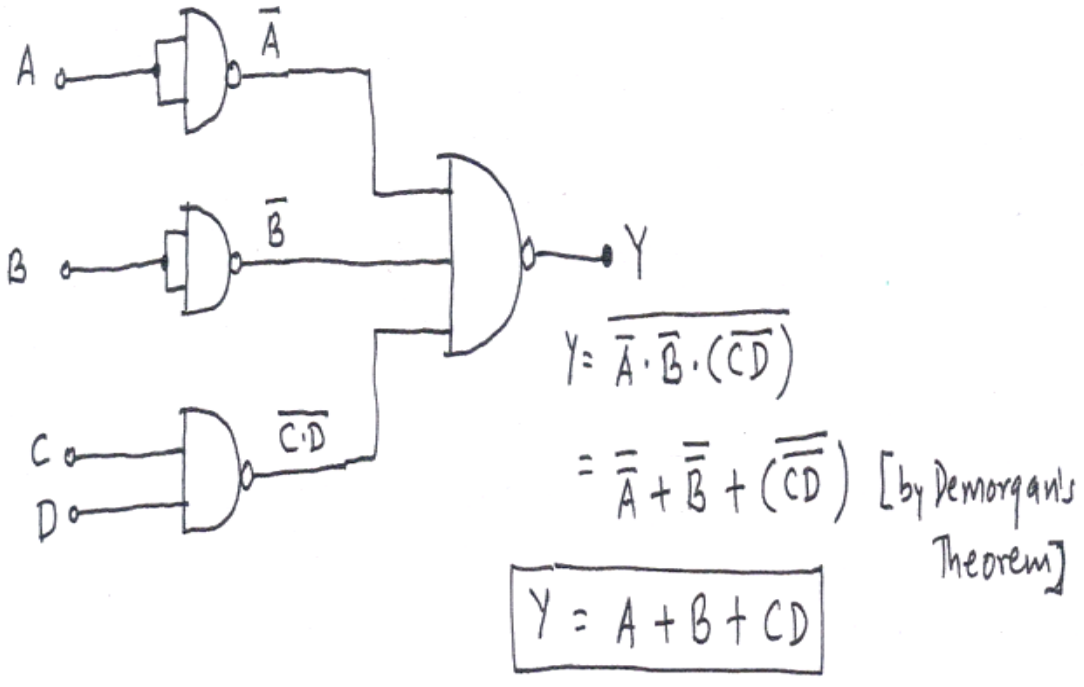
b. Implement the following expressions using NAND gates only.

(i) Y = A + B+ C.D

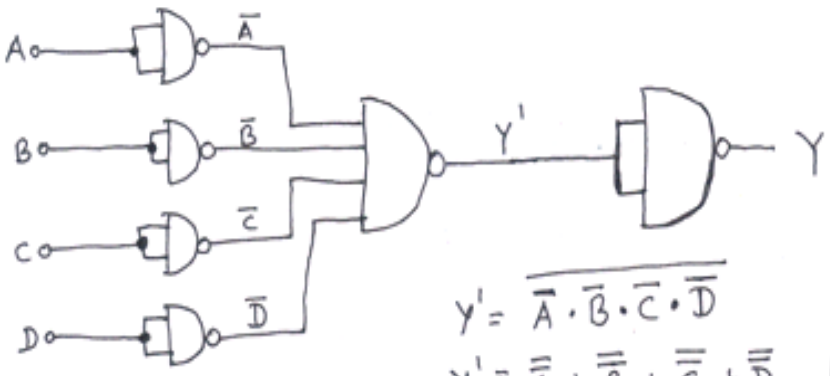
(ii) Y = $\overline{A + B + C + D}$

Answer:

(i)



(ii)



$$Y' = \overline{\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D}}$$

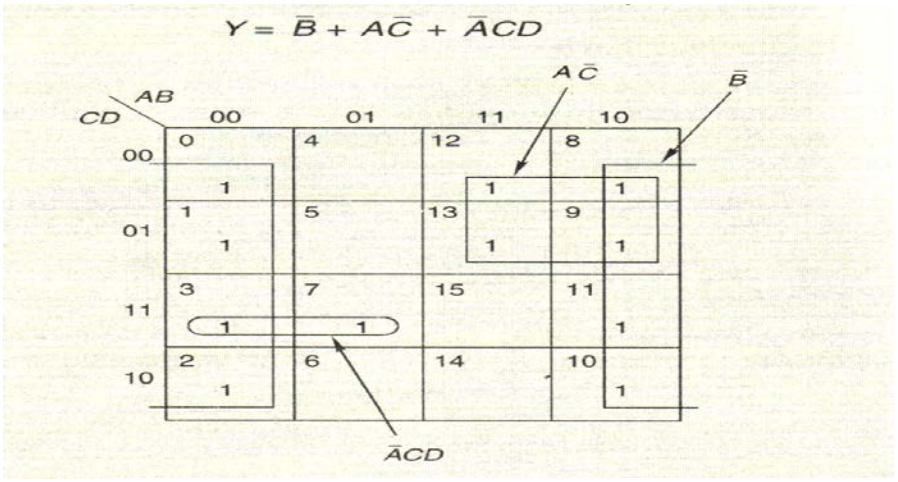
$$Y' = \bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{C}} + \bar{\bar{D}} \quad [\text{by Demorgan's Theorem}]$$

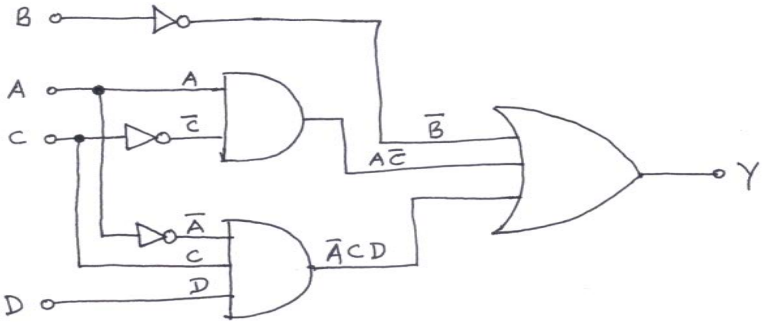
$$Y' = A + B + C + D$$

$$\therefore \quad Y = \bar{Y'} = \overline{A + B + C + D} \quad ..$$

c. Simplify the expression Y = Σ m (0,1,2,3,7,8,9,10,11,12,13) using K-map and implement using basic gates.

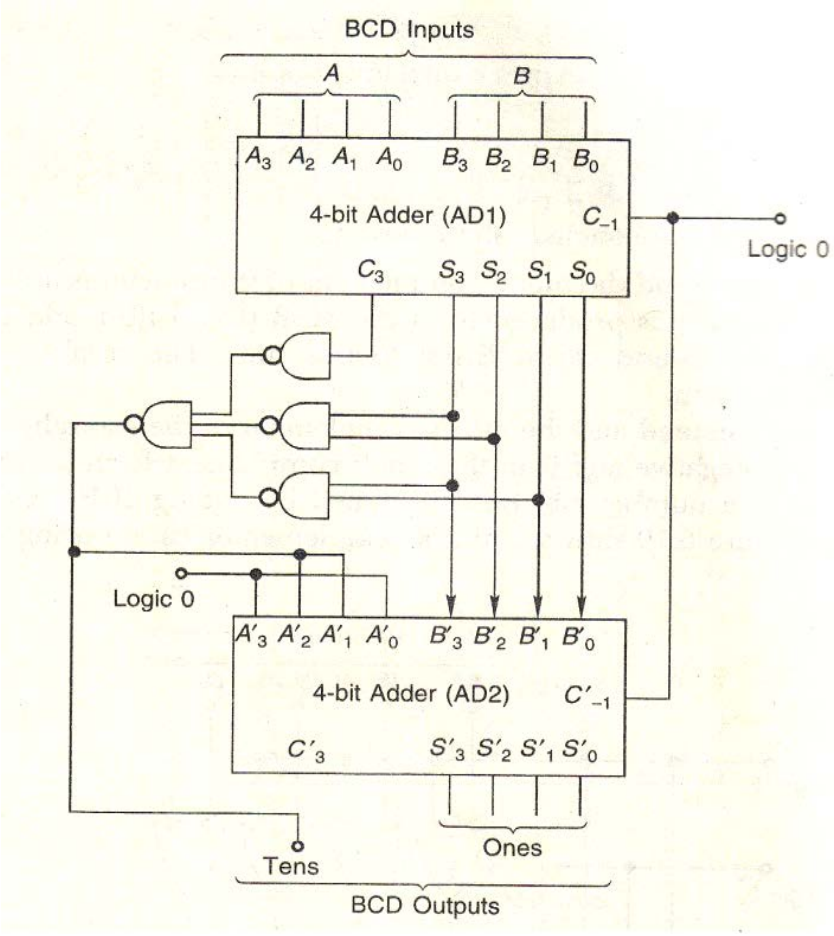
Answer:





Q8. a. Explain 1 digit BCD adder with suitable diagram.

Answer:



It consist of two 4 –bit binary adders, one for each BCD Digit. The C-1 for both adders is 0.

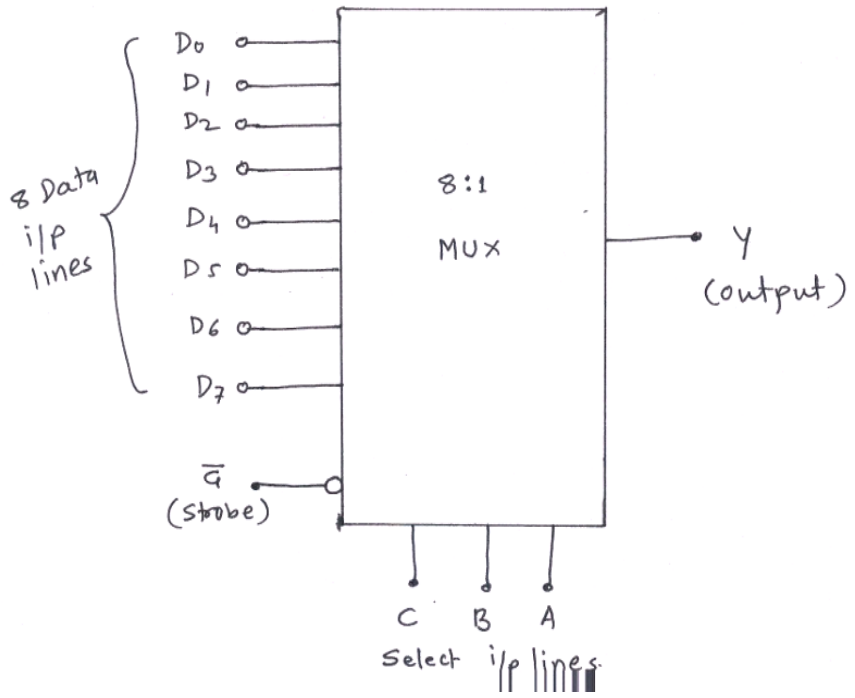
-The first adder (AD1) add the two BCD numbers. If the result of addition is an invalid BCD, (i.e. any number . 1001), then the NAND gate based hardware output becomes logic 1. Hence 6 (0110) gets added to the result of addition as given by AD1 and the valid BCD sum gets available at output pins of AD2

- If the result of addition is a valid BCD, the then the NAND gate based hardware output becomes logic 0. Hence 0 (0000) gets added to the result of addition as given by AD1 and the valid BCD sum gets available at output pins of AD2.

Thus the output sum is always a valid BCD number.

b. Explain the function of 8 : 1 multiplexer with the help of logic diagram and truth table.

Answer:



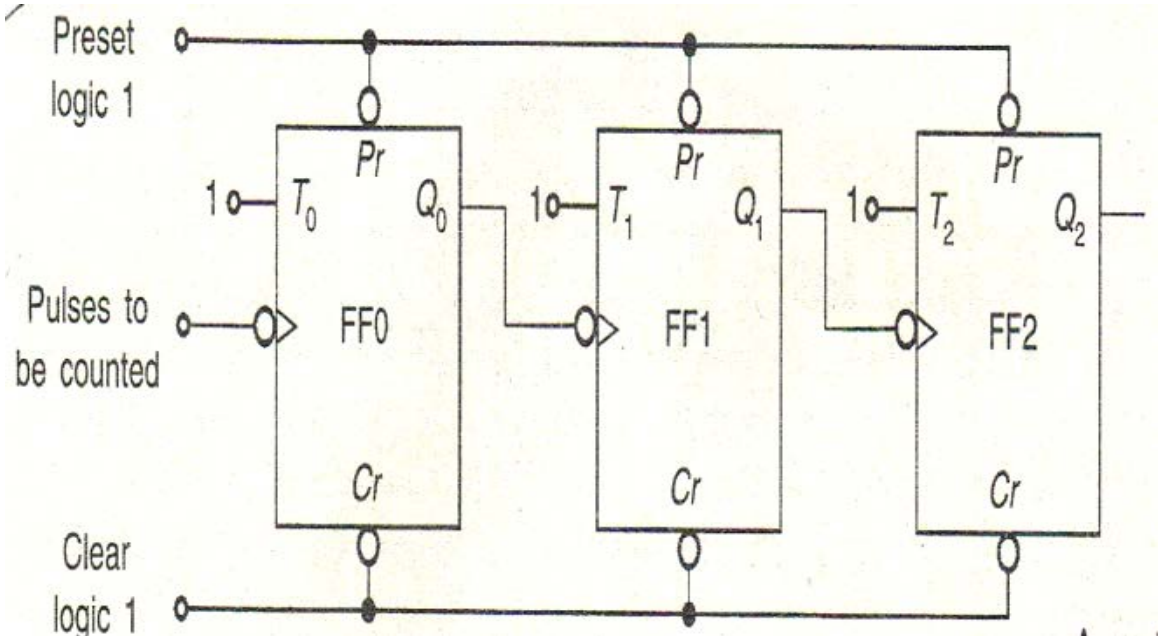
8:1 Mux has 8 data input lines (D0 to D7), 3 select line inputs (2^3 = 8) C,B,A and one strobe input $(\overline{G})$.

The strobe input must be logic 0 for proper functioning of the circuit as per truth table.
Depending upon the logic level on, any one of the input data line from D0 to D7 is selected, it is internally connected to output line Y and data on that selected data line gets transferred to output

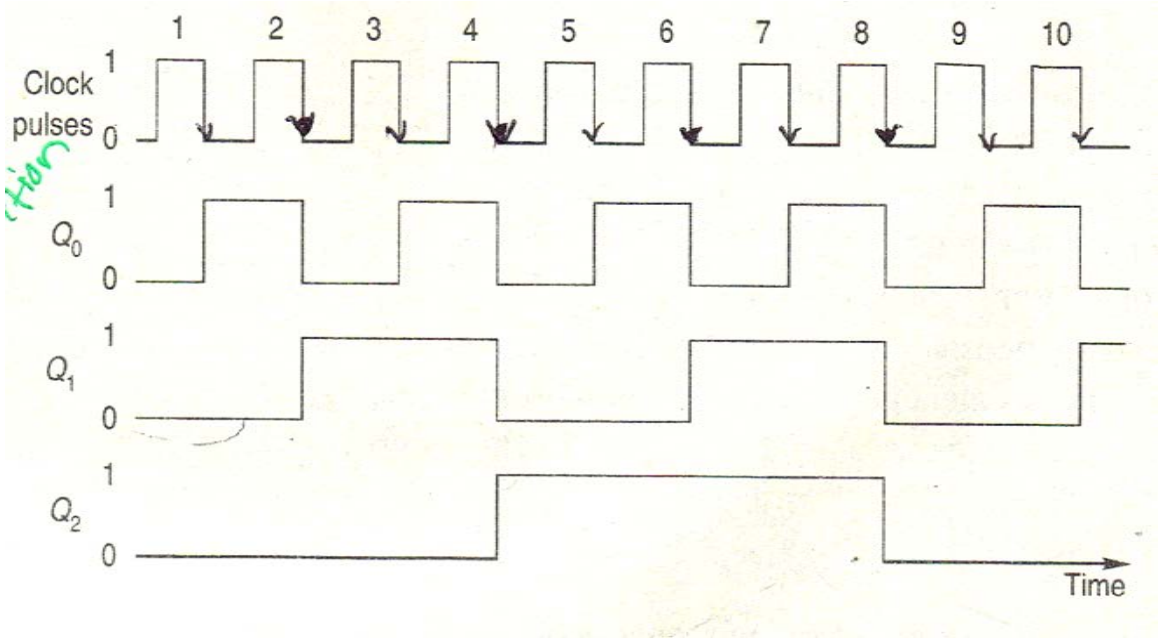
Strobe $(\overline{G})$	Select Inputs			Data Inputs								**o/p (Y)**
	C	B	A	D0	D1	D2	D3	D4	D5	D6	D7	
1	X	X	X	X	X	X	X	X	X	X	X	Z
0	0	0	0	X	X	X	X	X	X	X	X	D0
0	0	0	1	X	X	X	X	X	X	X	X	D1
0	0	1	0	X	X	X	X	X	X	X	X	D2
0	0	1	1	X	X	X	X	X	X	X	X	D3
0	1	0	0	X	X	X	X	X	X	X	X	D4
0	1	0	1	X	X	X	X	X	X	X	X	D5
0	1	1	0	X	X	X	X	X	X	X	X	D6
0	1	1	1	X	X	X	X	X	X	X	X	D7

Q9. a. Explain with waveforms, the implementation of 3 bit ripple counter using suitable flip-flops.

Answer:

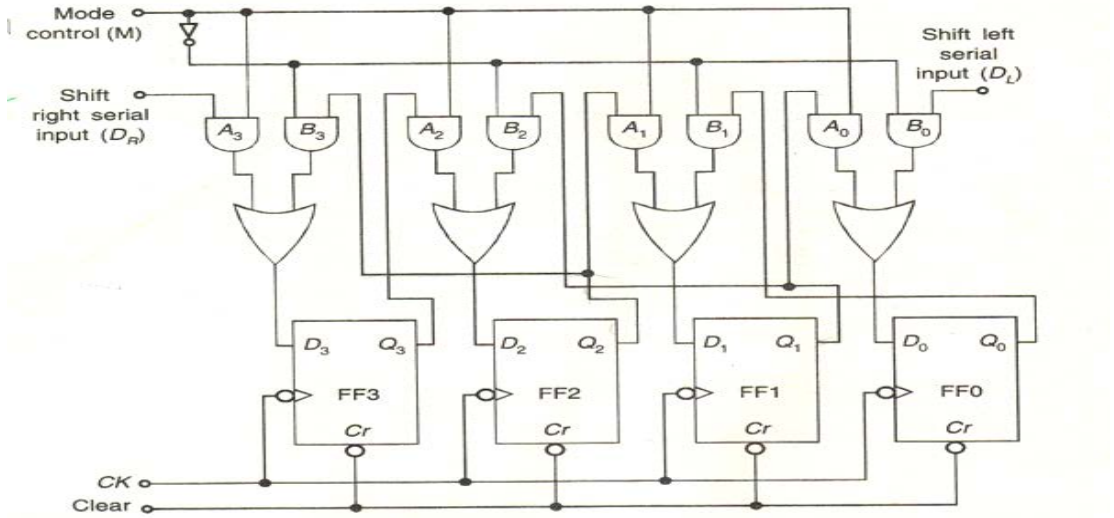


The clock pulses to be counted are given to FF0 while o/p Q0 of FFO is given as clock i/p to FF1 and so on. With T= 1, the o/p of T FF toggles with every negative edge of the clock input. The asynchronous Preset and Clear inputs are held at logic 1 for normal operation.



b. Draw the diagram of four-bit bi-directional shift register using D flip-flops and explain its operation.

Answer:



There are applications in which shifting data to the right and/or to the left is required. For example, a binary number can be divided by two by shifting it one stage to the right. In this process the least-significant bit is lost (unless additional circuitry is used to preserve it) causing an error of 0.5 if the number is odd. Similarly, a number stored in a shift register can be multiplied by two by shifting it one stage to the left, provided a 1 is not shifted out of the most-significant stage. A 4-bit bi-directional shift register is shown in Fig. 8.4.

When the mode control $M = 1$, all the A AND gates are enabled and the data at D_R is shifted to the right when clock pulses are applied. On the other hand, when $M = 0$, the A gates are inhibited and B gates are enabled allowing the data at D_L to be shifted to the left. M should be changed only when $CK = 0$, otherwise the data stored in the register may be altered.

Text Book

(1) Linear Integrated Circuits, Revised 2nd Edition, D Roy Choudhary, Shail B. Jain, New Age International Publishers.

(2) Digital Systems - Principles & Applications, 9th Edition, Ronald J. Tocci , Neal S Widmer & Gregory L. Moss, Pearson Education, 2008.