Q.2 a. Describe the functional unit of a computer system in detail.

Answer:
The computer system is divided into three separate units for its operation. These are 1) arithmetic logical unit, 2) control unit, and 3) central processing unit. 4) Input output unit.

(a) Arithmetic Logical Unit (ALU)
After you enter data through the input device it is stored in the primary storage unit. Arithmetic Logical Unit performs the actual processing of data and instruction. The major operations performed by the ALU are addition, subtraction, multiplication, division, logic and comparison. Data is transferred to ALU from storage unit when required. After processing, the output is returned back to storage unit for further processing or getting stored.

(b)Control Unit The next component of computer is the Control Unit, which acts like the supervisor seeing whether things are done in proper fashion. The control unit determines the sequence in which computer programs and instructions are executed. Things like processing of programs stored in the main memory, interpretation of the instructions and issuing of signals for other units of the computer to execute them. It also acts as a switch board operator when several users access the computer simultaneously. Thereby it coordinates the activities of computer's peripheral equipment as they perform the input and output. Therefore it is the manager of all operations mentioned in the previous section.

(c) Central Processing Unit (CPU)
The ALU and the CU of a computer system are jointly known as the central processing unit. You may call CPU as the brain of any computer system. It is just like a human brain that takes all major decisions, makes all sorts of calculations and directs different part of the computer by activating and controlling the operations.

(d)Input/output unit
A computer must receive both data and program statements to function properly and be able to solve problems. The method of feeding data and programs to a computer is accomplished by an input device. Computer input devices read data from a source, such as magnetic disks, and translate that data into electronic impulses for transfer into the CPU. Some typical input devices are a keyboard, a mouse, or a scanner.

b. Explain the following:
(i) Overflow in integer Arithmetic
(ii) Big-Endian and Little-Endian assignments.

Answer: Page number 32 & 35 of Text Book

Q.3 a. Discuss addressing mode and different types of addressing mode.

Answer:

The addressing mode specifies a rule for interpreting or translating the address field of the instruction into the effective address from where the operand is actually referenced.
□Typesof addressing modes are**Immediate Addressing**:

Direct Addressing:
In direct addressing mode, effective address of the operand is given in the address field of the instruction. It requires one memory reference to read the operand from the given location and provides only a limited address space. Length of the address field is usually less than the word length.
Ex **: Move P, Ro, Add Q, Ro P and Q are the address of operand.**

Indirect Addressing:
Indirect addressing mode, the address field of the instruction refers to the address of a word in memory, which in turn contains the full length address of the operand. The advantage of this mode is that for the word length of N, an address space of 2N can be addressed. He disadvantage is that instruction execution requires two memory reference to fetch the operand Multilevel or cascaded indirect addressing can also be used.

Register Addressing:
Register addressing mode is similar to direct addressing. The only difference is that the address field of the instruction refers to a register rather than a memory location 3 or 4 bits are used as address field to reference 8 to 16 generate purpose registers. The advantages of register addressing are Small address field is needed in the instruction.

Register Indirect Addressing:
This mode is similar to indirect addressing. The address field of the instruction refers to a register. The register contains the effective address of the operand. This mode uses one memory reference to obtain the operand. The address space is limited to the width of the registers available to store the effective address.

Displacement Addressing:
In displacement addressing mode there are 3 types of addressing mode. They are :
1) Relative addressing 2) Base register addressing 3) Indexing addressing.
This is a combination of direct addressing and register indirect addressing. The value contained in one address field. A is used directly and the other address refers to a register whose contents are added to A to produce the effective address.

Stack Addressing:
Stack is a linear array of locations referred to as last-in first out queue. The stack is a reserved block of location, appended or deleted only at the top of the stack. Stack pointer is a register which stores the address of top of stack location. This mode of addressing is also known as implicit addressing.

b. Explain with examples the difference between arithmetic shift and logical shift.

Answer:

Ans. difference between arithmetic shift and logical shift :

Arithmetic shift	Logical Shift
1. In computer programming, an arithmetic shift is a shift operator, sometimes known as signed shift.	1. In computer science, a logical shift is a shift operator that shifts all bits of operands but is not known as signed shift.
2. It Shifted left by is bits on a signed or unsigned binary number has effect of multiplying it by 2^n.	2. A logical shifts is often used when its operand is being treated as a squence of bits rather than numbers.
3. Arithmetic shift has bitwise operations i.e. bitwise left shift, bitwise right shift etc.	3. Logical shift has bitwise logical operation *i.e.* bitwise AND, bitwise OR etc.

Q.4 a. What do you mean by software and hardware interrupts? How these are used in microprocessor?

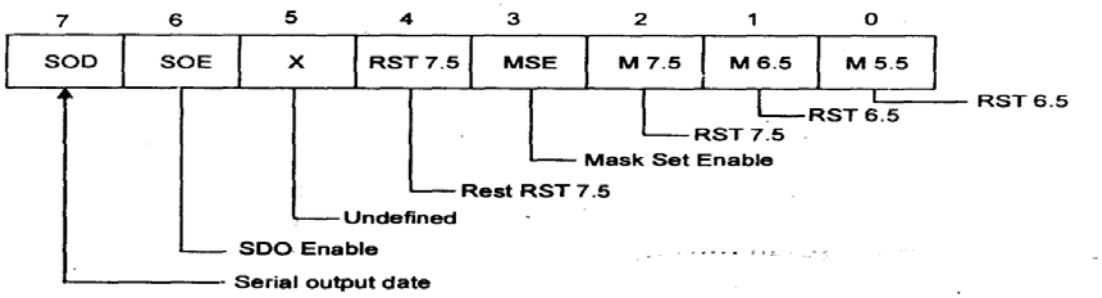
Answer:

Hardware and software interrupts: Interrupts caused by I/O devices are called Hardware interrupt. The normal operation of a micro processor can also be interrupted by abnormal internal conditions or special instruction. Such an interrupt is called a software interrupt. RST is instruction of processor are used for software interrupt. When RST n instruction is inserted in a program, the program is executed upto the point where RST n has been inserted. This is used in debugging of a program.

The internal abnormal or unusual conditions which prevent processing sequence of a microprocessor are also called exceptions. For example, divide by zero will cause an exception. Intel literature do not use the form exception. Where Motorola literature use the term exception. Intel includes exception in software interrupt when several I/O devices are connected to INR interrupt line, an external Hardware is used to interface I/O devices. The external Hardware circuits generate RSTn codes to implement the multiple interrupt scheme.

P.ST 7.5, RST 6.5 and RST 5.5 are maskable interrupts. These interrupts are enabled by software using instructions El and SIM (Set interrupt mask). The excretion of instruction SIM enables/disables interrupts according to hit pattern of accemable. Bit — 0 to 2 rest/ set the mask bits of interrupt mask for RST 5.5, 6.7 and 7.5. Bit 0 for RST 5.5 mask, bit I for RSI 6.5 mask and bit 2 for RST 7.5 mask. If a bit is set of the corresponding interrupt is masked off (disable). If it is

set to 0, corresponding interrupt is enabled. Bit 3 is set to 1 to make bits 0 - 2 effective. Bit 4 is an additional control for RSI 7.5. If it is set to I the flip- flop for RST 7.5 is reset. These RST 7.5 is disabled regardless of whether bit 2 for RST 7.5 is 0 or 1.



b. Explain two approaches to bus arbitration.

Answer: Page number 237 of Text Book

Q.5 a. Explain in detail how the PCI bus operates.

Answer: Page number 261 of Text Book

b. Explain how input and output interfaces can be combined into a single interface. Give circuit diagram for the same

Answer: Page number 252, 253 of Text Book

Q.6 a. What do you mean by memory hierarchy? Describe in detail.

Answer:
Memory is technically any form of electronic storage. Personal computer system have a hierarchical memory structure consisting of auxiliary memory (disks), main memory (DRAM) and cache memory (SRAM). A design objective of computer system architects is to have the memory hierarchy work as through it were entirely comprised of the fastest memory type in the system.

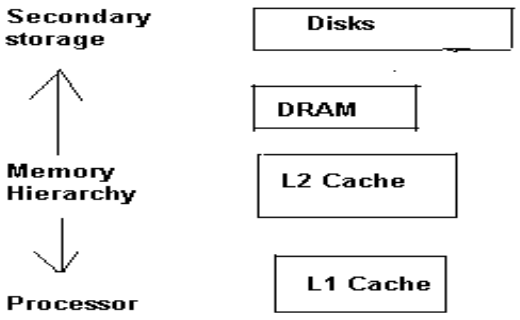
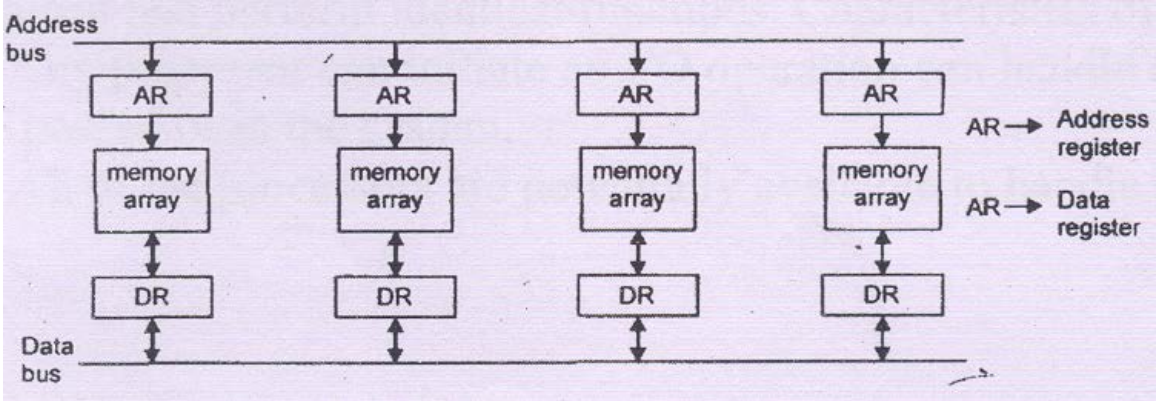


Fig.Memory Hierarchy.

b. What do you mean by interleaved memory? Explain.

Answer:
The memory is partitioned into a number of modules connected to a common memory address and data buses. A primary module is a memory array together with its own addressed data registers. Figure shows a memory unit with four modules.



Q7 a. Define the terms: Seek time, Rotational Delay, Access time.

Answer:
Seek time: Seek time is a time in which the drive can position its read/write ads over any particular data track. Seek time varies for different accesses in tie disk. It is preferred to measure as an average seek time. Seek time is always measured in milliseconds (ms).
Rotational Delay: All drives 1bve rotational delay. The time that elapses between the moment when the read/we heal\settles over the desired data track and the moment when the first byte of required data appears under the head.

Access time: Access time is simply the sum of the seek time and rotational latency time.

b. Explain working of an n-bit ripple-carry adder.

Answer: Page number 368 of Text Book

Q8. a. Give and explain the circuit arrangement for binary division.

Answer: Page number 391 of Text Book

b. Explain, (with the help of suitable examples) IEEE standard for floating-point numbers ( ).

Answer: Page number 395 of Text Book

Q9. a. What do you understand by Fetch cycle, instruction cycle, machine cycle?

Answer

Fetch cycle: The sequence counter is initialized to 0. The program counter (PC) contains the address the first instruction of a program under execution. The address of first instruction from PC is loaded into the address register (AR) during first clock cycle (To). Then instruction from memory location given by address register is loaded into the instruction register (IR) and the program counter is incremented to the address of next instruction in second clock cycle (TL). These micro-operations using register transfer is shown as

$$T_0 : AR \leftarrow PC$$
$$T_1 : IR \leftarrow M[AR], PC \leftarrow PC + 1$$

Instruction cycle: A program in computer consists of sequence of instructions. Executing these instructions runs the program in computer. Moreover each instruction is further divided into sequence of phases. The concept of execution of an instruction through different phases is called instruction cycle. The instruction is divided into sub phases as specified ahead—

1. First of all an instruction in fetched (accessed) from memory.
2. Then decode that instruction.
3. Decision is made for memory or register or I/O reference instruction. In case of memory indirect address, read the effective address from the memory.
4. Finally execute the instruction.

Machine cycle: Machine includes following Hardware components.

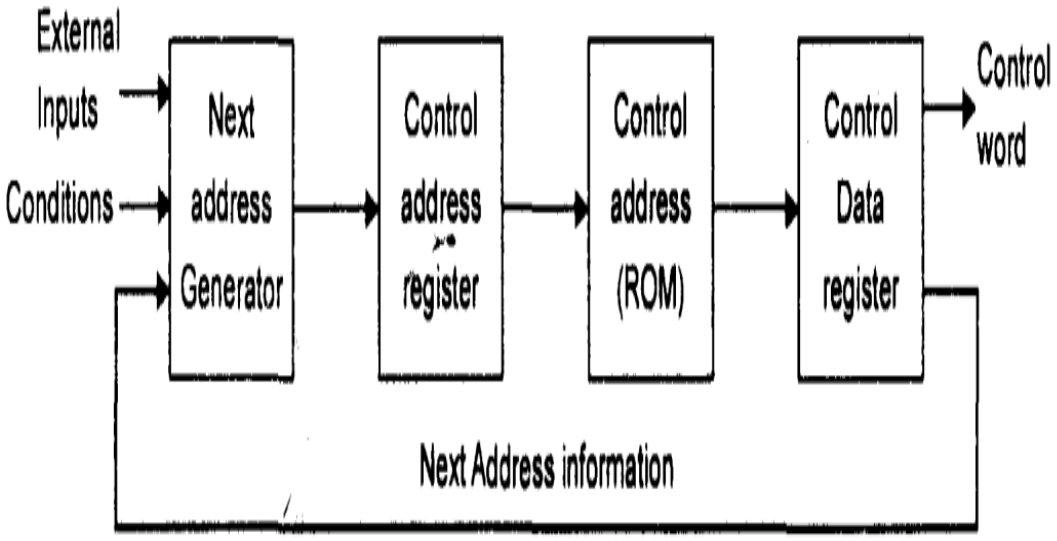
1. A memory unit with 4096 words of 16 bits each.
2. Nine registers.
3. Seven flip-flops.
4. Two decoders : a 3 x 8 operation recorder and a 4 x 16 timing decoder.
5. 16-bit common bus.
6. Control logic gates.
7. Adder and logic circuit connected to the input of AC.

The memory unit is a standard component that can be obtained readily from a commercial source.

b. Explain micro programmed control. Give basic organization of a microprogrammed control unit

Answer:

Micro programming is the latest software concept used in designing the control Unit. This is the concept controlling the sequence of micro operation computer. The operations are performed on data to read inside the registers are called micro operations. Micro programming is the concept for generating control signals using programs, These programs are called micro programs which are designed in control unit.



Text Book

Computer Organization, Carl Hamacher, Zvonko Vranesic, Safwat Zaky, 5th Edition, TMH, 2002.