Q 2 (a) Distinguish between following pair of instructions of 8085

(i) LXI H, 123H and LHLD 1234H
(ii) SPHL and PCHL
(iii) XRA M and ORA M
(iv) RRC and RLC

Answer

(i)LXI H, 123H- Loads 16 bit data (123H) in register pair. Operand is register pait and 16 bit data. This is the only instruction and that can directly load a 16 bit address in the stack pointer register.
LHLD 1234H – Copies the contents of memory location pointed out by 16 bit address register L and copies the contents of the next memory location in register H. Operand is 16 bit address

(ii) SPHL –Copy H and L registers to stack pointer
PCHL-Loads program counter with HL contents

(iii)XRA M and **ORA M**-Both are logical operation instructions. XRA M – the contents of the operand are exclusively OR-ed with contents of the accumulator and result is stored in accumulator .The contents of the operand are unchanged. With ORA instruction the contents of the operand are OR-ed with content of the accumulator and result is stored in accumulator

(iv) RRC –each binary bit of accumulator is rotated right by one position .Bit D0 is placed in D7 as well as in carry flag.
RLC- Each binary bit of accumulator is rotated left by one position. Bit D7 is placed in position D0 as well as in carry flag

Q 2 (b) What is PSW? Write a 8085 assembly program to exchange contents of accumulator and flag register.

Answer Page Number 98 of the textbook

Q 3 (a) Describe the working of the instructions CALL and RET.

Answer Page Number 107 of the textbook

Q 3 (b) Discuss the merits and demerits of I/O-mapped and memory-mapped I/O.

Answer Page Number 129 of the textbook

Q 4 (a) Write an assembly language program to perform block movement without overlap of a block starting at location X to the block staring at location Y.

Answer

```
        ORG C050H
SIZE:   DB   04 H
        ORG C200H
X:      DB 11H, 22H, 33H, 44H
        ORG C000H
Y:      EQU C100H
        LDA SIZE
        MOV C, A      ; Load C with contents of location SIZE
        LXI H, X      ; Load FL with C200H (address of X)
        LXI D Y       ; Load DE with C100J (address of Y)

; The jump instruction here is to perform movement of the byte pointed by HL memory
  to memory pointed   ; by DE
; Pointers DE and HL are incremented and counter is decremented.

LOOP:   MOV A, M
        STAX D        ; Move the byte pointed by HL to memory pointed by DE
        INX H
        INX D
        DCR C ; Increment pointers HL and DE; decrement C
        JNZ LOOP      ; jump to LOOP if result after decrement is nonzero.
        HLT
```

Q 4 (b) Write an assembly language program to find the smallest of N byte binary numbers. N value is stored at location X and numbers start form location X+1.Display the smallest number in the data field and its location in the address field.

Answer

```
        ORG C100H
X :     DB 04H,21H,52H ,32H 46H
        ORG C000H

CURDT:  EQU FFF9H
UPDDT:  EQU 06D3H
CURAD:  EQU FFF7H
```

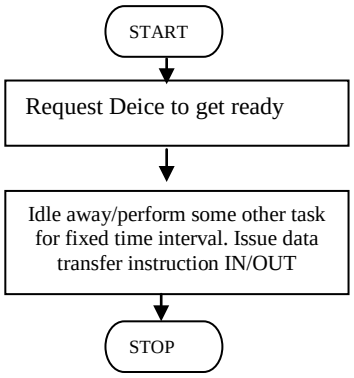
```
                UPDAD:    EQU 06BCH
                          LXI H, X          ; Load c with the number of
elements
                          MOV C, M          ; Decrement C. It indicates number
of comparisonsto be done
                          DCR C             ; for finding smallest number
                          INX H
                          MOV A,M ;         Load A with first element
                          SHLD CURAD        ; Store its location
                AGAIN:    INX H             ; Increment pointer HL
                          CMP M             ; Compare A with content of HL
                          JC SKIP           ; If A is smaller then hump to SKIP
                          MOV A, M          ; Else load A with number pointed by
HL
                          SHLD CURAD
                SKIP :    DCR C             ;Decrement C

                          JNZ AGAIN         ;If nonzero jump to AGAIN
                          STA CURDT
                          CALL UPDDT
                          CALL UPDAD        ; Display the result in
address and data filed
                          HLT
```

Q 5 (a) In how many ways a microprocessor can communicate with an I/O port for parallel data transfer with programmed I/O? Discuss each with proper flowchart.

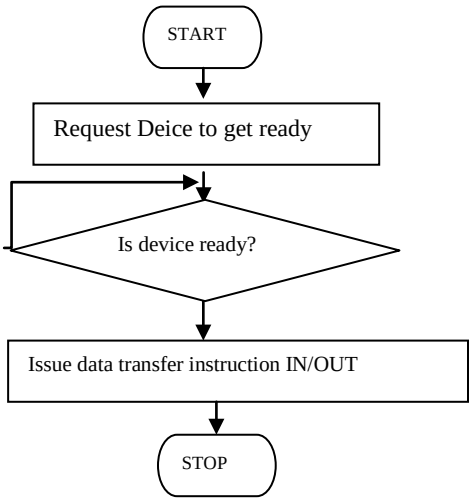
Answer

Microprocessor can communicate with an I/O port for parallel data transfer with programmed I/O in threeways:

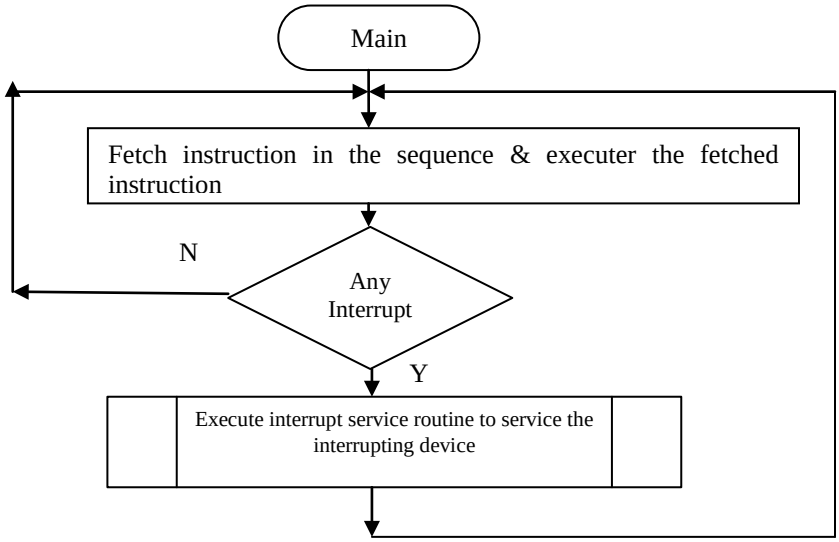
1. Basic /simple data transfer:- Simplest form of data transfer useful when we have accurate knowledge of the I/O device timing characteristics. When the device is ready for data transfer we execute IN or OUT instructions depending upon the direction of data transfer.



2. Status check data transfer: This method is complex than simple data transfer and is used when we do not have knowledge of the I/O device timing characteristics. The processor is kept on loop till it gets status information about the readiness of the I/O device for data transfer. This data transfer is more efficient than simple transfer.



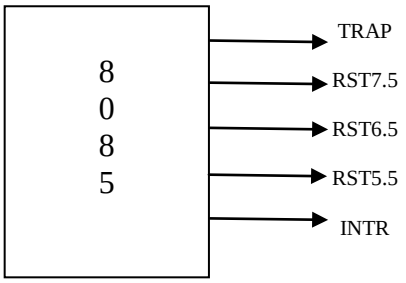
3. Interrupt driven I/O transfer: This is used when we do not have accurate knowledge about he timing characteristics of the I/O device; except that the device takes quite long time to get ready. In such cases status check transfer will waste lot of time of processor so interrupt driven I/O transfer is a preferred choice. The processor goes ahead with the required work and whenever device is ready interrupt request signal is sent to processor If such interrupt request comes half way through during instruction execution then the processor completes the instruction and performs the data transfer with I/O using IN and Out instructions. It again resumes the execution of the previous program. It is the most complex out of all three data transfer schemes but most efficient as does not waste processor time.



Q 5 (b) Explain functions of different interrupt pins available in 8085.

Answer

The interrupt pins of 8085 include: TRAP, RST5.5, RST 6.5, RST 7.5 and INTR. An interrupt can be activated by an I/O port even if processor is half way through an instruction, without having relation to a clock signal. Thus interrupts are asynchronous in nature. At end of every program instruction except those belonging to branch group 8085 checks for these interrupt signals. Functions of these interrupt pins are as mentioned below:



- INTR- Active high input pin having lowest priority level sensitive input. It can get activated when INTR pin is at logic 1 and IE flip flop s in logic 1.Its a non-vectored interrupt.
- RST 5.5 and RST 6.5. - These are level sensitive pins .RST 6.5 pin has higher priority than RST5.5. But both have higher priority than pin INTR. These pins remain high until 8085 checks all internal interrupt signals at the end of an instruction.
- RST7.5- It is edge sensitive pin used by peripherals that send a pulse rather than a sustained high signal. For interrupting a processor, flip flop connected to RST 7.5 is set to 1.This pin ha higher priority than pins RST 6.5, RST 5.5 and INTR.RST 7.5 interrupt cannot be masked by SIM instruction.

TRAP- It is non-maskable both level and edge sensitive interrupt pin. TRAP interrupt signal is activated whenever flip flop associated with it transits from 0 to 1 state or trap pin remains at logic 1 until the end of instruction. It is a vectored interrupt.

Q 6 (b) Write an 8085 assembly program to evaluate two 4-variable Boolean expressions

$X = PQ\overline{R}S + P\overline{Q}R\overline{S} + \overline{P}\,\overline{S}$ **and**

$Y = P\overline{Q}\,\overline{R}\,\overline{S} + P\overline{R}S$

using logic controller interface.

Answer Page Number 346 of the textbook

Q 7 (a) What is the need for interrupt controller in microcomputer system? Draw a neat functional pin diagram of Intel 8259 and state function of various pins.

Answer

Need for interrupt contoller: 8085 has five interrupt pins where five I/O devices can be connected .To connect more than five one has to use polling scheme which results in slow interrupt response. Thus to overcome problem of polling and to connect multiple I/O devices programmable interrupt controller is used

Pin description

- Vcc and GND- Power supply +5V
- D_{7-0}- Eight bidirectional data pins for communication with microprocessor
- RD*- Active low input pin activated by processor to read status information from 8259
- WR*- Active low input pin activated by processor to write control information to 8259
- CS*- Active low input pin for selecting the chip
- A_0- Address input pin. It is used along with RD*/WR*
- IR_0-IR_7- Eight asynchronous interrupt pins. Interrupt requests can be programmed for level triggered mode or edge triggered mode.
- INT- Active high output pin that interrupts the processor.
- INTA*- Active low input pin used to receive signals from INTA* output of 8085.
- CAS_{0-2}-Cascade lines used to cascade multiple 8259 chips.
- SP*/EN*- Stands for slave program/ enable buffer. Its a dual pin which when used as SP*-its active low input and is equal to 0 when 8259 is in slave mode and is equal to 1 when 8259 is master. EN* is active low output pin that controls buffer trans-receivers in buffered mode.

Q 7(b) What is the need for DMA data transfer in microcomputer system? State the function of following pins of DMA controller 8257

(i) Ready **(ii) HLDA**

(iii) HRQ **(iv)** $\overline{IOW}$

(v) TC **(vi)** $\overline{MR}$

Answer

Need for DMA data transfer in microcomputer system-If programmed data transfer is used for reading memory location 3456H and writing output port number 50H ,it takes 13 clocks for reading from memory location with LDA instruction and ten clocks to write output port number .Thus it takes total of 23 clock cycles .If the processor clock frequency is 3MHz with clock period of 0.33μs, it takes 7.66 μs .But if DMA transfer is used it takes only 1.33μs.

Some I/O devices such as hard disk, A/D converter etc have ability to perform high speed data transfer for which programmed data transfer is not suitable choice due to time consumed. DMA data transfer is needed for such situations in which I/O port can access memory directly without processors intervention. The controller circuit supervises DMA data transfer and hence performs faster data transfer operations.

Function of following pins of DMA controller 8257

(i) Ready- Active high input pin Devices with slow input access times can use this pin to insert wait states during DMA read/write machine cycles

(ii) HLDA- Hold acknowledge- Active high input pin connected to HLD output of 8085.When this input pin is active means processor has gone on hold state.

(ii) HRQ- Hold request- Active high output pin connected to HOLD pin of 8085.Whenever it is active corresponding DMA channel is enabled.

(iv) $\overline{IOW}$ - Active low input pin that is activated by the processor to write an AR,CR or the control register when 8257 is in slave mode.

(v) TC-Stands for terminal count. Active high output pin activated when all the LS 14 bit of CR become 0 fro the DMA channel being serviced.

(vi) $\overline{MR}$-Active low pin that is in tri-state when 8257 is in slave mode.

Q 8 (a) Discuss the need of a programmable interval timer in microcomputer system. In how many modes of operation a counter can be configured to work?

Answer

Need of a programmable interval timer in microcomputer system-There are many situations where accurate delays are required to be generated in a microcomputer system. Use of hardware like timer 555 is processor time consuming process .So to introduce accurate delays using hardware programmable interval timer is used. The counters can be configured to work in following modes-

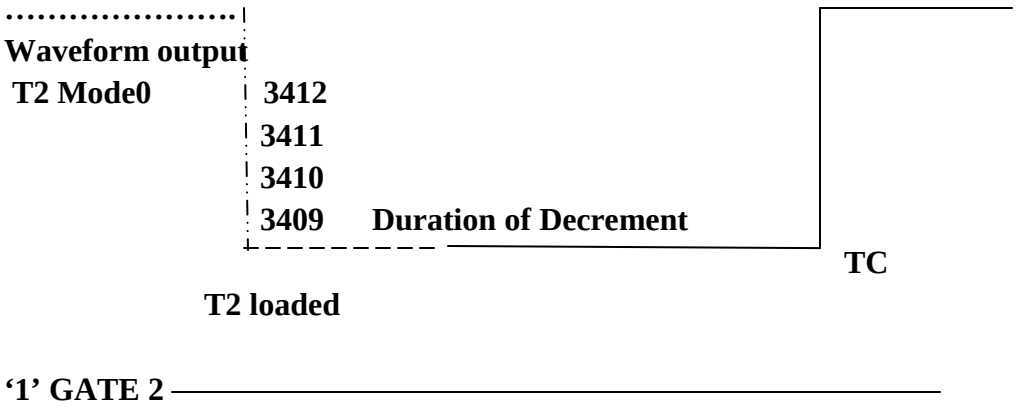
- Mode0 Interrupt on the terminal count
- Mode1- Re-trigger able monostable multi
- Mode 2- rate generator
- Mode3- Square wave generator
- Mode 4- software triggered strobe
- Mode 5- hardware triggered strobe

Q 8 (b) Briefly explain mode 2 operation of 8253

Answer

Mode 0 operation of 8253- Before the counter is set up for mode 0 operation the corresponding output pin will be in tri-state .In mode 0 operation the counter value is copied into the corresponding counter when the processor loads the counter a little later. The count down of counter takes place with every clock pulse as long as gate input is at logic 1.when it reaches TC value of 0000H then the output pin goes high (logic 1)Which can be used to interrupt the processor .Hence the name interrupt on terminal count. The output waveform is shown below-

If the gate input value becomes logic 0 during count down operation it is suspended temporarily .When the gate input becomes logic 1again the count down continues from the pint of suspension.



Q 8 (c) Discuss in brief what information is indicated on Intel 8251 USART control port to configure it for transmission / reception in asynchronous mode?

Answer

Intel 8251 USART configuration for transmission /reception in asynchronous mode: The parallel data to be transmitted in serial format is sent by processor to the transmit buffer of 8251.The transmit buffer is an 8 bit port that can be written but not read by the processor. The processor write to the transmit buffer by activating CS* and WR* inputs of 8251.Intel 8251 programmed and configured to suit our requirements by writing on to the control port. The control port is used to supply information about-mode instruction, synchronization of characters (s) and command instruction. For asynchronous transmission/reception information indicted includes-

- **Number of bits/character**- ASCII code is normally used for representing a character .It uses a 7 bit code. Extended ASCII code used 8 bits that are used when some special characters are to be represented./intel allows user to specify character lengths as 5,6,7 or 8 bits by writing appropriate bit on MI.
- **Parity bit**- Serial communication since used over long distances, during transit data may get corrupted because of noise on the communication medium. The receiver of the data needs to be sure about the correctness of the received data. This is achieved by appending a parity bit at the end of the character. there are two types of parity bits –even and odd. Even parity bit is appended if data has number of 1's in the data are even.
- **Start and stop bit**- The time gap included in the asynchronous transmission/ reception is identified by start bit appended at the beginning and stop bit at the end of the information. When there is nothing to transmit the TxD of 8251 will be in 1 state ,receiver will know that transmission state is on but nothing is being tranmitted.At the

onset on information transmission a start bit is sent which is always logical 0 then LSB of information and then MSB of information ,parity bit is sent then followed by stop bit at the end. Stop bit is always logical 0.The number of stop bits can be programmed to be 1,1.5 or 2 bits.

Even if transmitter/ receiver frequency mismatch exists there is no problem in the communication as with every start bit synchronisation takes place. Also the number of stop bits cater for the time gaps.

Number of characters for transmitting and receiving a bit- Intel 8251 uses a transmit clock TXC* input to send out the information in transmit shift register. For every falling edge of the TxC* a of transmit shift register is sent out on TxD output if 8251 is programmed in X1 mode If X16 mode a bit is sent out for every 16.clock.In X64 mode it is sent out after every 64 clock transmission on TxC*.

Q 9 (a) What is a microcontroller? What are its applications?

Answer Page Number 547 of the Textbook.

Text Book

The 8085 Microprocessor; Architecture, Programming and Interfacing, K. Udaya Kumar and B.S. Umashankar, Pearson Education, 2008