Q2 (a) Write the basic structure of NMOS transistor for enhancement and depletion mode indicating all layers.

Answer Page Number 8,Figure1.4 a, b of Text Book

Q2 (b) With neat sketch explain the NMOS n-well Fabrication process.

Answer Page Number 12 of Text Book

Q2 (c) Compare CMOS technology with Bipolar technology.

Answer

Cmos = Low static power high wise margin pallang quality low o/p quick
Bipolor = high static power low noise margin low poeing high o/p drive

Q3 (a) Derive an expression for I_{ds} in terms of K, $\left(W/L\right)$ ratio and V_{ds} in both saturation and non – saturation.

Answer

Ids = Qc/p, Tsd =L/v= $\frac{b^2}{\mu vds}$

Qc= Eg Eins Eo WL
=WL Eins Eo/D [(Vgs-Vt)-Vds/2]
∴. non saturation region
Ids = Eins Eoll / D w/L [(“gs-vt)-vds/2]vds
=K
Ids = β [(“Vgs-Vt)Vds- $(Vds)^2$ /2]
Saturation region

Ids=k $\frac{W}{L}(\frac{Vgs-Vt}{2})^2$

Ids= $\frac{\beta}{2}(Vgs-Vt)^2$

Q3 (b) With neat circuit diagrams explain the various form of pull up used in MOS circuits. Compare the merits and demerits of each.

Answer

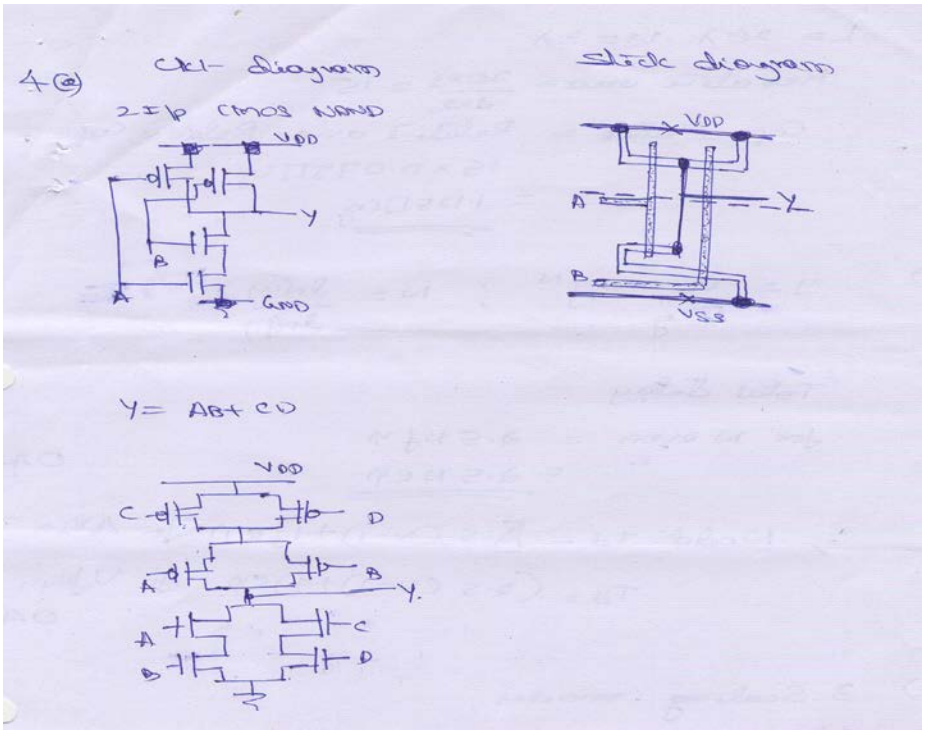
Page Number 45-47 Textbook

1. Load resistance Rl
2. NMoS depletion mode Transistors poll up
3. NMOs enhanced mode Transitor pull up
4. C Mos pull-up

Q4 (a) Write the circuit and stick diagram for

(i) two input CMOS NAND gate
(ii) y = AB+CD

Answer



Q4 (b) Write the design rules of transistor, wires and contacts. Explain briefly with neat sketch

Answer Page Number 74-75 Textbook

Q5 (b) Calculate the capacitance of a metal layer with L = 20 λ and width = 3 λ in terms of standard unit of capacitance.

Answer
L=20λ **W=3** λ
Relaline area = 20*3/2*2=15
Capace lance = Relative a*a*Relation
15*0.075Iicg=1.125 ***cg

Q5 (c) Derive an expression for total delay of N inverters (NfMOS) connected in cascaded form to drive a large capacitive load.

Answer
$y = C_L$/****cg $=f^N$
N=,ln(y)/ln(f)
Total delay
For N even =2.5Nfp

=2.5Nep
nodd: Td =[2.5(N-1)+1]ep for Δ **vin**
Td =(2.5(N-1)+4ep for ∇ **f vin**

Q6 (a) Explain briefly three different scaling models defined in VLSI design.

Answer
Scaling mode

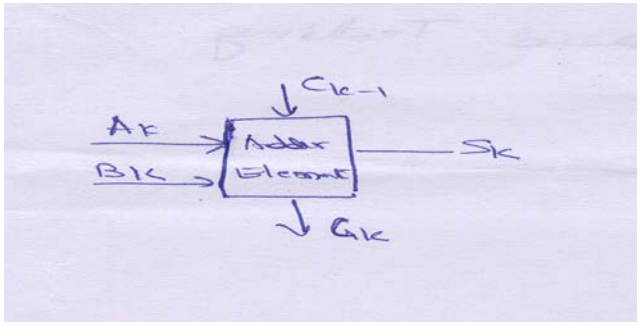
1. Constant electric field scaling model
2. Constant voltage scaling model
3. Combine voltage dimension

Q6 (b) Draw schematic and stick diagram of an 2-input NOR-gate using CMOS and BiCMOS logic.

Answer Page Number 148 Textbook

Q7 (a) Design an adder element that can be cascaded to form 'n' bit adder.

Answer Page Number 215of Text-Book



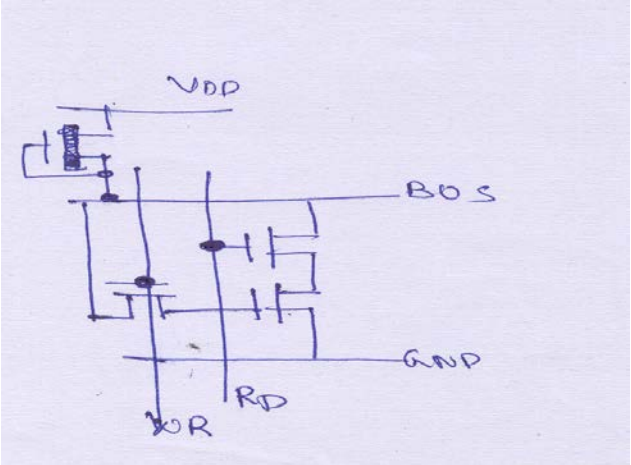
$$S_k = W_k \bar{c}_{k-i} + \bar{H}_k c_{k-1}$$
$$c_k = A_k B_k + H_k c_{k-1}$$
$$A/c = Bk$$
$$S_k = c_{k-1}$$
$$else$$
$$S_k = \bar{c}_{k-1}$$
$$A/c = B/c$$
$$C_k = Ak = Bk$$
$$else$$
$$C_k = c_{k-1}$$

Q7 (b) Write the circuit of Manchester carry chain element. Explain briefly with figure the requirement of buffering in cascaded Manchester carry chain circuit.

Answer Page Number 228 of Textbook

Q8 (a) Write the circuit of three transistor dynamic RAM cell and explain briefly read and write functions.

Answer



Q8 (b) Write note on factors influencing choice of layer for wiring.

Answer Table 10-6 (Page Number - 311) of Text Book

Q9 (a) With an example explain sensitized path based testing used for combination logic circuit.

Answer

Sensilized path based Testing

1. Manifeslation
2. Propagation
3. Consistency

Page Number 337 of Textbook

Q9 (b) Explain DRC, Circuit Extractor and Simulator with example.

Answer Page Number 301-303 of Textbook

Text Book

Basic VLSI Design, Douglas A. Pucknell and Kamran Eshraghian, PHI, 3rd Edition, 2007