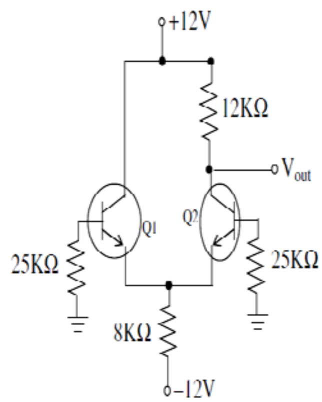
Q2 (a) Classify ICs on the basis of applications, devices used and chip complexity.

Answer Article 1.2 -1.3 of Text Book I

Q2 (b) In the differential amplifier circuit shown below, the transistors have identical characteristics and their β =100. Determine the
(i) Output voltage
(ii) The base currents and
(iii) The base voltages taking into account the effect of the R_B and V_{BE}.
Assume V_{BE}=0.7 Volts, $R_B = 25K\Omega$, $R_C = 12K\Omega$ **and** $R_E = 8K\Omega$.
$V_{EE} = -12V$, $V_{CC} = +12V$



Answer

Ans:

Tail current, $I_T = \frac{V_{EE}}{R_E} = \frac{12v}{8k} = 1.5mA$

The collector current in transistor Q2 is half thus tail current (i.e. 0.75mA) because each transistor gets half the tail current.

$\therefore \quad V_{out} = V_{cc} - I_c. \quad Rc = 12 - (0.75)(10k)$

$V_{out} = 4.5v$

Tail current $I_T = \frac{V_{EE} - V_{BE}}{R_E} = \frac{12 - 0.7}{8k}$

$I_T = 1.41mA$

$V_{out} = V_{cc} - \frac{I_T}{2} XRc = 12 - \frac{1.41m}{2} X12k$

$V_{out} = 3.54$

And Tail current, $I_T = \dfrac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{2\beta dc}}$

$$I_T = \frac{12 - 0.7}{8k + \frac{25k}{2\times100}}$$

$$I_T = 1.390mA$$

And output voltage,

$$V_{out} = V_{cc} - \frac{1}{2} I_T . R_c$$

$$= 12 - \frac{1}{2}\left(\frac{1.390}{2} m\right)(12k)$$

$$V_{out} = 3.66v$$

If the results obtained are compared, we find that the results obtained improve with each refinement, but the improvement is not significant.

$\therefore$ The ideal tail current is 1.41mA

$$\therefore \quad I_B = \frac{I_c}{\beta} = \frac{0.75m}{100} = 7.5\mu A$$

$$\therefore \quad V_B = -I_B . R_B = -(7.5\mu)(25k)$$

$$V_B = -0.1875v$$

Q3 (a) Explain what you understand by 'offset voltage' and 'offset current' of op-amp. Discuss with a neat circuit diagram the technique used for minimizing offset voltage and offset current in an inverting amplifier.

Answer Article 3.2 – 3.4 of Text Book I

Q3 (b) Calculate the output voltage 'V_0' for the following non-inverting op-amp summer with V_1 =2V and V_2 = -1V

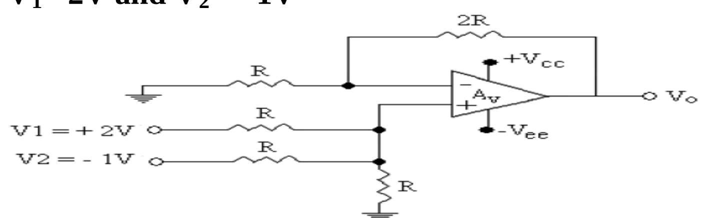


Fig.2

Answer

Ans:

$V_O = ([R_2V_1 + R_1V_2] / [R_1 + R_2])* ([R + R_f] / R)$

If in the summer circuit the value of resistance are selected as $R_1 = R_2 = R$ and $R_f = 2R$. Then

$V_O = - [(2R) V_1/R + (2R) V_2/R]$

$= - [2(V_1 + V_2)]$

$= - [2(2 -1) \ ] = -2$ V

Q4 (a) Explain Schmitt trigger with the help of transfer characteristics. Also obtain the expression of hysteresis voltage V_H and output waveform for sinusoidal input signal.

Answer Article 5.3 of Text Book I

Q4 (b) The input to an op-amp differentiator circuit is a sinusoidal voltage of peak value 10µV and frequency of 2 kHz. If the values of differentiating components are given as R = 40 kΩ and C =3µF, determine the output voltage of differentiator circuit.

Answer

Ans:

$$V_{in} = V_{\max} \sin 2\pi ft = 10\times10^{-6} \sin 2\pi.2000.t$$
$$V_{in} = 10\sin 4000\pi\, t\,\mu v$$
$$\text{Scale factor} = CR = 3\times10^{-6}\times40\times10^{3} = 0.12$$
$$\therefore V_{out} = -CR\frac{dV_c}{dt} = -0.12\frac{d}{dt}(10\sin 4000\pi\, t)\mu v$$
$$V_{out} = -0.12\times10\times\frac{d}{dt}(\sin 4000\pi\, t)\mu v$$
$$V_{out} = 1.2(4000\pi.\cos 4000\pi\, t)\mu v$$
$$V_{out} = 15.0816(\cos 4000\pi\, t)\mu v$$

Q5 (a) Explain the working of R-2R Ladder Digital to Analog Converter.

Answer Article 10.2 of Text Book I

Q5 (b) Explain Monostable multivibrator circuit operation using 555 timers. Also, determine the frequency of output signal.

Answer Article 8.3 of Text Book I

Q5 (c) Explain the working of Series Op-Amp Regulator

Answer Article 6.2 of Text Book I

Q6 (a) Differentiate between analog and digital signals.

Answer Article 1.1 of Text Book II

Q6 (b) Explain the concept of Parity bits with reference to error detection.

Answer Article 2.10 of Text Book II

Q6(c) Convert the following:

(i) $(5A34F)_{16}$ to binary

(ii) $(56)_{10}$ to Gray Code

(iii) $(93)_{10}$ to Excess-3 Code

Answer

(i) (0 1 01 1 0 1 0 0 0 1 1 0 1 0 0 1 1 1 1) $_2$

(ii) 56 = $(111000)_2$= (100100)

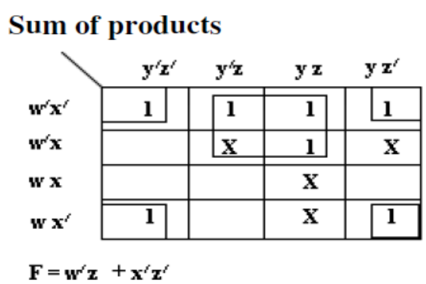
(iii) Ex-3 representation of 93 is 11000110

Q7(a) Simplify the Boolean function 'F' together with don't care conditions 'd' in sum of Products

$F(w, x, y, z) = \sum(0,1,2,3,7,8,10)$

$d(w, x, y, z) = \sum(5,6,11,15)$

Answer



Q7 (b) State and prove De Morgan's theorem using truth table.

Answer Article 3.11 of Text Book II

Q7 (c) Show that NAND gate is a Universal gate.

Answer Article 3.12 of Text Book II

Q8 (a) Explain the 4-bit parallel binary adder.

Answer Article 6.10 of Text Book II

Q8 (b) Write a short note on 8: 1 Multiplexers

Answer Article 9.5 of Text Book II

Q9 (a) Draw and explain the working of NAND-gate latch.

Answer Article 6.1 of Text Book II

Q9 (b) Distinguish between synchronous and asynchronous counters. Design a 3-bit UP-DOWN synchronous counter.

Answer

Difference between synchronous and asynchronous counter:

1. In synchronous counters synchronized at the same time. But in the case of asynchronous counter the output of first flip-flop is given as the clock input of the next flip-flop.

2. In synchronous counter the output occurs after nth clock pulse if number of bits are N. But in asynchronous counter the output is derived by previous one that's why n+1 step or clock pulse will be required.

Design of 3 bit UP DOWN counter:-

For M = 0, it acts as an UP counter and for M = 1 as a DOWN counter. The number of flip-flop required is 3. The input of the flip-flops are determined in a manner similar to the following table.

Truth Tables

Direction	Present State			Required FlipFlop					
M	Q_3	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	0	1	X	0	X	0	X
0	0	0	1	X	1	1	X	0	X
0	0	1	0	1	X	X	0	0	X
0	0	1	1	X	1	X	1	1	X
0	1	0	0	1	X	0	X	X	0
0	1	0	1	X	1	1	X	X	0
0	1	1	0	1	X	X	0	X	0
0	1	1	1	X	1	X	1	X	1
1	0	0	0	1	X	0	X	1	X
1	1	1	1	X	1	1	X	X	0
1	1	1	0	1	X	X	0	X	0
1	1	0	1	X	1	X	1	X	0
1	1	0	0	1	X	0	X	X	1
1	0	1	1	X	1	1	X	0	X
1	0	1	0	1	X	X	0	0	X
1	0	0	1	X	1	X	1	0	X

From truth table

The $J_0 = K_0 = 1$

$J_1 = K_1 = Q_0\overline{M} + \overline{Q_0}M$

$J_2 = K_2 = \overline{M}Q_1Q_0 + M\overline{Q_1}\,\overline{Q_0}$

Connecting the equations of all the flip-flops into NAND realization circuit

$J_1 = K_1 = Q_0\overline{M} + \overline{Q_0}M$

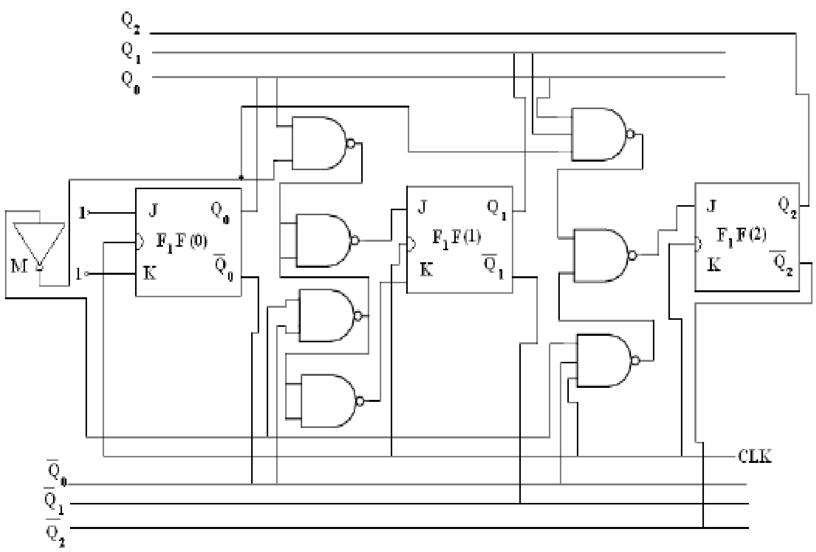
$= \overline{Q_0\overline{M} + \overline{Q_0}M}$

$= \overline{Q_0\overline{M}}.\overline{\overline{Q_0}M}$

$J_2 = K_2 = \overline{M}Q_1Q_0 + M\overline{Q_1}\,\overline{Q_0}$

$= \overline{\overline{M}Q_1Q_0 + M\overline{Q_1}\,\overline{Q_0}}$

$= \overline{\overline{M}Q_1Q_0.M\overline{Q_1}\,\overline{Q_0}}$



Logic diagram of 3 bit UP – DOWN Counter

Text Book

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2. Digital Systems – Principles and Applications, Ninth Edition, Ronald J Tocci, Neal S Widmer and Gregory L. Moss, Pearson Education, 2008.