Q.2 a. What is power loss in an ideal switch? Explain the conduction losses in a bipolar junction transistor with the help of circuit diagram. (8)

Answer:

1.5 Power Losses in Real Switches

An ideal switch is shown in Figure 1.5. The power loss generated in the switch is the product of the current through the switch and the voltage across the switch. When the switch is off, there is no current through it (although there is a voltage V_S across it), and therefore there is no power dissipation. When the switch is on, it has a current (V_S/R_L) through it, but there is no voltage drop across it, so again there is no power loss. We also assume that for an ideal switch the rise and fall time of the current is zero. That is, the ideal switch changes from the off state to the on state (and vice versa) *instantaneously*. The power loss during switching is therefore zero.

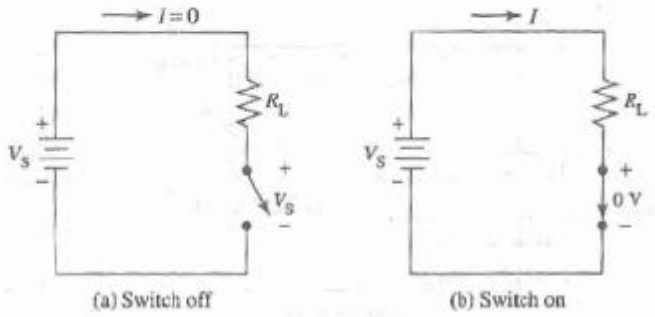


Figure 1.5
Power losses in an ideal switch

Unlike an ideal switch, an actual switch, such as a bipolar junction transistor, has two major sources of power loss: conduction loss and switching loss.

1.5.1 Conduction Loss

When the transistor in Figure 1.6(a), is off, it carries a *leakage current* (I_{LEAK}). The power loss associated with leakage current is $P_{OFF} = V_S * I_{LEAK}$. However, since the leakage current is quite small and does not vary significantly with voltage, it is usually neglected and thus the transistor power loss is essentially zero. When the transistor is on, as in Figure 1.6(b), it has a small voltage drop across it. This voltage is called the *saturation voltage* ($V_{CE(SAT)}$). The transistor's power dissipation or conduction loss due to the saturation voltage is:

$$P_{ON} = V_{CE(SAT)} * I_C \quad 1.1$$

where

$$I_C = \frac{V_S - V_{CE(SAT)}}{R_L} \approx \frac{V_S}{R_L} \quad 1.2$$

Equation 1.1 gives the power loss due to conduction if the switch remains on indefinitely. However, to control the power for a given application, the switch is turned on and off in a periodic manner. Therefore, to find the average power loss we must consider the duty cycle:

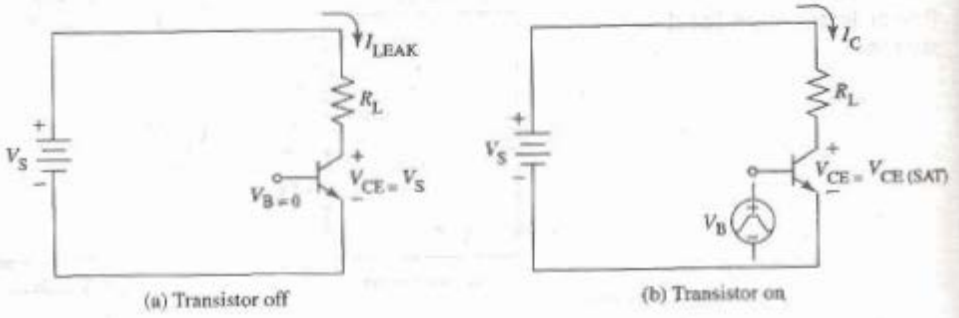
$$P_{ON(avg)} = V_{CE(SAT)} * I_C * \frac{t_{ON}}{T} = V_{CE(SAT)} * I_C * d \quad 1.3$$

Similarly,

$$P_{OFF(avg)} = V_S * I_{LEAK} * \frac{t_{OFF}}{T} \quad 1.4$$

Here, the duty cycle d is defined as the percentage of the cycle in which the switch is on:

$$d = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{t_{ON}}{T} \quad 1.5$$



(a) Transistor off (b) Transistor on

losses in a switch

b. Explain, how the power diode must be protected against the following:-(8)
(i) Overvoltage
(ii) Overcurrent
(iii) Transients

Answer:

2.9 Diode Protection

A power diode must be protected against overvoltage, overcurrent and transients.

2.9.1 Overvoltage

When a diode is forward-biased, the voltage across it is low and poses no problems. A reverse-biased diode acts like an open circuit. If the voltage across the diode exceeds its breakover voltage, it breaks down, resulting in a large current flow. With this high current and large voltage across the diode, it is quite likely that the power dissipation at the junction will exceed its maximum value, destroying the diode. It is a common practice to select a diode with a peak reverse voltage rating that is 1.2 times higher than the expected voltage during normal operating conditions.

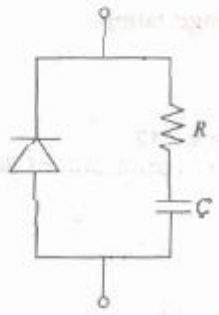
2.9.2 Overcurrent

Manufacturer's data sheets provide current ratings based on the maximum junction temperatures produced by conduction losses in diodes. In a given circuit, it is recommended that the diode current be kept below this rated value. Overcurrent protection is then accomplished by using a fuse to ensure that the diode current does not exceed a level that will increase the operating temperature beyond the maximum value.

2.9.3 Transients

Transients can lead to higher-than-normal voltages across a diode. Protection against transients usually takes the form of an RC series circuit connected across the diode. This arrangement, shown in Figure 2.11, snubs or reduces the rate of change of voltage and is commonly called a *snubber circuit*.

Figure 2.11
A snubber circuit



Q.3 a. How does a Power Bipolar Junction Transistor used as a switch? Draw its V-I characteristics and explain the significance of saturation, active and cut-off regions. (8)

Answer:

3.2 Power Bipolar Junction Transistors (BJTs)

Power transistors are available in both NPN and PNP types. However, we will concentrate on the NPN device, since it has a higher current and voltage rating than the PNP device. The structure and symbol of an NPN transistor are shown in Figure 3.1. This type of transistor is called a *bipolar junction transistor* (BJT). BJT is usually referred to as a transistor.

A transistor has three terminals: the *base* (B), the *collector* (C) and the *emitter* (E). The collector and the emitter in a transistor are not reversible. In fact the transistor's characteristics and ratings change significantly when these two terminals are reversed. If the arrowhead on the emitter points toward the base, the transistor is a PNP transistor. If the arrow points away from the base, it is an NPN transistor.

When a transistor is used as a switch to control power from the source to the load, terminals C and E are connected in series with the main power circuit, while terminals B and E are connected to a driving circuit that controls the on and off action. A small current through the base-emitter junctions turns on the collector-to-emitter path. This path may carry many times more current than the base-emitter junction.

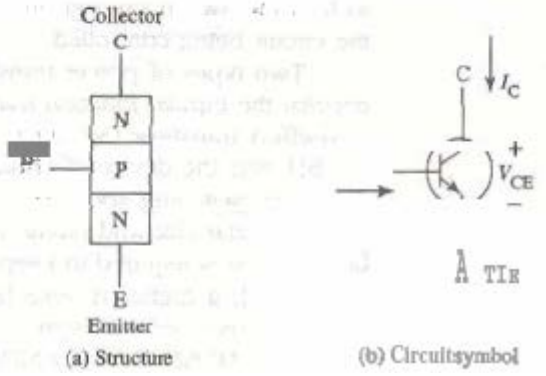


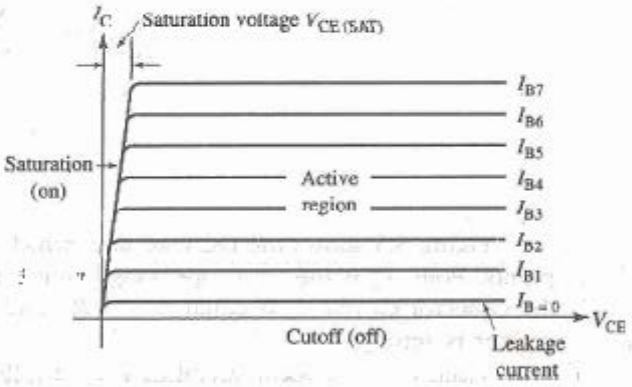
Figure 3.1 An NPN transistor and its symbol

3.2.1 BJT V-I Characteristics

Since most applications of power transistors have a common emitter connection, the characteristic will be explained for that configuration. Figure 3.2 shows the V-I characteristic of a transistor. There s of operation, the cutoff, saturation, and active regions. If the base current I_B is zero, the collector current I_C is negligibly small and the transistor is in the cutoff region, which is *the* off state of the tr tor. In this region bo h *the* collector-base and base-emitter junctions are reverse-biased and the transistor behaves as an open switch. On the other hand, if the base current I_B is sufficient to drive the transistor into saturation (the collector current is very high and V_{CE} is approximately zero), then the transistor behaves as a closed switch. In the saturation region, both junctions are forward-biased. In the active region of operation, the base-emitter junction is forward-biased while the collector-base junction is reverse-biased. The active region is used for amplification and is avoided in switching applications.

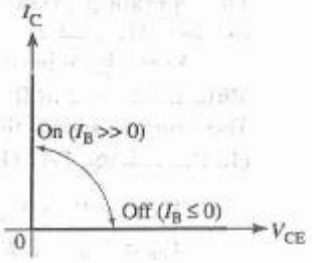
Note that the V-I characteristic does not show any reverse region. A BJT cannot block more than about 20 V in the reverse direction. Therefore BJTs are not used to control AC power, unless a reverse shunting diode is connected between the emitter and the collector to protect the transistor from reverse voltages.

Figure 3.2
BJT *V-I* characteristic



Since transistors are used mainly as switches, the idealized transistor characteristic is of prime importance. Figure 3.3 shows the V-I characteristic of a BJT

Figure 3.3
Idealized characteristic of a transistor



operating as a switch. When the transistor is off, there is no collector current no matter what the value of V_{CE} is. When the transistor is on, the voltage V_{CE} is zero no matter what the value of the collector current is. A transistor has excellent characteristics as an ideal switch.

3.2.2 Biasing a Transistor

When a transistor is used as a controlled switch, the base current is provided by the control circuit connected between the base and the emitter. The collector and the emitter form the power terminals of the switch. Figure 3.4 shows how an NPN transistor is biased. The input base current I_B determines whether the transistor switch will be off (with no current to the load R_C) or on (allowing current to flow).

Figure 3.4
Biasing a transistor

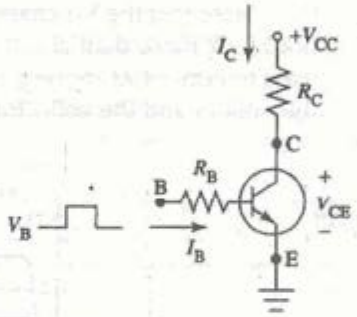


Figure 3.5 shows the DC load line, which represents all possible operating points. Point P_1 is the ideal operating point for the switch when it is on. Here the collector current I_C is equal to V_{CC}/R_C, and the voltage across the collector-emitter is zero.

Point P_4 is the ideal operating point for the switch when it is off. Here the collector current I_C is zero and the voltage across the collector-emitter is equal to the supply voltage V_{CC}.

The line drawn between points P_1 and P_4 is the load line. The intersection of the load line with the base current is the operating point of the transistor. The operating point is determined by the circuit that is external to the transistor, i.e., V_{CC} and R_C.

Point P_2, where the load line intersects the $I_B = 0$ curve, is the actual operating point at cutoff. At this point, the collector current is the leakage current. The voltage across the collector-emitter terminal can be found by applying Kirchoff's voltage law (KVL) around the output loop:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C \qquad \textbf{3.1}$$

Point P_3, where the load line intersects the $I_B = I_{B(sat)}$ curve, is the actual operating point when the BJT is on. Point P_3 is called the saturation point. An on transistor has a small voltage drop across its collect-emitter terminals; this voltage is called the saturation voltage $V_{CE(sat)}$. The collector current is at a maximum here and is given by

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \approx \frac{V_{CC}}{R_C} \qquad 3.2$$

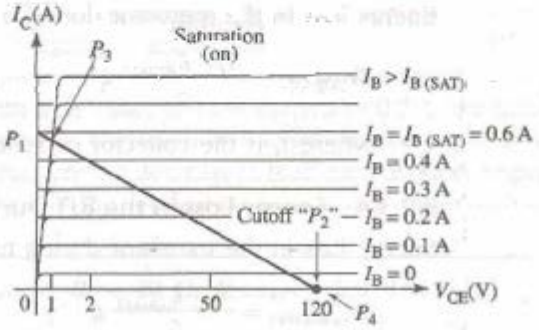
The minimum base current required to ensure satisfactory operation is given by

$$I_B = \frac{I_{C(sat)}}{\beta} = \frac{V_{CC}}{\beta R_C} \qquad 3.3$$

where β is the DC current gain given by I_C/I_B.

Any value of I_B higher than the value calculated using Equation 3.3 will ensure a saturated on state. In fact, to accommodate any changes in I_C above the required value, it is desirable to use a little higher value of base current than is obtained by the above formula. A high base current also reduces the turn-on time and therefore reduces power dissipation.

Figure 3.5 DC load line



All operating points between cutoff and saturation are in the active regions of a transistor. In this region, both I_C and V_{CE} are relatively high, resulting in high power dissipation in the transistor.

b. A Power MOSFET has I_{DSS} = 2 mA, $R_{DS(ON)}$ = 0.3 Ω, duty cycle d = 50%, I_D = 6 A, V_{DS} = 100 V, t_r = 100 ns and t_f = 200 ns. If the frequency of switching is 40 KHz, then find (8)

(i) on-state loss

(ii) off-state loss

(iii) turn-on switching loss

(iv) turn-off switching loss

Answer:

Given Data I_{DSS} = 2 mA, $R_{DS(ON)}$ = 0.3 Ω, duty cycle (d) = 50%, I_D = 6 A, VDS = 100 V, t_r = 100 ns, t_f = 200 ns and frequency of switching(f) = 40 kHz

The Time Period (T) = $\frac{1}{f} = \frac{1}{40(10^3)} = 25\ \mu S$

Therefore, $t_{ON} = t_{OFF} = \frac{T}{2} = 12.5\ \mu S$

(i) On-State Loss (P_{ON}) = $I_D^2 R_{DS(ON)} \frac{t_{ON}}{T} = \frac{6^2 X 0.3 X 12.5(10^{-6})}{25(10^{-6})}$ = 5.4 W.

(ii) Off-State Loss (P_{OFF}) = $V_{DS(max)} I_{DSS} \frac{t_{OFF}}{T} = \frac{100 X 2(10^{-3}) X 12.5(10^{-6})}{25(10^{-6})}$ = 0.1W

(iii) Turn-on Switching Loss ($P_{SW(ON)}$) =

$$\frac{V_{DS(\max)} I_D t_r}{6} X\ f = \frac{100 X 6 X 100(10^{-9})}{6} X 40(10^3) = 0.4 \text{ W}.$$

(iv) Turn-off Switching Loss ($P_{SW(OFF)}$) =

$$\frac{V_{DS(\max)} I_D t_f}{6} X\ f = \frac{100 X 6 X 200(10^{-9})}{6} X 40(10^3) = 0.8 \text{ W}.$$

Q.4 a. What is the necessity of connecting two SCRs in parallel? Draw the circuit of connecting two SCRs in parallel and explain its operation with the help of on-state characteristics. (9)

Answer:

The maximum power that can be controlled by a single SCR is determined by its rated forward current and rated forward blocking voltage. To maximize one of these two ratings, the other has to be reduced. Although SCRs are currently available with very high voltage ratings, in many applications, such as transmission lines, the required voltage rating exceeds the voltage that can be provided by a single SCR. Then it is necessary to connect two or more SCRs in series. Similarly, for very high current applications, SCRs have to be connected in parallel. For high-voltage, high-current applications, series-parallel combinations of SCRs are used.

4.8.2 SCRs in Parallel

When the load current exceeds the rating of a single SCR, SCRs are connected in parallel to increase their common current capability. If SCRs are not perfectly matched, this results in an unequal sharing of current between them. Figure 4.17 shows the *V-I* characteristics of two SCRs, SCR_1 and SCR_2. The ratings of the SCRs are the same. When these SCRs are connected in parallel, they will have equal voltage drops V_{SCR} across them. However, due to their mismatch in characteristics, SCR_2 is carrying the rated current (I_2), while SCR_1 is carrying a current I_1, which is much less than its rated value. The total rated current of the parallel connection is only $I_1 + I_2$ instead of $2I_2$.

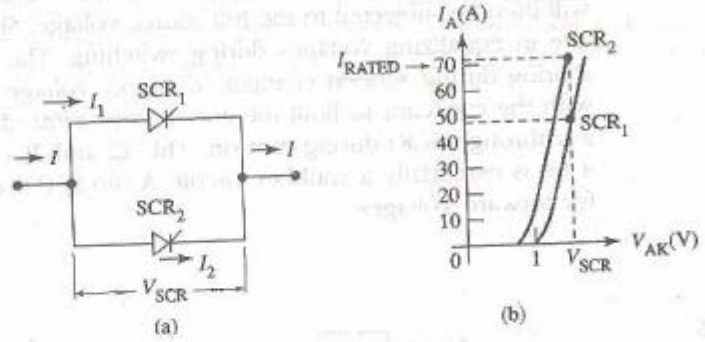


Figure 4.17
Current sharing between two parallel SCRs (a) two SCRs in parallel (b) on-state characteristics

Matched-pair SCRs are generally available for parallel connection, but they are very expensive. With unmatched SCRs, equal current sharing is enforced by adding a low-value resistor or inductor in series with each SCR. Forced current sharing using equal-value resistors is shown in Figure 4.18. The basic requirement is to make current I_1 close to I_2; a maximum difference of 20% is acceptable. If we assume the voltage V_1 across SCR_1 to be greater than the voltage V_2 across SCR_2, the value of R can be obtained from

$$I_1R + V_1 = I_2R + V_2$$

$$R = \frac{V_1 - V_2}{I_2 - I_1} \qquad 4.11$$

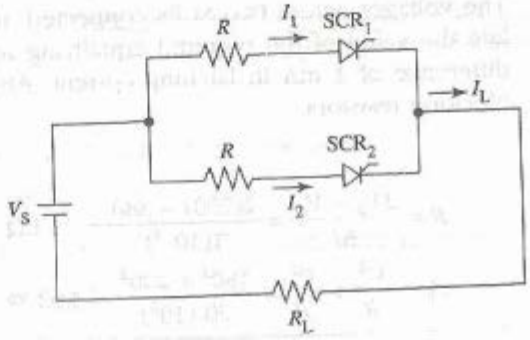


Figure 4.18
Forced current sharing using resistors

b. What are the most common methods of achieving commutation? Explain the commutation method by external source and explain its operation with the help of waveforms. (7)

Answer:

If an SCR is forward-biased and a gate signal is applied, the device turns on. However, once the anode current I_A is above the holding current, the gate loses control. The only way to turn the SCR off is to reduce the anode current below the holding current value or to make the anode negative with respect to the cathode. The process of turnoff is known as *commutation*. In AC applications, the required condition for turnoff is achieved when the source reverses during the negative half-cycle. This method is called *natural* or *line commutation*. For DC applications, additional circuitry must be used to turn the SCR off. These circuits first force a reverse current through the SCR for a short period to reduce the anode current to zero. They then maintain the reverse bias for the necessary time to complete the turnoff. This process is called *forced commutation*.

It should be noted that if a forward voltage is applied instantly after the anode current is decreased to zero, the SCR will not block the forward voltage and will start conducting again, even though it is not triggered by a gate pulse. It is therefore important to keep the device reverse-biased for a finite time, called the *turnoff time* (t_{OFF}), before a forward anode voltage can be applied. The turnoff time of an SCR is specified as the minimum period between the instant the anode current becomes zero and the instant the device is able to block the forward voltage.

SCR turnoff can be accomplished in the following ways:

1. diverting the anode current to an alternate path
2. shorting the SCR from anode to cathode
3. applying a reverse voltage *(by making the cathode positive with respect to the anode)* across the SCR
4. forcing the anode current to zero for a brief period
5. opening the external path from its anode supply voltage
6. momentarily reducing the supply voltage to zero

The most common methods of achieving commutation are discussed briefly in the following subsections.

1. Capacitor Commutation
2. Commutation by Resonance
3. AC Line Commutation

4.14.2 Commutation by External Source

In this type of commutation circuit, the commutation energy is obtained from an external source in the form of a pulse. A simple circuit is shown in Figure 4.29. The pulse generator reverse-biases the SCR and thus turns it off. The pulse width must be such that the SCR is reverse-biased for a period greater than the turnoff time of the SCR.

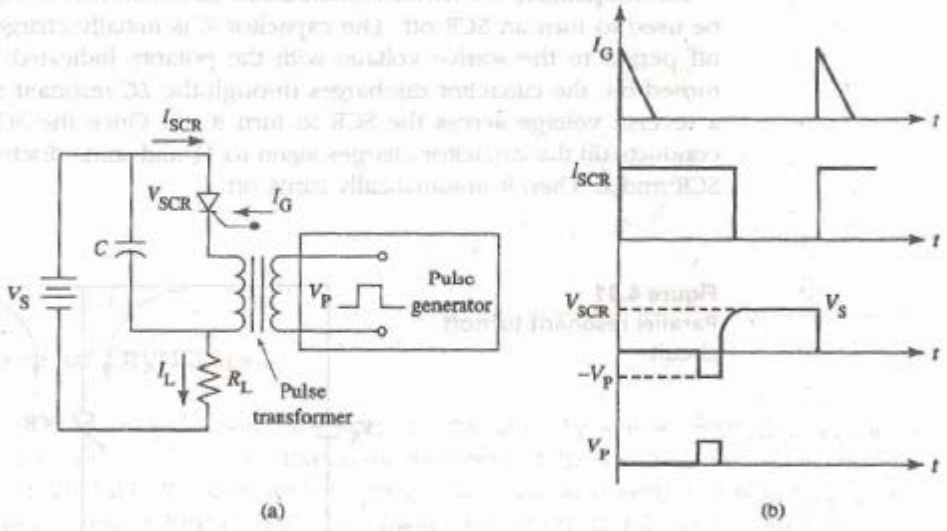


Figure 4.29
Commutation by external source (a) circuit (b) waveforms

When the SCR is triggered by applying a gate signal, current flows through the SCR, the secondary of the pulse transformer, and the load. To turn the SCR off, a positive pulse from the pulse transformer is applied to the cathode of the SCR. The capacitor is charged to only about 1 V and can be considered a short circuit for the duration of commutation.

Q.5 a. Draw a neat diagram for Single Phase Full Wave Controlled Bridge Rectifier with a resistive load and explain its operation with the help of waveforms. (10)

Answer:

6.4.1 In Circuits With a Resistive Load

Figure 6.15 shows a full-wave controlled bridge rectifier circuit with a resistive load. In this circuit, diagonally opposite pairs of SCRs turn on and off together. The circuit operation is similar to that of the full-wave center-tap circuit discussed in Section 6.3. The average DC output voltage can be controlled from zero to its maximum positive value by varying the firing angle. The average value of the DC voltage is

$$V_{o(avg)} = \frac{V_m(1+\cos\alpha)}{\pi} \qquad 6.13$$

and

$$I_{RMS} = \frac{I_m}{\sqrt{2}}\sqrt{1-\frac{\alpha}{\pi}+\frac{\sin 2\alpha}{2\pi}} \qquad 6.14$$

The SCRs are controlled and fire in pairs with a delay angle of α. The current and voltage waveforms become full-wave, as shown in Figure 6.16.

Figure 6.15
Full-wave bridge rectifier circuit

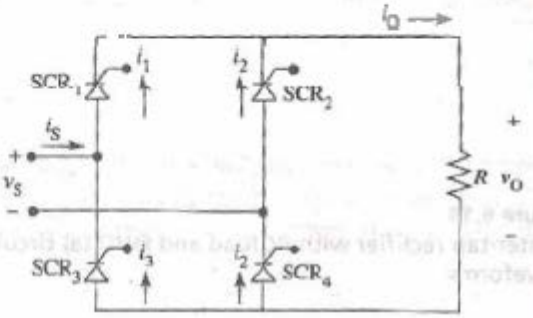
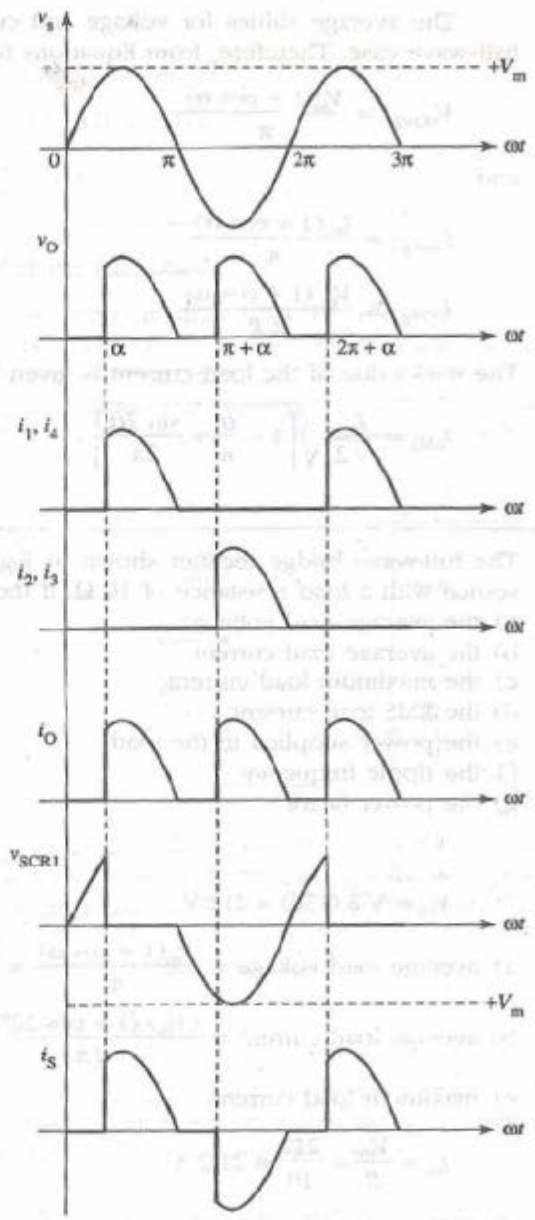


Figure 6.16
Waveforms of the bridge rectifier with a resistive load



The average values for voltage and current are again twice those of the half-wave case. Therefore, from Equations 6.1 and 6.2,

$$V_{o(avg.)} = \frac{V_m(1 + \cos \alpha)}{\pi} \qquad 6.15$$

and

$$I_{o(avg.)} = \frac{I_m (1 + \cos \alpha)}{\pi}$$

$$I_{o(avg.)} = \frac{V_m (1 + \cos \alpha)}{\pi R} \qquad 6.16$$

The RMS value of the load current is given by

$$I_{RMS} = \frac{I_m}{\sqrt{2}} \sqrt{\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]} \qquad 6.17$$

b. A single phase half wave controlled rectifier connected to a 150 V, 60 Hz source to supplying a resistive load of 10 Ω. If the delay angle α is 30°, then find:

(i) the maximum load current

(ii) the average load current (6)

Answer:

Given Data: VS = 150 V, f = 60 Hz, Resistive Load (R) = 10 Ω and Delay Angle (α) = 30°

Peak Load Voltage = $V_m = \sqrt{2}\ V_S$ = 1.414 X 150 = 212 V.

(i) Maximum Load Current (I_m) = $\frac{V_m}{R} = \frac{212}{10} = 21.2A$

(ii) Average Load Current = $\frac{(I_m)(1+\cos\alpha)}{2\pi} = \frac{(21.2)(1+\cos 30^\circ)}{2\pi} = 6.3A$

Q.6 a. Draw a neat diagram for Three Phase Half Wave Controlled Rectifier circuit with a resistive load and explain its operation with waveforms. (10)

Answer:

7.2.1 With a Resistive Load

A basic three-phase half-wave rectifier consisting of three diodes and a resistive load is shown in Figure 7.1. The circuit can be analyzed by first determining the periods in which each diode is on and then applying the appropriate source voltage across the load resistor *R*. Each diode conducts for 120° intervals in the sequence D_1, D_2, D_3, . . . to give the combined output voltage v_o shown in Figure 7.2.

At any given time, the most positive instantaneous voltage turns its respective diode on. The on diode connects its most positive source terminal to the other two diode cathodes, keeping the other two diodes off. Therefore, only one diode is on at any time (ignoring the moment of switching). The sudden switchover from one diode to another is called *commutation*.

The input voltage waveform v_s in Figure 7.2 is used to find the periods when each diode is on. Consider the interval between 0° and 30°. During this time, the phase voltage v_{CN} is higher than both v_{AN} and v_{BN}. As a result, diode D_3 is forward-biased and the output voltage (v_o) becomes equal to v_{CN}. During

Figure 7.1
Three-phase half-wave rectifier circuit diagram

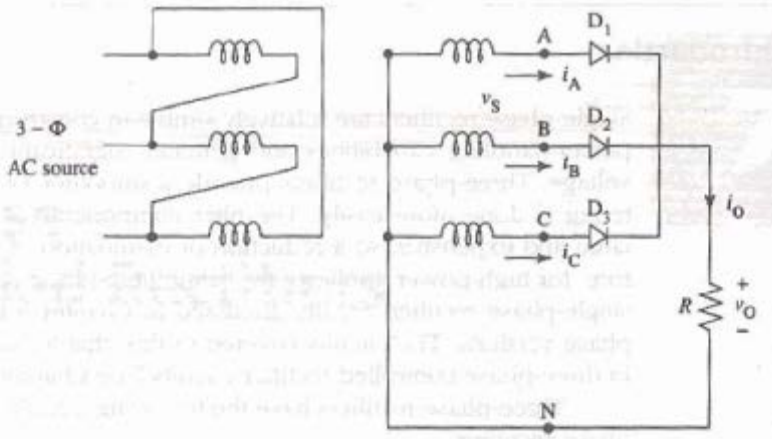
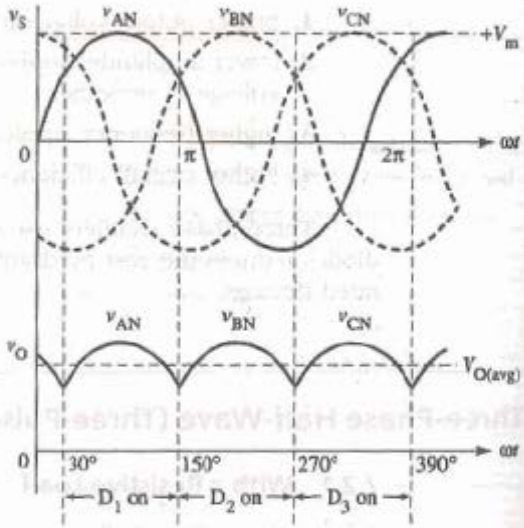


Figure 7.2
Load voltage waveforms



this interval, the voltage across D_1 is v_{AC} and that across D_2 is v_{BC}. Diodes D_2 and D_3 are therefore reverse-biased. From 30° to 150°, the most positive voltage is v_{AN}; it turns diode D_1 on and appears across R as v_o. At 150°, the instantaneous voltage of v_{BN} becomes greater than v_{AN}. Diode D_1 becomes reverse-biased and turns off as diode D_2 becomes forward-biased and begin to conduct. This applies v_{BN} across R from 150° to 270°. At 270°, v_{CN} again becomes the most positive and D_3 turns on. Diode D_3 connects v_{CN} across R from 270°. The cycle is then repeated.

The output voltage across the load v_o follows the peaks of the input supply voltage and pulsates between V_{max} and 0.5 V_{max}. This circuit is called a three-pulse rectifier, since the output repeats itself three times in every cycle of v_s. The ripple voltage is smaller than that produced by a single-phase rectifier. The ripple frequency (f_r) of the output voltage is

$$f_r = n f_s \qquad 7.1$$

where

n = pulse number or number of diodes = 3

and

f_S = AC supply frequency

Therefore,

$f_r = 3 * 60 = 180$ Hz

Filtering is thus easier since the size of the filter is reduced as the ripple frequency increases.

A general expression for the average load voltage is

$$V_{o(avg.)} = \frac{n}{\pi} V_m \sin\left(\frac{\pi}{n}\right) \quad 7.2$$

For the case of a three-pulse rectifier,

$$V_{o(avg.)} = 0.827\ V_m \quad 7.3$$

In terms of line voltage, average load voltage is given by

$$V_{o(avg.)} = 0.477\ V_{L(m)} \quad 7.4$$

where,

V_m = maximum value of phase voltage

$V_{L(m)}$ = maximum value of line voltage

Because the load is resistive, the load current has the same waveform as the load voltage. The individual diode currents are equal to the load current during the time when a particular diode conducts for its 120° interval. Each diode current is then zero for a 240° interval (see Figure 7.3).

In general, each diode conducts for a period of $\frac{2\pi}{n}$.

The average load current is given by

$$I_{o(avg.)} = \frac{n}{\pi} I_m \sin\left(\frac{\pi}{n}\right) \quad 7.5$$

$$= 0.827\ I_m \quad 7.6$$

where

$I_m = V_m/R$

The average current in each diode is only one-third the load current:

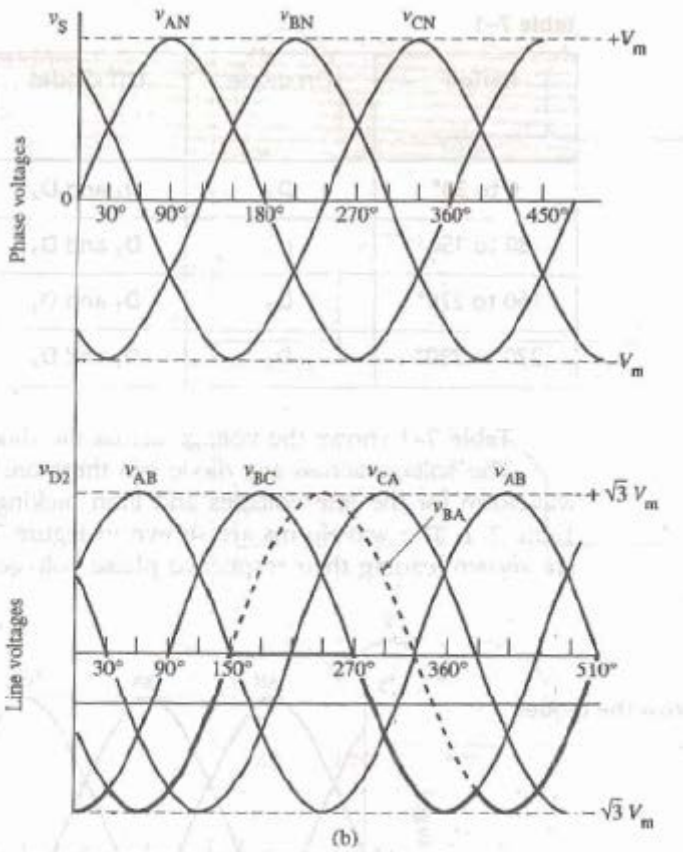
$$I_{D(avg.)} = I_{o(avg.)}/n = I_{o(avg.)}/3 \quad 7.7$$

The maximum load current and maximum diode current are obviously the same, and because the load is resistive,

$$I_{o(m)} = \frac{V_m}{R}$$

$$= 1.21\ I_{o(avg.)} \quad 7.8$$

Figure 7.4
Voltage across the diodes
(b) v_{D2}



The PIV rating for the diodes should be

PIV rating $\geq V_{L(m)}$ or $\sqrt{6}\,V_{s(m)}$.

b. A six pulse half controlled bridge rectifier is connected to a three phase 220 V AC source. Calculate the firing angle if the terminal voltage of the rectifier is 240 V. What is the maximum value of the DC output voltage? (6)

Answer:

Given that the terminal voltage of the rectifier ($V_{o(avg.)}$) = 240 V and the source voltage $V_{L(S)}$ = 220 V

Therefore, the maximum voltage ($V_{L(m)}$) = $\sqrt{2}\,(V_{L(S)})$ = $\sqrt{2}\,(220V)$ = 311 V.

(i) The formula for finding of Firing Angle (α) is $(V_{O(avg.)}) = \frac{3}{2\pi} V_{L(m)}(1+\cos\alpha)$

Hence $(1+\cos\alpha) = \frac{V_{O(avg.)}\,2\pi}{3.V_{L(m)}} = \frac{240VX\,2\pi}{3X\,311V} = 1.62$

So that $(\cos\alpha) = 0.62$

Therefore, the Firing Angle $(\alpha) = 52^\circ$

(ii) Maximum value of DC output voltage is obtained with $(\alpha = 0^\circ)$ is given by

$$V_{O(\max)} = \frac{3}{2\pi}\left(V_{L(m)}\right)(1+\cos\alpha) = \frac{3}{2\pi}(311)(1+1) = 297V$$

Q.7 a. What is a DC Chopper? Explain its principle with the help of suitable diagram and waveforms. What are its various industrial applications? (8)

Answer:

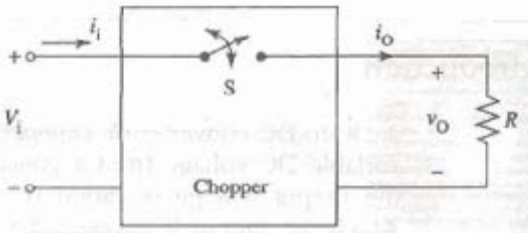
The fundamental principle of a basic chopper is illustrated in Figure 9.1. A switch is connected in series with the DC voltage source (V_i) and the load. The switch S can be a power transistor, an SCR, or a GTO thyristor. It is assumed throughout this chapter that the switching devices are ideal. Ideal switches have the following characteristics:

1. They have zero resistance (zero voltage drop) when on.
2. They have infinite resistance (zero leakage current) when off.
3. They can switch from either state in zero time.

Ideally, the power loss in the chopper is zero, so the output power is equal to the input power:

$$V_o I_o = V_i I_i \qquad 9.1$$

Figure 9.1
Basic DC chopper



V_o = average output voltage
V_i = input voltage
I_o = average output current
I_i = average input current

We assume that the output voltage is adjustable in a certain range from zero to the input level. Let us operate the switch so that it is on (closed) for a time T_{ON} and off (open) for a time T_{OFF} in each cycle with a fixed period T. The resulting output voltage waveform (shown in Figure 9.2) is a train of rectangular pulses of duration T_{ON}.

Figure 9.2
Waveform of v_0 for Figure 9.1

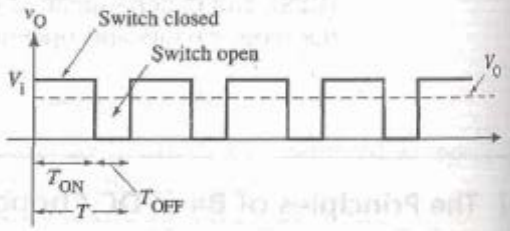


Figure 9.2 shows that the instantaneous voltage across the load is either zero (S off) or V_i (S on). The average (DC) output voltage over a cycle is given by

$$V_o = \frac{T_{ON}}{T_{ON} + T_{OFF}} V_i$$

$$V_o = \frac{T_{ON}}{T} V_i$$

where T is the period ($T_{ON} + T_{OFF}$). The chopper switching frequency is $f =$

If we use the idea of duty cycle (d), which is the ratio of the pulse width T_{ON} to the period of the waveform,

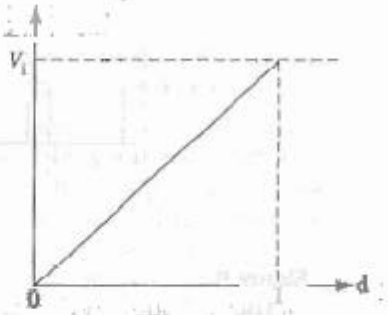
$$d = \frac{T_{ON}}{T}$$

then

$$V_o = d\,V_i \qquad 9.4$$

From Equation 9.4, it is obvious that the output voltage varies linearly with the duty cycle. Figure 9.3 shows the output voltage as d varies from zero to one. It is therefore possible to control the output voltage in the range zero to V_i.

Figure 9.3 Output voltage v_0 as a function of duty cycle



If the switch S is a transistor, the base current will control the on and off period of the transistor switch. If the switch is a GTO thyristor, a positive gate pulse will turn it on and a negative gate pulse will turn it off. If the switch is an SCR, a commutation circuit is required to turn it off.

The load current waveform is similar to Figure 9.2, and its average value is given by

$$I_o = \frac{V_o}{R} = \frac{d\,V_i}{R} \qquad 9.5$$

The effective (RMS) value of the output voltage is

$$V_{o(RMS)} = \sqrt{\frac{V_i^2\,T_{ON}}{T}} = V_i\sqrt{\frac{T_{ON}}{T}} = V_i\sqrt{d} \qquad 9.6$$

The average output voltage can be varied in one of the following ways:

1. **Pulse-width modulation** (PWM). In this method, the pulse width T_{ON} is varied while the overall switching period T is kept constant. Figure 9.4 shows how the output waveforms vary as the duty cycle is increased.
2. **Pulse frequency modulation** (PFM). In this method, T_{ON} is kept constant while the period (frequency) is varied. As shown in Figure 9.5, the output voltage reduces as frequency is decreased, being high at higher frequencies.

Figure 9.4
Output voltage waveforms with fixed switching frequency

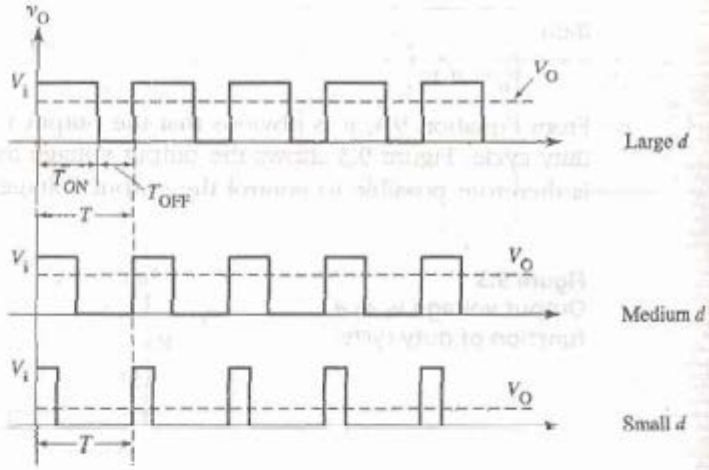
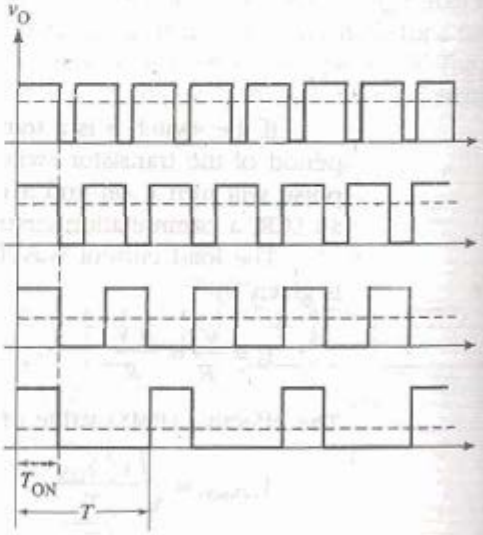


Figure 9.5
Output voltage waveforms with variable switching frequency



For either PWM or PFM control, the output voltage is zero when switch S is open, and it is equal to the input voltage when the switch is closed for a time longer than the normal switching cycle.

In the PFM method, it is necessary to reduce the chopper switching frequency to obtain a lower output voltage. This may result in discontinuity at low frequencies. Moreover, a reduction in frequency increases the output current ripple, thereby Increasing losses and hearing in the load. On the other hand, h e losses in the components become very high at higher frequencies. The PWM method has the advantage of low ripple, which means smaller filter components.

b. What is a Buck-Boost Chopper? Draw its circuit configuration and explain its working with the help of voltage and current waveforms. (8)

Answer:

9.5 Buck-Boost Choppers

A buck-boost DC-to-DC chopper circuit combines the concepts of the step-up and step-down choppers. The output voltage can be either higher than, equal to, or lower than the input voltage. A reversal of the output voltage polarity may also occur. The circuit configuration is shown in Figure 9.18(a). The switch can

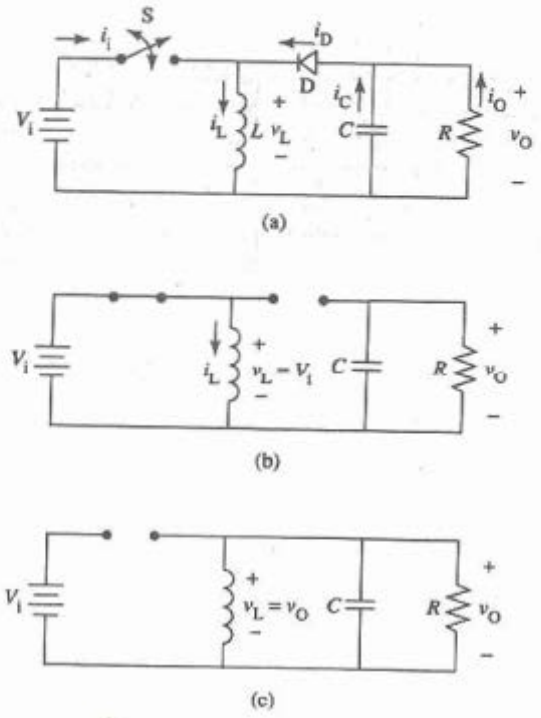


Figure 9.18
(a) Buck-boost DC chopper
(b) equivalent circuit with switch on (c) equivalent circuit with switch off

be any type of controlled switching device such as a power transistor, a GTO thyristor, or an IGBT.

When S is on, the diode D is reverse-biased and i_D is zero. The circuit can be simplified as shown in Figure 9.18(b). The voltage across the inductor is equal to the input voltage, and the current through the inductor i_L increases linearly with time. When S is off, the source is disconnected. The current through the inductor cannot change instantly, so it forward-biases the diode and provides a path for the load current. The output voltage becomes equal to the inductor voltage. The circuit can be simplified as shown in Figure 9.18(c). The voltage and current waveforms are shown in Figure 9.19.

With the switch *on* (T_{ON}),

$$W_{ON} = V_i I_i T_{ON}$$

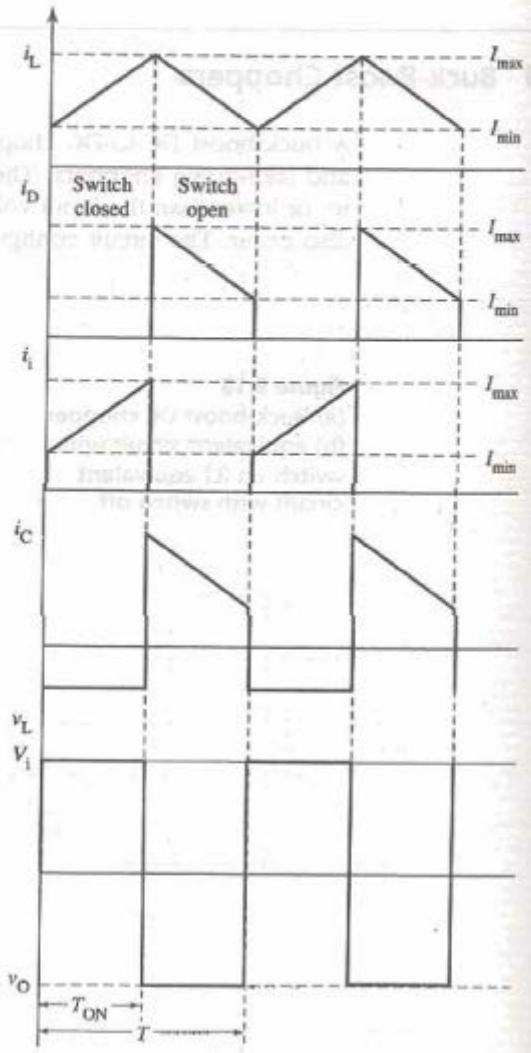


Figure 9.19 Voltage and current waveforms for buck-boost chopper

With the switch off (T_{OFF})

$$W_{OFF} = V_o I_i T_{OFF}$$

Ignoring losses,

$$W_{ON} = W_{OFF}$$

$$V_i I_i T_{ON} = V_o I_i T_{OFF}$$

or $$V_o = V_i \frac{T_{ON}}{T_{OFF}}$$

Now, $$d = \frac{T_{ON}}{T}$$

$$T_{ON} = d\,T$$

and $$T = T_{ON} + T_{OFF}$$

$$T_{OFF} = T - T_{ON}$$

$$= T\left(1 - \frac{T_{ON}}{T}\right)$$

$$= T(1 - d)$$

Substituting in V_o,

$$V_o = V_i \frac{d\,T}{(1 - d)\,T}$$

$$V_o = \frac{d}{1 - d} V_i \qquad \textbf{9.28}$$

The output voltage can be controlled by changing the duty cycle d. Depending on the value of d, the output voltage can be higher than, equal to, or lower than the input voltage. When $d > 0.5$, the output voltage is greater than the input voltage and the circuit operates in the step-up mode. If $d < 0.5$, the output voltage is less than the input voltage and the circuit acts like a step-down chopper. The buck-boost chopper can transfer from operating in the step-down mode to operating in the step-up mode very smoothly and quickly by changing only the control signals for switch S.

Now, from Equation 9.7,

$$I_L = \frac{I_{max} + I_{min}}{2}$$

$$I_i = I_L\, d = \left(\frac{I_{max} + I_{min}}{2}\right) d$$

The average power input is

$$P_i = V_i * I_i$$

$$= \left(\frac{I_{max} + I_{min}}{2}\right) d\, V_i$$

The output power is

$$P_o = \frac{V_o^2}{R}$$

If we neglect power losses, the power input must equal the power output:

$$\left(\frac{I_{max} + I_{min}}{2}\right) d\, V_i = \frac{V_o^2}{R}$$

$$I_{max} + I_{min} = \frac{2\, V_o^2}{R\, d\, V_i}$$

Substituting V_o from Equation 9.28,

$$I_{max} + I_{min} = \frac{2\, d^2\, V_i^2}{R\, d\, (1-d)^2\, V_i} = \frac{2\, d\, V_i}{R(1-d)^2} \qquad 9.29$$

with the switch closed (T_{ON}),

$$\Delta I_L = \frac{V_i}{L} T_{ON}$$

or $$I_{max} - I_{min} = \frac{V_i}{L} T_{ON} = \frac{V_i}{L} d\, T \qquad 9.30$$

Adding Equations 9.29 and 9.30,

$$2\, I_{max} = \frac{2\, d\, V_i}{R(1-d)^2} + \frac{V_i}{L} d\, T$$

$$I_{max} = V_i \left[\frac{1}{R(1-d)^2} + \frac{T}{2\, L}\right] d \qquad 9.31$$

Similarly, I_{min} is given by

$$I_{min} = V_i \left[\frac{1}{R(1-d)^2} - \frac{T}{2\, L}\right] d \qquad 9.32$$

The peak-to-peak ripple in the input current I_i is given by

$$I_{p\text{-}p} = I_{max} - I_{min} = \frac{V_i T\, d}{L} \qquad 9.33$$

For continuous current conditions, the minimum value of the inductance required is obtained by setting Equation 9.32 equal to zero:

$$I_{min} = 0 = V_i \left[\frac{1}{R(1-d)^2} - \frac{T}{2\, L}\right] d$$

$$\frac{1}{R(1-d)^2} = \frac{T\, d}{2\, L}$$

Solving for L,

$$L = \frac{R\, T\, d\, (1-d)^2}{2} \qquad 9.34$$

Q.8 a. Explain the working of a full bridge VSI with a neat circuit diagram and waveforms. (8)

Answer:

10.3.2.1 With a Resistive Load

A full-bridge VSI can be constructed by combining two half-bridge VSIs. Figure 10.5 shows the basic circuit for a single-phase full-bridge voltage source inverter. Four switches and four freewheeling diodes are required. The amplitude of the output voltage and therefore the output power are twice that of the half bridge. The switches are turned on and off in diagonal pairs, so either switches S_1 and S_4 or S_2 and S_3 are turned on for a half-cycle ($T/2$). Therefore, the DC source is connected to the load alternately in opposite directions. The output frequency is controlled by the rate at which the switches open and close. If the pairs of switches are turned on at equal intervals, the output voltage waveform will be

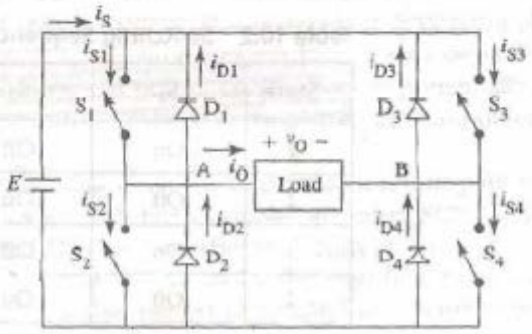


Figure 10.5
Full-bridge voltage source inverter

a square wave with a peak amplitude of E, as shown in Figure 10.6(a). The switching sequence is given in Table 10.2.

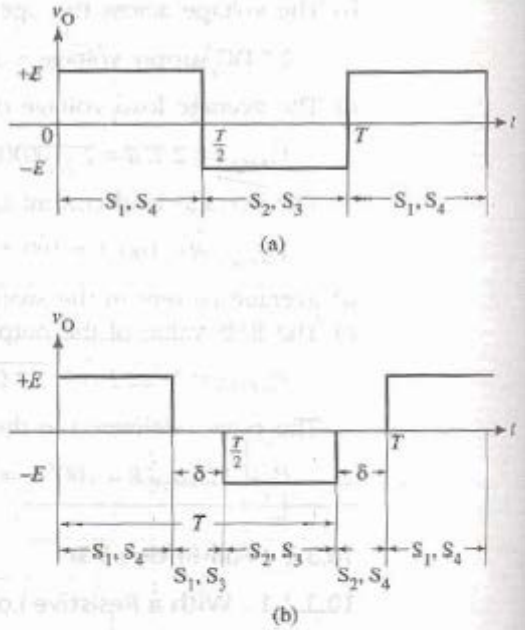


Figure 10.6
Switching sequence and output voltage waveform for the bridge inverter
(a) squarewave output
(b) step-wave output

Comparing the waveforms of Figure 10.6(a) and 10.3(b) shows that the output voltage waveforms of the half-bridge and full bridge inverter are identical. Therefore, the same equations apply.

When the switching state is changed while going from one state to the other, both pairs of switches must be in the off state for a short time to avoid the possibility of short-circuiting the DC source in the transient state in which the switches can be simultaneously closing. Therefore, switching from the on state to the off must be done as quickly as possible, while the switching from off to on must be carried out with an appropriate delay and take a definite time.

Table 10.2 Switching Sequence for a Squarewave Output

State	S_1	S_2	S_3	S_4	Output Voltage
1	On	Off	Off	On	$+E$
2	Off	On	On	Off	$-E$
3	On	Off	Off	On	E
4	Off	On	On	Off	$-E$

Table 10.3 Switching Sequence for a Step-Wave Output

State	S_1	S_2	S_3	S_4	Output Voltage
1	On	Off	Off	On	$+E$
2	On	Off	Off	On	$+E$
3	On	Off	On	Off	0
4	Off	On	On	Off	$-E$
5	Off	On	On	Off	$-E$
6	Off	On	Off	On	0
7	On	Off	Off	On	$+E$
8	On	Off	Off	On	$+E$

We can control the AC voltage by using a third switch state during which the output voltage is zero. The output waveform is the step wave shown in Figure 10.6(b). In the third switch state, switches S_1 and S_3 or S_2 and S_4 close for a time δ, during which $v_o = 0$. The switching sequence is given in Table 10.3.

The average value of the output voltage is given by

$$V_{o(avg.)} = E\frac{(T/2)-\delta}{T/2} = E\left(1-\frac{\delta}{T/2}\right) = E\left(1-\frac{2\delta}{T}\right) \qquad \textbf{10.8}$$

The RMS value of the output voltage is given by

$$V_{o(R.M.S.)} = E\sqrt{1-\frac{2\delta}{T}}$$

Therefore, the magnitude of the output voltage may be controlled somewhat by delaying the turn-on of the appropriate pair of switches after the conducting pair has been turned off.

b. What are the most commonly used methods of pulse width modulation? Explain multiple pulse width modulation with the help of waveforms when the number of pulses (m) = 2 and 3. (8)

Answer:

10.5 Pulse-Width Modulation (PWM)

The three most commonly used methods for pulse-width modulation fall into the following groups:

1. Single pulse-width modulation
2. Multiple pulse-width modulation
3. Sinusoidal pulse-width modulation

10.5.1 Single Pulse-Width Modulation

In this method of voltage control, the output voltage waveform consists of a single pulse in each half-cycle of the required output voltage. For a given frequency ($f = 1/T$), the pulse width t_w can be varied to control the AC output voltage. The output voltage waveform of a single-phase bridge inverter (see Figure 10.5) without modulation is shown in Figure 10.11(a). Here switches S_1 and S_4 are on for one half-cycle and S_2 and S_3 are on for the other half-cycle to give maximum output voltage.

Voltage control is achieved by varying the phase of S_3 and S_4 with respect to S_1 and S_2. Figure 10.11(b) shows the output voltage waveform when the conduction interval of S_3 and S_4 is advanced by an angle $\delta = 90°$. The output voltage is [illegible] by [illegible] square-wave voltages, which are in phase with respect to each other. The output voltage consists of alternating pulses with a pulse width of $(180° - \delta) = 90°$.

The output voltage can be smoothly adjusted from its maximum (0° delay) to zero (low delay) by either phase-advancing or -delaying the turn-on of one pair of switches with respect to the other.

10.5.2 Multiple Pulse-Width Modulation

Instead of reducing the pulse width to control the output voltage, the output of the inverter can be switched on and off rapidly several times during each half-cycle to produce a train of constant magnitude pulses.

Figure 10.12 shows the idea of multiple pulse-width modulation. The output voltage waveform consists of m pulses for each half-cycle of the required output voltage. If f is the output frequency of the inverter, the frequency of the pulses (f_p) is given by

$$f_p = 2 f m$$

Therefore, the number of pulses per cycle is

$$2m = f_p / f$$

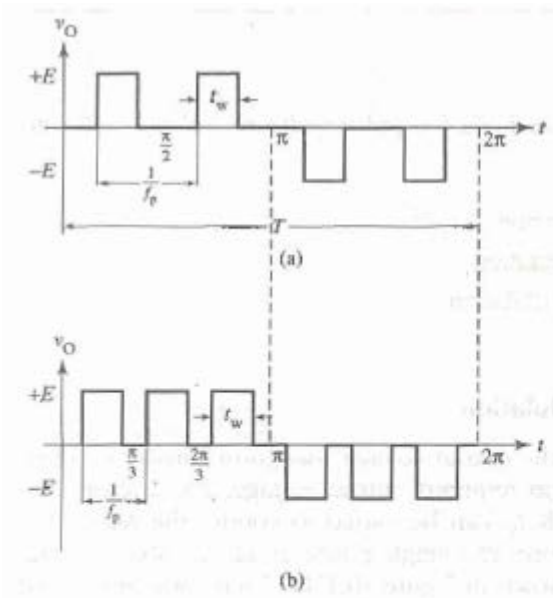


Figure 10.12
Multiple pulse-width modulation waveforms
(a) $m = 2$ (b) $m = 3$

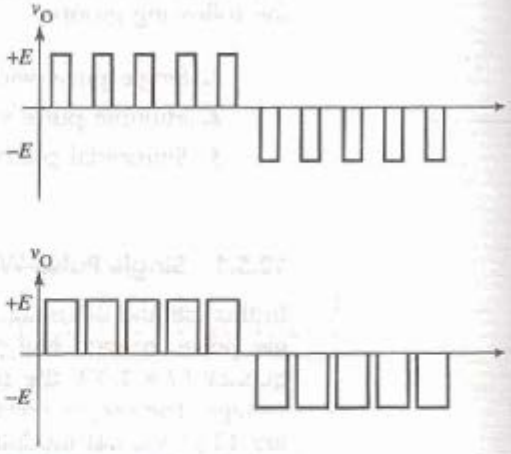


Figure 10.13
Variable duty cycle with fixed $m = 5$

Figure 10.12(a) shows the output voltage waveform for $m = 2$. The pulse width t_w should be less than $\pi/2$. In Figure 10.12(b), for $m = 3$, it is clear that $t_w < \pi/3$. In general, the pulse width $t_w \leq \pi/m$.

An alternative approach for controlling the magnitude of the output voltage is to keep m constant and vary the pulse width t_w (see Figure 10.13).

Q.9 a. What do you mean by AC power control? Discuss the differences between integral cycle control and AC phase control. (8)

Answer:

11.2 AC Power Control

There are two basic methods for controlling the load power: *integral cycle control* or *on-off control* and *phase control*. The first method is suitable for systems with a large time constant, such as a temperature control system. The load power can be controlled by connecting the source to the load for a few complete cycles then disconnecting the source from the load for another number of cycles, and repeating the switching cycle. The relative duration of the on and off periods, i.e., the duty cycle d, is adjusted so that the average power delivered to the load meets some particular objective. Figure 11.2 shows a typical pattern. In ideal circumstances, the average power to the load can be controlled from 0% through 100%.

11.3 Integral Cycle Control

In the AC voltage controller in Figure 11.1, the thyristors can be fired at $\alpha = 0°$ to allow complete cycles of source voltage to be applied to the load. If there is no firing signal in any cycle, then no voltage appears across the load. Thus it is possible to allow complete cycles of source voltage to be applied to the load followed by complete cycles of extinction. If the load voltage is turned on and off in this manner (Figure 11.2), the average power to the load can be varied. The ratio of on time to total cycle time (the period in which the conduction pattern repeats) controls the average load power. In Figure 11.2, T_{ON} is the number of cycles for which the load is energized and T is the number of cycles in the full period of operation. During the T_{ON} part of the cycle, the switch is on and the load power is maximum. During the remaining T_{OFF} ($T_{OFF} = T - T_{ON}$) cycles, the switch is off and the load power is zero.

For a resistive load R, the average load power is given by

$$P_{o(avg)} = \frac{V_i^2 T_{ON}}{R T} = \frac{V_i^2}{R} d = P_{o(max)} d \qquad \textbf{11.1}$$

The RMS value of the output voltage is given by

$$V_o = \frac{V_m}{\sqrt{2}} \sqrt{\frac{T_{ON}}{T}} = V_i \sqrt{d} \qquad \textbf{11.2}$$

where

V_m = maximum value of input voltage

V_i = RMS value of input voltage = $V_m/\sqrt{2}$

Because T_{ON} can be varied only as an integer, the average value of the load power is not a continuous function but has only discrete levels. The number of steps available for regulating the average power depends on the total number of cycles included in the repeat pattern.

Power conversion is the ratio of the average power output ($P_{o(avg.)}$) to the maximum possible power output ($P_{o(max)}$). $P_{o(avg.)}/P_{o(max)}$ is equal to the duty cycled

$$d = T_{ON}/(T_{ON} + T_{OFF}) = T_{ON}/T$$

where

T = time period = $T_{ON} + T_{OFF}$

The source current is always in time phase with the source voltage. However, this does not mean that an integral cycle control circuit operates at unity power factor—for part of the time, the source current is not present at all and therefore is not in phase with the source voltage.

The power factor is given by

$$PF = \sqrt{T_{ON}/T} = \sqrt{d} \qquad 11.3$$

It is clear from Equation 11.3 that a power factor of one will result when $T_{ON} = T$, which would result in sinusoidal operation.

A closed-loop control system can be used to vary the value of T_{ON} to maintain some variable close to a selected set point. Such a system would depend on sufficient energy storage in the controlled system to smooth variations that result from the on-off nature of the control. Integral cycle control has the advantage of fewer switching operations and low radio frequency interference (RFI) due to control during the zero crossing of the AC voltage, that is, in this method, switching occurs only at zero voltage for resistive loads. The rate of change of the load current depends on the system frequency, which is small, so there is low electrical noise compared with other control methods.

11.4 AC Phase Control

11.4.1 In Circuits with a Resistive Load

The basic circuit in Figure 11.1 can be used to control the power to a resistive load. As is done with a controlled rectifier, output voltage is varied by delaying conduction during each half-cycle by an angle α. The delay angle α is measured from the source voltage zero.

SCR_1, which is forward-biased during the positive half-cycle, is turned on at an angle α. It conducts from α to π, supplying power to the load. SCR_2 is turned on half a cycle later at $\pi + \alpha$. It conducts up to 2π, supplying power to the load. The waveforms in Figure 11.3 are identical to those of a full-wave rectifier with a resistive load. The difference here is that each second half-cycle has a negative current rather than a positive one. There is, however, no effect on the power, because power is a squared function.

The equation for the RMS value of the output voltage is

$$V_{o(RMS)} = V_i \left\{ 1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi} \right\}^{1/2} \qquad 11.4$$

The equation for the RMS value of the output current with a resistive load is similar to Equation 11.4:

$$I_{o(RMS)} = \frac{V_i}{R} \left\{ 1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi} \right\}^{1/2} \qquad 11.5$$

By varying the delay angle α, the output current of the load can be continuously adjusted between the maximum value of V_i/R at $\alpha = 0$ and zero at $\alpha = 180°$.

The RMS current rating of the triac is given by

$$I_{T(RMS)} = I_{o(RMS)} \qquad 11.6$$

The RMS current rating of the SCRs is given by

$$I_{SCR(RMS)} = I_{o(RMS)}/\sqrt{2} \qquad 11.7$$

Output power is given by

$$P_{o(avg.)} = I^2_{o(RMS)}\,(R) \quad \text{or} \quad V^2_{o(RMS)}/R \qquad 11.8$$

Examination of Equations 11.5 and 11.8 shows that the load power can be varied by changing α over the full range from zero to 180°. Suitable trigger circuits exist to allow conduction to be adjusted essentially over this entire range.

Table 11.1

α (°)	$V_{o(RMS)}$ (V)	$P_{o(avg.)}$ (W)	$P_{o(avg.)}/P_{o(max)}$	$V_{o(RMS)}/V_i$
0	50.0	25.0	1.0	1.0
30	49.3	24.3	0.97	0.98
60	44.8	20.1	0.80	0.89
90	35.4	12.5	0.50	0.71
120	21.9	4.8	0.20	0.44
150	8.5	0.72	0.03	0.17
180	0.0	0.0	0.0	0.0

The **control characteristic** of a single-phase AC power controller can be calculated as a function of the delay angle. If we assume V_i = 50 V and load resistance $R = 100\ \Omega$, then at $\alpha = 0°$, using Equation 11.4, output voltage $V_{o(RMS)} = V_i = 50$ V and

$$P_{o(max)} = V_i^2/R = 50^2/100 = 25\ \text{W}$$

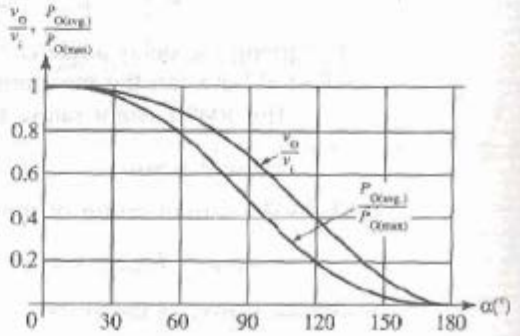
while

$$P_{o(avg.)} = V_{o(RMS)}^2/R$$

Evaluating output voltage and power for successive values of the delay angle gives the results shown in Table 11.1.

The control characteristic, $V_{o(RMS)}/V_i$ and $P_{o(avg.)}/P_{o(max)}$ versus α, for a resistive load is plotted in Figure 11.4.

Figure 11.4
Variation of output voltage and power with delay angle for a resistive load



Because the current is nonsinusoidal, the power factor presented to the AC source is less than unity, although the load is resistive. Whatever the wave-

form, by definition the power factor is given by

$$PF = \frac{\text{active power}}{\text{apparent power}}$$

$$= \frac{P}{V_i I_i}$$

$$= \frac{[V^2_{o(RMS)}/R]}{V_i [V_{o(RMS)}/R]}$$

$$= \frac{V_{o(RMS)}}{V_i}$$

Substituting Equation 11.4, we obtain

$$PF = \left\{1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right\}^{1/2} \qquad 11.9$$

The resulting power factor is unity only when α is zero, it becomes progressively smaller as α increases, becoming approximately zero for $a = \pi$.

The switch current becomes zero just when the source voltage is zero, because the load is resistive. Therefore, when the switch begins blocking at the time of the current zero, negligible source voltage is present. The problem of *du/dt* being large at turnoff does not *exist*, and no snubber is required to reduce the rate of voltage buildup across the device terminals.

For values of $a > 90°$, the switch blocks the peak source voltage before it turns on. The minimum switch voltage capability therefore is the peak value of the source voltage. This blocking capability is of course necessary in both directions for either the SCR or the triac implementation of the switch.

$$PIV \geq V_{i(m)} \qquad 11.10$$

b. Compare the advantages and disadvantages of semiconductor switches over mechanical switches. (8)

Answer:

12.2 Comparison of Semiconductor and Mechanical Switches

A semiconductor switch offers several advantages over other switching devices:

1. *It provides extremely high switching speeds*, because the switch turns on immediately.
2. Operation is quiet because there are no moving parts and no arcing.
3. Radio frequency interference (RFI) is eliminated by using zero voltage
4. No routine maintenance is required because there are no contacts a moving parts that wear.
5. Operational life is much longer.
6. It is completely safe in an explosive environment.
7. Immune from vibration and shock.
8. It can be installed in any position or location.
9. There is no switch contact bounce when closing.
10. It is small and lightweight.
11. It is easily tailored to electronic control.
12. The cost is low,
13. It offers greater reliability.
14. In addition to turning a load on or off, it can also be used to control the load power from zero to maximum.
15. The control circuit can be easily isolated from the power circuit.
16. It is easy to control remotely.

Some of the disadvantages of a semiconductor switch are:

1. Due to reverse leakage current when off, it does not allow the load to be completely isolated from the source.
2. It is likely to fail when subjected to overvoltage and overcurrent situations unless protected by an RC snubber circuit.

3. It has higher power losses in the on-state condition, so cooling is required.
4. The on-state voltage drop across the device may not be permissible in some applications.
5. Due to the higher cost of the device and the complexity of control, its use is normally limited to single-phase circuits.
6. The same switch cannot be used in both AC and DC circuits, since the AC switch turns off naturally while the DC switch needs additional force commutation circuitry to turn it off.
7. Continuous firing pulses are required to maintain the switch in the on state.
8. It can cause false triggering as a result of voltage transients caused by switching inductive loads on neighboring lines.
9. To prevent false triggering, the firing circuits must be completely isolated or shielded from power circuits.
10. Protection circuits are necessary to safely turn off the device before the surge current or fault current ratings are exceeded.
11. Overload capability is limited by the maximum current of the semiconductor device.

Static switches are used in both AC and DC switching operations. AC switching requires bidirectional control, which is usually implemented by using a triac or two SCRs connected in antiparallel. Since the device turns off naturally, the upper frequency limit is determined by the type of device used. For low-frequency switching applications, a single triac can be used. For high-frequency applications a configuration of two antiparallel SCRs is employed. DC switching requires control for only one direction of current flow, and the switching device is usually an SCR. The switching speed is limited by the commutation circuit and the reverse recovery time of the SCR.

DE71 Distribution of Marks

(16)8

MODERATION-I

Q.2 (a) Power loss — 02
Conduction losses diagram – 2
explanation – 4
} 8

(b) over voltage – 3
over current – 3
Transients – 2
} 8

} 16

Q.3 (a) BJT as switch – 2
V–I characteristics – 2
significance — 4
} 8

(b) Calculations 4x2 = 8

} 16

Q.4 (a) necessity — 2
Diagram — 2
Explanation — 5
} 9

(b) Methods — 2
Commutation method – 4
Waveforms — 1
} 7

} 16

Q.5 (a) Diagram — 2
Waveforms — 2
Explanation — 6
} 10

(b) Formulae – 2
Calculations – 4
} 6

} 16

Q.6 (a) Diagram – 3 2
Waveforms – 3 3
Explanation – 5
10
(b) Formulae – 2
Calculation – 4
6
16

Q.7 (a) Definition – 2
Principle – 2
Diagram + waveforms – 2
applications – 2
8
(b) Definition – 1
circuit – 2
Waveforms – 2
explanation – 3
8
16

Q.8 (a) ckt circuit diagram – 2
waveform – 2
explanation – 4
8
(b) Methods – 2
PWM method – 4
waveforms – 2
8
16

Q.9 (a) Definition – 2
Explanation – 6
8
(b) Advantages – 4
Disadvantages – 4
8
16

TEXT BOOK

I. Power Electronics for Technology, First Impression (2006), Ashfaq Ahmed, Purdue University - Calumet, Pearson Education