Q.2 a. With the help of neat diagrams, explain briefly the basic planar process used to fabricate ICs. (12)

Answer:

BASIC PLANAR PROCESS

1.Silicon wafer (Substrate) preparation

2.Epitaxial Growth

3.Oxidation

4.photolithiography

5.Diffusion

6.Ion Implementation

7.Isolation Technique

8.Metallization

9.Assembly Processing and packaging

1.Silicon wafer (Substrate) preparation

The following steps are used in the preparation of Si-wafers

1.crystal growth and doping

2.Ingot trimming and grinding

3.Ingot slicing

4.Wafer polishing and etching

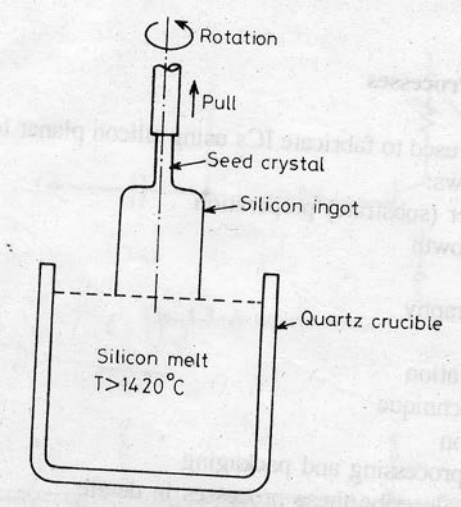
5.Wafer cleaning

The starting material for crystal growth is highly purified (99.9999) polycrystalline silicon. The czochralski crystal growth process is the most oftenused for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant is put in a quartz

Crucible and is then placed in a furnace.the material is then heated to a temperature in excess of the silicon melting point of 1420 degree celsius. A small single crystal rod of silicon called a seed crystal is then dipped into the silicon melt slowly pulled as shown.

As the seed crystal is pulled out of the melt it brings with it a solidified mass of silicon with name crystalline structure as that of seed crystal. During the crystal pulling process the seed

crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross section the diameter of about 10 to 15 cm and ingot length order of 100 cm



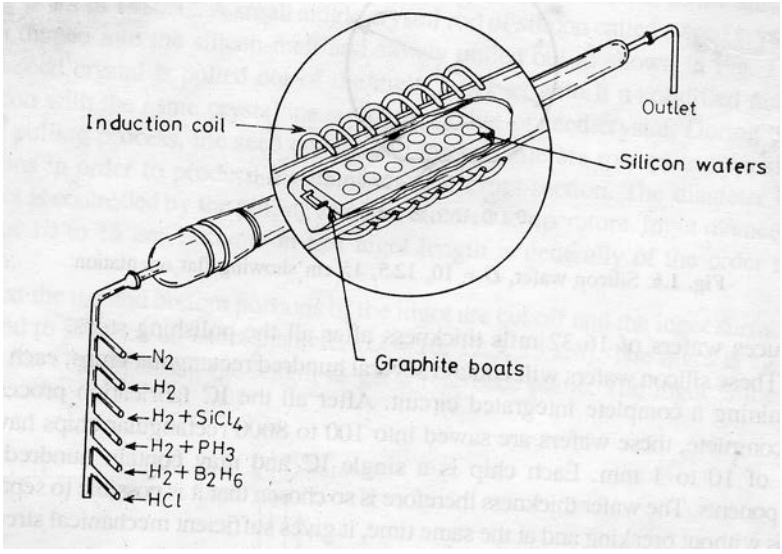
The top an dbottom portions of the ingot are cut off and ingot surface is ground to produce an exact diameter the ingot is also ground flat slightly along the lenth to get referne plane. The ingot is then sliced using a stainless steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circulars wafers or slices.

EPITAXIAL GROWTH

The word epitaxy is derived from greek word epi meaning upon and the past tense of the word teinon meaning arranged . arranging atoms in single crystal fashion upon a sigle crystal substrate so resulting layer is an extenxion of the substate crystal structure.

$SiCl4+2H2 \longrightarrow Si +4Hcl$

OXIDATION



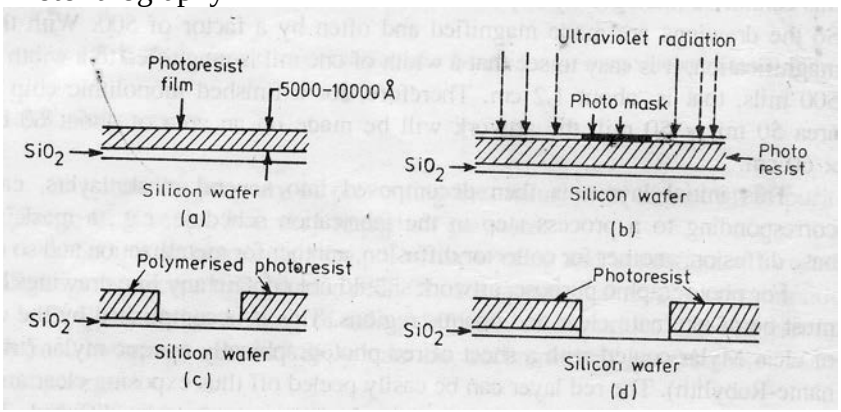
SiO2 has the property of preventing diffusion of almost all impurities through it. It serves very important purposes.

SiO2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid . Thus it stands against any contamination

By selective etching of SiO2 difussion of impurities through carefully defined Windows in the SiO2 can be accomplished to fabricate various components.

$Si + 2H2O \longrightarrow SiO2 + 2H2$

Photolithography



It has become possible to produce microscopically small circuit and device patterns on Si wafers. As many as 10000 transistors can be fabricated on a 1cm * 1cm chip .the conventional photolithographic process uses ultraviolet light exposure and device dimension or line width as small as 2 micrometer can be obtained . With the advent of latest technology using X rays or electron beam lithographic techniques it has become possible to produce device dimension down to submission range <1 micro meter

It involves two process

Making of a photographic mask

Photo etching

First the preparation of initial artwork and secondly its reduction

b. Write a short note on thick film technology. (4)

Answer:

The basic thick film process are

1.Screen Printing

2.Ceramic Firing

Q.3 a. Draw the ac equivalent circuit for common-emitter transistor amplifier with coupling and bypass capacitors and explain the elements used in it. (8)

Answer:

Common-Emitter Circuit

Consider the transistor amplifier circuit shown in Fig. 6-17. When the capacitors are regarded as ac short circuits, it is seen that the circuit input terminals are the transistor base and emitter, and the output terminals are the collector and the emitter. So, the emitter terminal is *common* to both input and output, and the circuit configuration is termed *common-emitter* (CE).

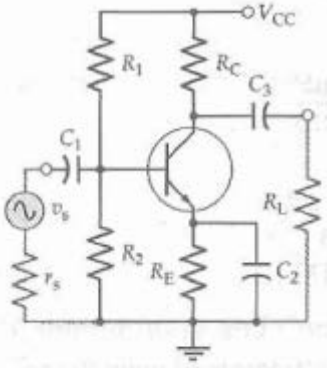


Figure 6-17 Transistor common-emitter amplifier with coupling and bypass capacitors.

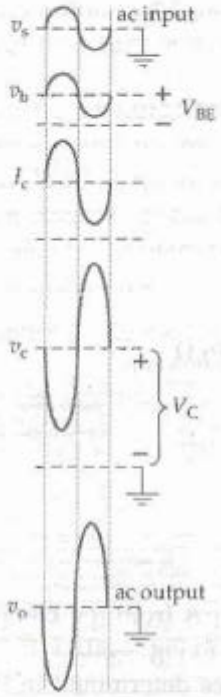


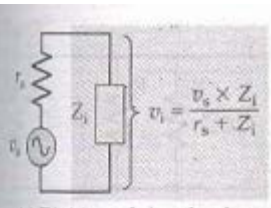
Figure 6-18 Voltage and current waveforms in a common-emitter amplifier.

The current and voltage waveforms for the CE circuit in Fig. 6-17 are illustrated in Fig. 6-18. It is seen that there is a 180° *phase shift* between the input and output waveforms. This can be understood by considering the effect of a positive-going input signal. When v_s increases in a positive direction, it increases the transistor base-emitter voltage (V_{BE}). The increase in V_{BE} raises the level of I_C, thereby increasing the voltage drop across R_C, and thus reducing the level of the collector voltage (V_C). The changing level of V_C is capacitor-coupled to the circuit output to produce the ac output voltage (v_o). As v_s increases in a positive direction, v_o goes in a negative direction, as illustrated. Similarly, when v_s changes in a negative direction, the resultant decrease in V_{BE} reduces the I_C level, thereby reducing V_{RC} and producing a positive-going output.

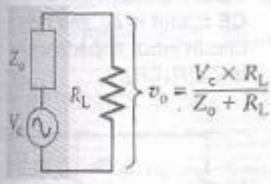
The circuit in Fig. 6-17 has an *input impedance* (Z_i), and an *output impedance* (Z_o). These can cause voltage division of the circuit input and output voltages, as illustrated in Fig. 6-19. So, for most transistor circuits, Z_i and Z_o are important parameters. The circuit voltage amplification (A_v), or *voltage gain*, depends on the transistor parameters and on resistors R_C and R_L.

h-Parameter Equivalent Circuit

The first step in ac analysis of a transistor circuit is to draw the ac equivalent circuit, by substituting short-circuits in place of the power



(a) Division of signal voltage

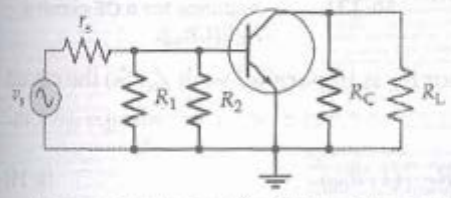


(b) Division of output voltage

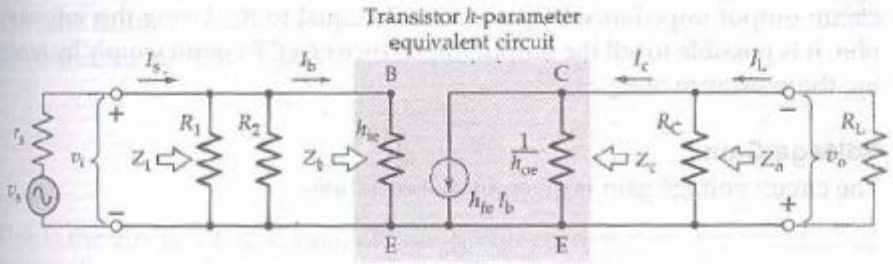
Figure 6-19 Circuit input and output voltages are divided by the effects of Z_i and Z_o.

supply and capacitors. When this is done for the circuit in Fig. 6-17, it gives the ac equivalent circuit shown in Fig. 6-20a (reproduced from Fig. 6-6b). The *h*-parameter circuit is now drawn simply by replacing the transistor in the ac equivalent circuit with its *h*-parameter model (from Fig. 6-12b). This gives the CE *h*-parameter equivalent circuit in Fig. 6-20b. Note that the feedback voltage generator ($h_{re}v_c$) in Fig. 6-12b is omitted in Fig. 6-20b. As discussed, the effect of $h_{re}v_c$ in a CE circuit is unimportant for most practical purposes.

The current directions and voltage polarities in Fig. 6-20b are those that occur when the instantaneous level of the input voltage is moving in a positive direction.



(a) ac equivalent circuit for CE transistor circuit



(b) *h*-parameter equivalent circuit for CE circuit

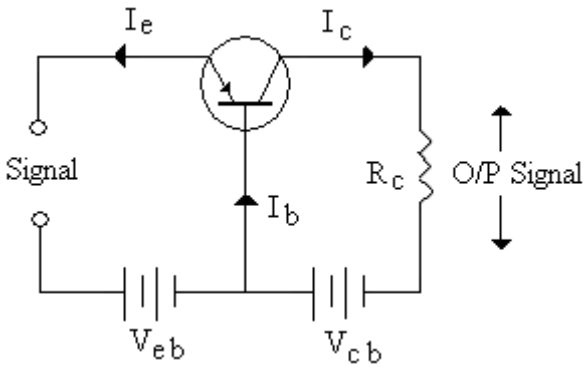
Figure 6-20 A common-emitter *h*-parameter circuit is drawn by first replacing the power supply and all capacitors with short-circuits; then the *h*-parameter model is substituted for the transistor.

b. Compare the characteristics for CC, CE & CB circuit with diagram. (8)

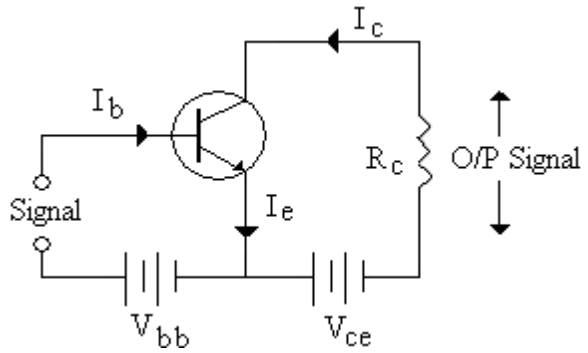
Answer:

A transistor can be connected in a circuit in the following three configurations.

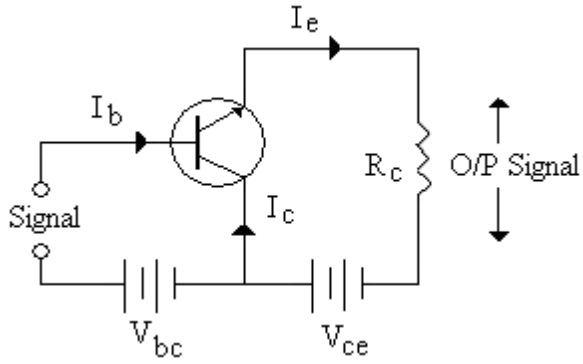
1. Common base configuration



2. Common emitter configuration



3. Common collector configuration



The reasons for wide use of CE configuration are

(i) High current gain: In CE configuration IC is output current and IB is the input current. Collector current is given by IC = ß IB. As the value of ß is very large output current IC is much more than the input current IB. The value of ß is ordinarily high and ranges from 10 to 500.

(ii) High voltage and power gain: Due to high current gain the CE configuration has the highest voltage and power gain of the three transistor configurations.

(iii) Moderate output to input impedance ratio: In the CE configuration the ratio of output impedance to input impedance is small. Therefore this configuration is ideal for coupling between various transistor stages. CE configuration is used for small signal and power amplifier applications.

Q.4 a. Draw typical drain and transfer characteristics for a P-channel JFET and explain. (8)

Answer:

istics for Ex. 9-2.

p-Channel JFET Characteristics

Figure 9-15 shows a circuit for obtaining the characteristics of a *p*-channel JFET. Note the direction of the arrowhead on the FET symbol, and the drain current direction. Note also the supply voltage polarity and the polarity of the gate-source bias voltage. The drain terminal is negative with respect to the source, and the gate terminal is positive with respect to the source. To obtain a table of quantities for plotting a drain characteristic, V_{GS} is maintained constant at the desired (positive) level, $-V_{DS}$ is increased in steps from zero, and the I_D levels are noted at each step.

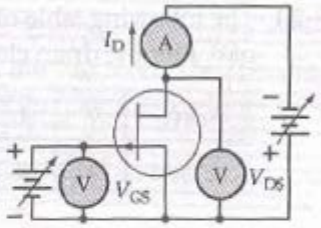


Figure 9-15 Circuit for determining the characteristics of a *p*-channel JFET.

Typical *p*-channel JFET drain characteristics and transfer characteristics are shown in Fig. 9-16. It is seen that these are similar to the characteristics for an

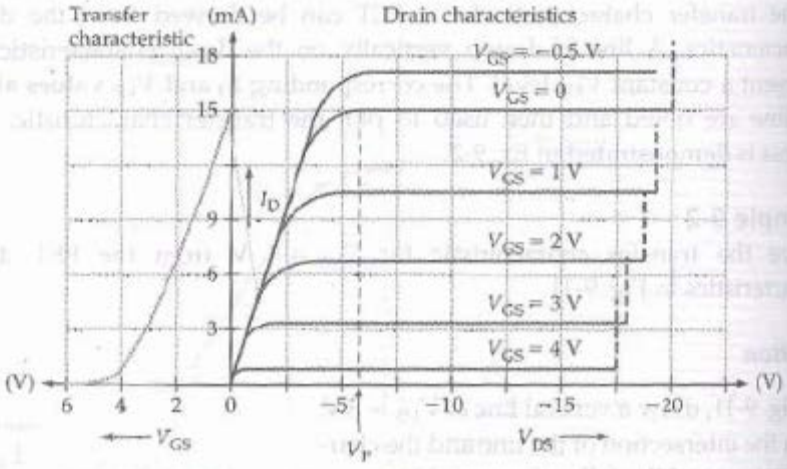


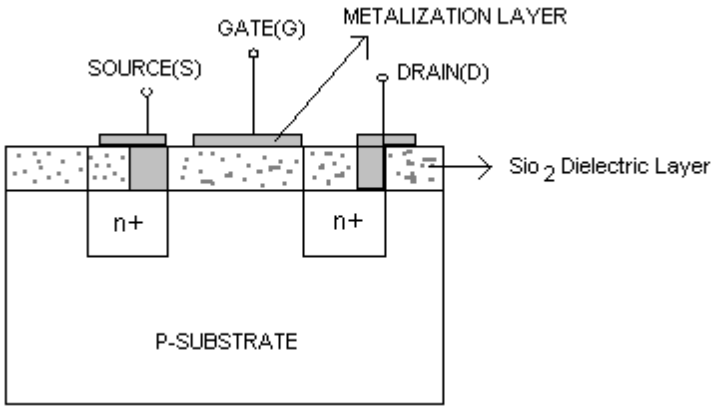
Figure 9-16 Transfer and drain characteristics for a *p*-channel JFET.

n-channel JFET, except for the voltage polarities. In Fig. 9-16, when $V_{GS} = 0$, $I_{DSS} = 15$ mA, and progressively more positive levels of V_{GS} reduce I_D toward cutoff $V_{GS(off)} = +6$ V. Using V_{GS} of -0.5 V produces a higher I_D than when $V_{GS} = 0$. As in the case of the *n*-channel JFET, forward bias at the gate-channel junctions should be avoided; consequently, negative V_{GS} levels are normally not used with a *p*-channel JFET.

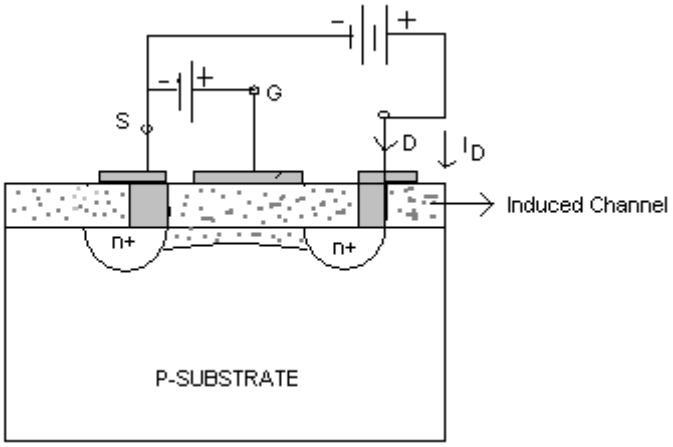
The transfer characteristic for a *p*-channel device can be obtained experimentally or can be derived from the drain characteristics, just as for an *n*-channel FET.

b. Draw a neat sketch to illustrate the structure of a N-channel E-MOSFET and explain its operation. (8)

Answer:



N-Channel E-MOSFET Structure



Operation of N-Channel E-MOSFET

Operation:

It does not conduct when VGS = 0. In enhancement mosfet drain (ID) current flows only when VGS exceeds gate-to-source threshold voltage.When the gate is made positive with respect to the source and the substrate, negative change carriers within the substrate are attracted to the +ve gate and accumulate close to the surface of the substrate. As the gate voltage increased, more and more electrons accumulate under
the gate, these accumulated electrons i.e., minority charge carriers make N-type channel stretching from drain to source.
Now a drain current starts flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends on the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

Q.5 a. Explain the working of transformer coupled class-A power amplifier and derive an expression for its collector efficiency. (9)

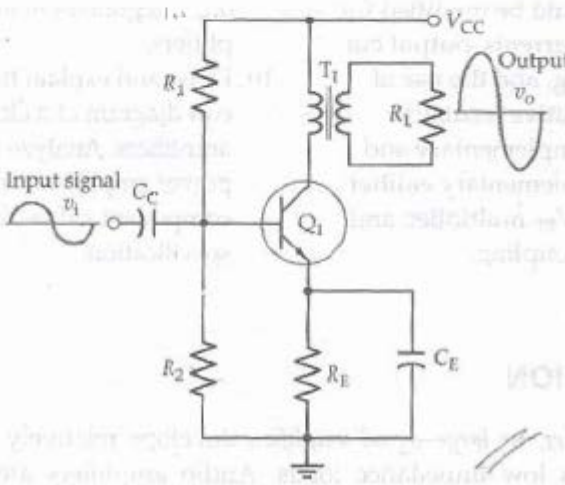
Answer:

Class A Circuit

Instead of capacitor coupling, a transformer may be used to ac-couple amplifier stages while providing dc isolation between stages. The resistance of the transformer windings is normally very small, so that there is no effect on the transistor bias conditions.

Figure 19-1 shows a load resistance (R_L) transformer-coupled to a transistor collector. The low resistance of the transformer primary winding allows any desired level of (dc) collector current to flow, while the transformer core couples all variations in I_C to R_L via the secondary winding. This circuit is a voltage-divider bias circuit in which resistors R_1 and R_2 determine the transistor base voltage (V_B), and resistor R_E sets the emitter current level.

The circuit in Fig. 19-1 is referred to as a *class A amplifier*, which is defined as one that has the Q-point (bias point) approximately at the centre of the ac load line. This enables the circuit to produce maximum equal positive and negative changes in V_{CE}.



Efficiency of a Class A Amplifier

Power is delivered to an amplifier from the dc power supply. The amplifier converts the dc power into ac power supplied to the load (see Fig. 19-6). Some of the input power is

dissipated in the transistor or in other components. This is wasted power. The efficiency (η) of a power amplifier is a measure of how good the amplifier is at converting the dc input (supply) power (P_i) into ac output power (P_o) dissipated in the load.

$$\eta = \frac{P_o}{P_i} \times 100\% \qquad (19\text{-}4)$$

The dc supply power is

$$P_i = V_{CC} \times I_{ave}$$

In the case of a class A amplifier, $I_{ave} = I_{CQ}$

So

$$P_i = V_{CC} \times I_{CQ}$$

Refer again to the class A circuit in Fig. 19-6, and assume that $V_R \ll V_{CC}$. In this case, V_{CEQ} is approximately equal to V_{CC}, and the peak voltage developed across the transformer primary approaches $\pm V_{CC}$ if the transistor is driven to cutoff and saturation. Also, the peak current developed in the transformer windings approaches $\pm I_{CQ}$. Thus, the maximum ac power delivered to the transformer primary can be calculated as follows:

$$P'_o = V_{rms} \times I_{rms} = (V_p/\sqrt{2}) \times (I_p/\sqrt{2})$$

giving

$$P'_o = 0.5\, V_p I_p \qquad (19\text{-}5)$$

Using the highest possible current and voltage, and assuming that the transformer is 100% efficient,

$$P_o = 0.5 V_{CC} I_{CQ}$$

The maximum theoretical efficiency for a class A transformer-coupled power amplifier can now be determined as

Eq. 19-4:

$$\eta = \frac{P_o}{P_i} \times 100\% = \frac{0.5 V_{CC} I_{CQ}}{V_{CC} I_{CQ}} \times 100\%$$

$$= 50\%$$

In a practical class A transformer-coupled power amplifier circuits, 50% efficiency is never approached. Any practical calculation of power amplifier efficiency must take the output transformer efficiency (η_t) into account.

$$\eta_t = \frac{P_o}{P'_o} \times 100\% \qquad (19\text{-}6)$$

b. Explain the working of opto-coupler with the help of a diagram and give its applications. (7)

Answer:

Operation and Construction

An *optocoupler* (*optoelectronic coupler*) is essentially a phototransistor and an LED combined in one package. Figure 21-35 shows the typical circuit and terminal arrangement for one such device contained in a DIP package. When current flows in the LED, the emitted light is directed to the phototransistor, producing current flow in the transistor. The coupler may be operated as a switch, in which case both the LED and the phototransistor are normally *off*. A pulse of current through the LED causes the transistor to be switched *on* for the duration of the pulse. Linear signal coupling is also possible. Because the coupling is optical, there is a high degree of electrical isolation between the input and output terminals, and so the term *optoisolator* is sometimes used. The output (detector) stage has no effect on the input, and the electrical isolation allows a low-voltage dc source to control high-voltage circuits.

The cross-section diagram in Fig. 21-35c illustrates the construction of an optocoupler. The emitter and detector are contained in a transparent insulating material that allows the passage of illumination while maintaining electrical isolation.

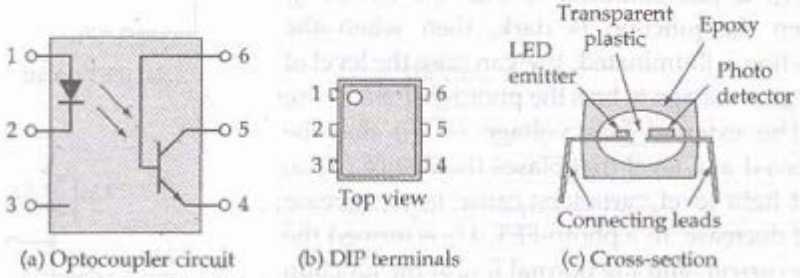


Figure 21-35 An octocoupler is composed of an LED and a phototransistor. The input and output are electrically isolated.

Applications

The circuit of an optocoupler in a dc or pulse-type coupling application is shown in Fig. 21-37. The diode current is switched *on* and *off* by the action of transistor Q_1 operating from a 24 V supply. Transistor Q_2 is turned *on* into saturation when D_1 is energized. The collector current of Q_2 provides the load (*sinking*) current and the current through resistor R_2. *Pull-up* resistor R_2 is necessary to ensure that the load terminal is held at the 5 V supply level when Q_2 is *off*.

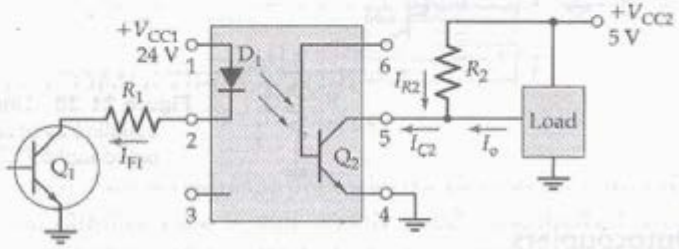


Figure 21-37 Octocoupler used for coupling a signal from a 24 V system to a 5 V system.

Q.6 a. Explain the differential amplifier with the help of suitable diagram. (8)

Answer:

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits (see section 4.3). A typical circuit is shown in Fig. 2.8, Since, the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at the same potential, designated as v_3. The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \qquad (2.25)$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3}{R_2} = 0 \qquad (2.26)$$

Rearranging, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \qquad (2.27)$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_1}{R_1} = 0 \qquad (2.28)$$

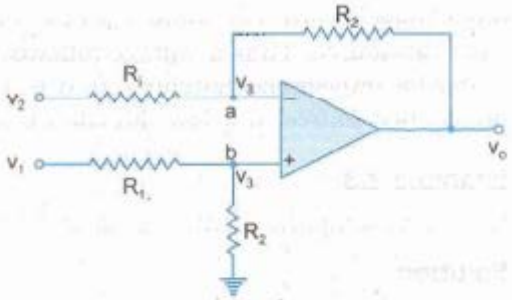


Fig. 2.8 A differential amplifier

Subtracting Eq. (2.28) from (2.27) we get

$$\frac{1}{R_1}(v_1 - v_2) = \frac{V_o}{R_2} \qquad (2.29)$$

Therefore,

$$v_o = \frac{R_2}{R_1}(v_1 - v_2) \qquad (2.30)$$

Such a circuit is very useful in detecting very small differences in signals, since the gain R_2/R_1 can be chosen to be very large. For example, if $R_2 = 100\ R_1$, then a small difference $v_1 - v_2$ is amplified 100 times.

Differem-mode and Common-mode Gains

In Eq. (2.30) if $v_1 = v_2$ then $v_o = 0$. That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-amp, however, a practical op-amp exhibits some small response to the common mode component of the input voltages too. For example, the output v_o will have different value for case (i) with $v_1 = 100\ \mu V$ and $v_2 = 50\ \mu V$ and case (ii) with $v_1 = 1000\ \mu V$ and $v_2 = 950\ \mu V$, even though the difference signal $v_2 - v_2 = 50\ \mu V$ in both the cases, The output voltage depends not only upon the difference signal v_d at the input, but is also affected by the average voltage of the input signals, called the common-mode signal v_{CM} defined as,

$$v_{CM} = \frac{v_1 + v_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch, the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So, even with the same voltage applied to both inputs, the output is not zero. The output, therefore, must be expressed as,

$$v_o = A_1 v_1 + A_2 v_2 \quad (2.31)$$

where, A, (A_2) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since $v_{CM} = (v_1 + v_2)/2$ and $v_d = (v_1 - v_2)$,

$$v_1 = v_{CM} + \frac{1}{2} v_d \quad (2.32)$$

and

$$v_2 = v_{CM} - \frac{1}{2} v_d \quad (2.33)$$

Substituting the value of v_1 and v_2 in Eq. (2.31), we get

$$v_o = A_{DM} v_d + A_{CM} \quad (2.34)$$

where,

$$A_{DM} = \frac{1}{2}(A_1 - A_2) \quad (2.35)$$

and

$$A_{CM} = A_1 + A_2 \quad (2.36)$$

The voltage gain for the difference signal is A_{DM} and that for the common-mode signal is A_{CM}.

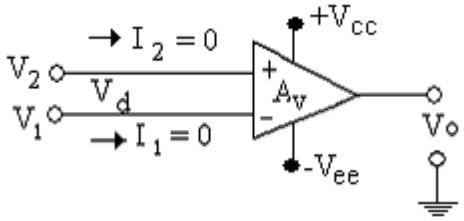
b. Discuss the characteristics of an ideal operational amplifier. (8)

Answer:

The **Fig.** shows the schematic of an ideal op-amp. The following are the important properties of an ideal op-amp.

i) The input impedance of an ideal op-amp is infinite. Hence it draws no current at both theinput terminals.

ii)The gain of an ideal op-amp is infinite (¥), hence the differential input Vd =V1-V2 is zero for the finite output voltage V0



iii) The output voltage V0 is independent of the current drawn from the output terminal. Thus its output impedance is zero.

This results in the following Characteristic of an ideal op-amp.

a) Infinite Voltage gain: It is denoted as AOL. It is the differential open loop gain.

b) Infinite input impedance: It is denoted as Rin and ensures that no current flows into an ideal op-amp.

c) Zero output impedance: It is denoted as Ro and ensures that the output voltage of the opamp remains the same, irrespective of the load.

d) Zero offset voltage: This ensures zero output for zero input signal voltage in an ideal opamp.

e) Infinite bandwidth: This ensures that the gain of the op-amp will be constant over the

frequency range from d.c to infinite.

f) Infinite CMRR: This ensures zero common mode gain for an ideal op-amp. Due to this common mode noise output voltage is zero.
g) Infinite slew rate: This ensures that the changes in the o/p voltage occur simultaneously with the changes in the input voltage.

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The – and + symbols at the input refer to inverting and non-inverting input terminals respectively, i.e if $v_1 = 0$, output v_0 is 180° out of phase with input signal v_2. And, when $v_2 = 0$, output v_0 will

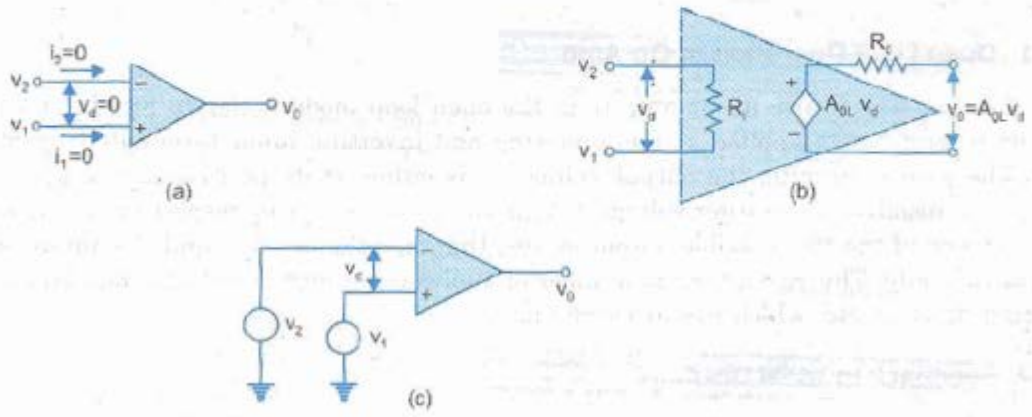


Fig. 2.4 (a) Ideal op-amp (b) Equivalent circuit of an op-amp (c) Open loop circuit

be in phase with the input signal applied at v_1. This op-amp is said to be ideal if it has the following characteristics,

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Output impedance	R_o	=	0
Bandwidth	BW	=	∞

Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$.

It can be seen that

(i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading oh the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non-inverting terminals, i.e., differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o.

(iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate soma of these characteristics.

A physical, amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 24 (b) where $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$. It can be seen that og-amp is a voltage controlled voltage source and $A_{OL}\, v_d$ is an equivalent *Thevenin* voltage source and R_o is *the Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the shown voltage is

$$v_o = A_{OL}\, v_d$$
$$= A_{OL}\,(v_1 - v_2) \qquad (2.1)$$

equation amplifies difference input voltages.

Q.7 a. What is the input impedance of a non-inverting operational amplifier? (4)

Answer:

Input resistance: This is the differential input resistance as seen at either of the input terminals with the other terminal connected to ground. For the 741C, the input resistance is 2 MΩ.

b. Explain why CMRR approaches infinity for an emitter coupled differential amplifier when R_E approaches to infinity. (4)

Answer:

Common-mode gain, A_{CM}

Now, consider the case when v_1 and v_2 both are increased by an incremental voltage v_c. The differential signal v_d now is zero and common-mode signal is v_c. Both the collector currents i_{C1} and i_{C2} will increase by an incremental current i_c. The current through R_E now increases by $2i_c$. The voltage, V_E at emitter node is now increased by $2i_c R_E$ and no longer constant. In order to draw the common mode half circuit, replace resistance R_E by $2R_E$ as shown in Fig. 2.14 (a). The common-mode gain, A_{CM} is calculated from the small-signal hybrid-π equivalent model shown in Fig. 2.14 (b). It can be seen,

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{v_{02}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E} \qquad (2.53\ (a))$$

For $\beta_0 >> 1$,

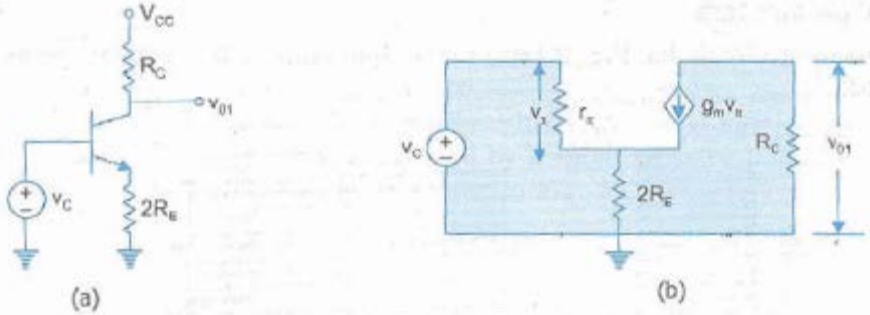


Fig. 2.14 (a) common-mode half circuit (b) ac equivalent circuit using hybrid-π model

$$A_{CM} = \frac{-g_m R_C}{1+2g_m R_E} \cong -\frac{R_C}{2R_E} \qquad (2.53\ (b))$$

It can be seen that, if the output is taken differentially, then the output voltage $v_{01} - v_{02}$ will be zero and the common-mode gain will be zero. In this analysis, we have assumed that the circuit is perfectly symmetrical. However, in practical circuits, it will not be so, and the differential output voltage will not be exactly zero. If the output is taken single ended, the common-mode gain will be finite and given by Eqs. (2.53 (a)) and (2.53 (b)).

The common mode gain, A_{CM}, using h-parameter model can be easily computed as

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{-h_{fe} R_C}{h_{ie} + (1+h_{fe})2R_E} \qquad (2.54)$$

The common-mode rejection ratio (CMRR) is defined as

$$\text{CMRR} = \frac{|A_{DM}|}{|A_{CM}|}$$

For differential-input, differential-output, using Eqs. (2.50) and (2.53 b), we obtain

$$\text{CMRR} \cong \frac{g_m R_C (1+2g_m R_E)}{g_m R_C}$$

$$= 1 + 2g_m R_E \qquad (2.55)$$

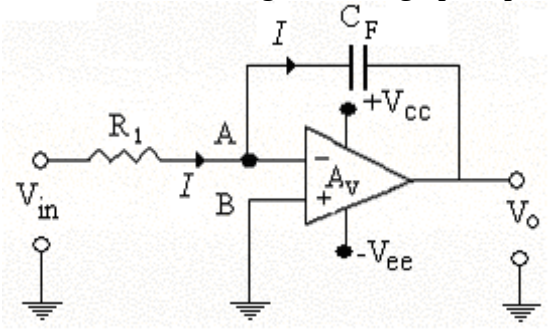
$$\cong 2 g_m R_E$$

c. Draw the circuit of Integrator using Op-Amp and derive an expression for its output voltage. (8)

Answer:

A circuit in which the output voltage is directly proportional to the integral of the input

voltage is called an integrator. Integrators can be passive integrator or active integrator. **Fig** shows an active integrator using op-amp.



Expression for output voltage:

Since node B is grounded, node A is also at ground potential. Hence VA=VB=0. As the input current of op- amp is zero, the current through CF is the current through R1. From input side

I = Vin/R1

From output side I = CF d(VA-VO)/dt = - CF(dVO/dt)

Therefore Vin/R1 = - CF (dVO/dt)

Integrating

$\int$ (Vin/R1) dt = - CF $\int$dVo / dt = - CF VO

Vo = -(1/R1 CF) $\int$Vin dt

Q.8 a. Draw the circuit diagram of Triangular Wave Generator & derive an expression for frequency of oscillation. (8)

Answer:

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. 5.12(a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. 5.12 (b). Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

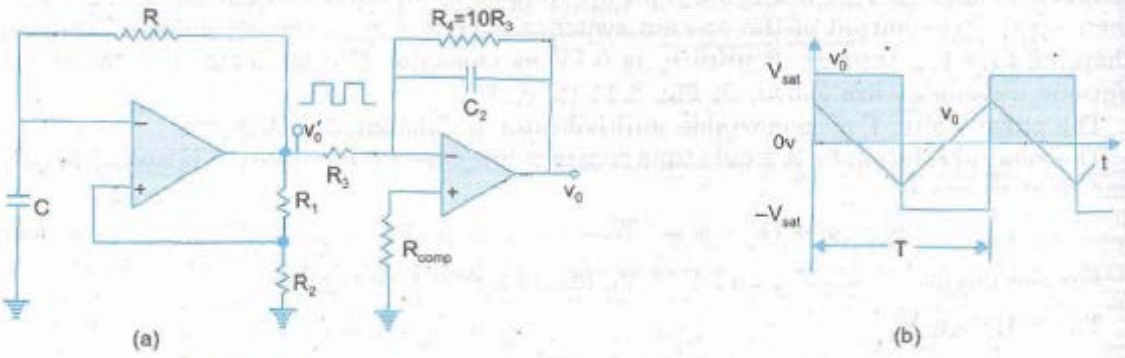


Fig. 5.12 (a) Triangular waveform generator (b) output waveform

Another triangular wave generator using lesser number of components is shown in Fig. 5.13(a). It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (–) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.

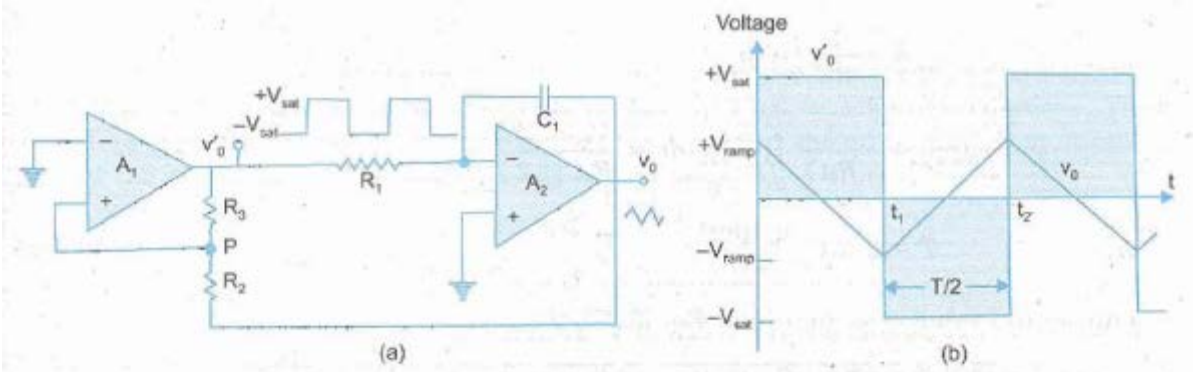


Fig. 5.13 (a) Triangular waveform generator using lesser components (b) Waveforms

Initially, let us consider that the output of comparator A_1 is at $+V_{sat}$. The output of the integrator A_2 will be a negative going ramp as shown in Fig. 5.13(b). Thus one end of the voltage divider R_2R_3 is at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2. At a time $t = t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0V. This switches the output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in the positive direction. And at the instant $t = t_2$, the voltage at point P becomes just above 0V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform. It can be seen that the frequency of the square wave and triangular wave will be the same. However, the amplitude of the triangular wave depends upon the RC value of the integrator A_2 and the output voltage level of A_1. The output voltage of A_1 can be set to desired level by using appropriate zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \tag{5.18}$$

At $t = t_1$, the voltage at point P becomes equal to zero. Therefore, from Eq. (5.18),

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \tag{5.19}$$

Similarly, at $t = t_2$, when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat}) \tag{5.20}$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o\,(pp) = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_3}V_{sat} \tag{5.21}$$

The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$. Putting the values in the basic integrator equation

$$v_o = -\frac{1}{RC}\int v_i\,dt$$

$$v_o(\text{pp}) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt = \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

or, $$T = 2\,R_1C_1\frac{v_o\,(\text{pp})}{V_{sat}} \qquad (5.22)$$

Putting the value of v_o (pp) from Eq. (5.21), we get

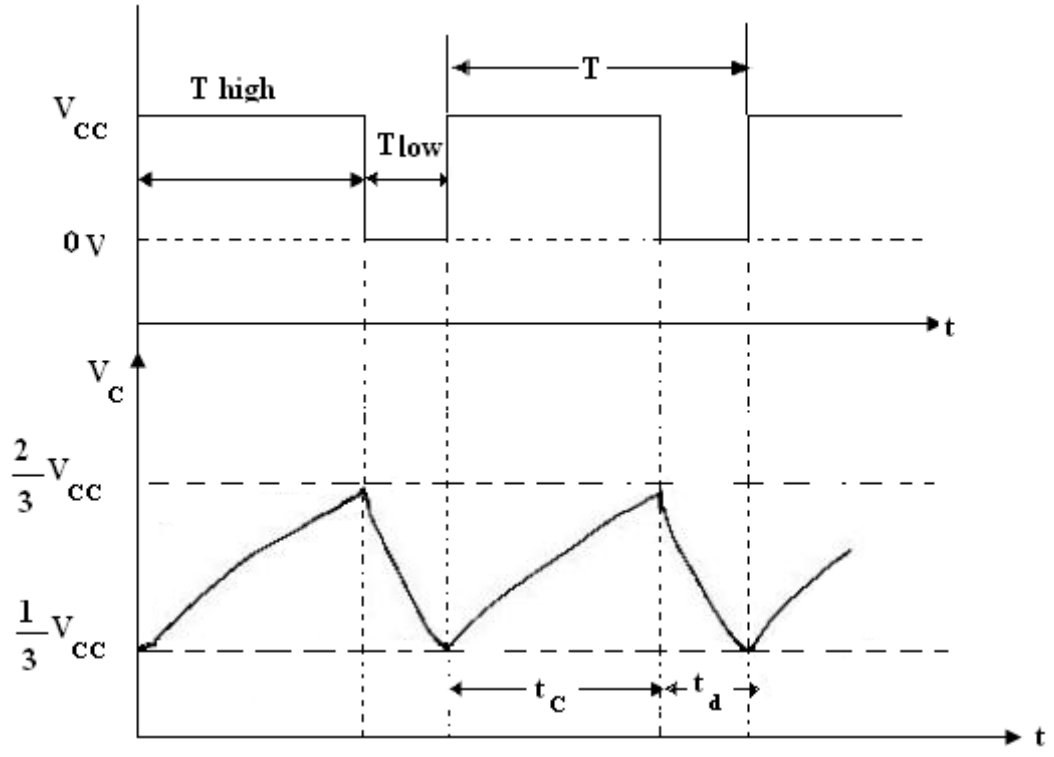
$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation f_o is,

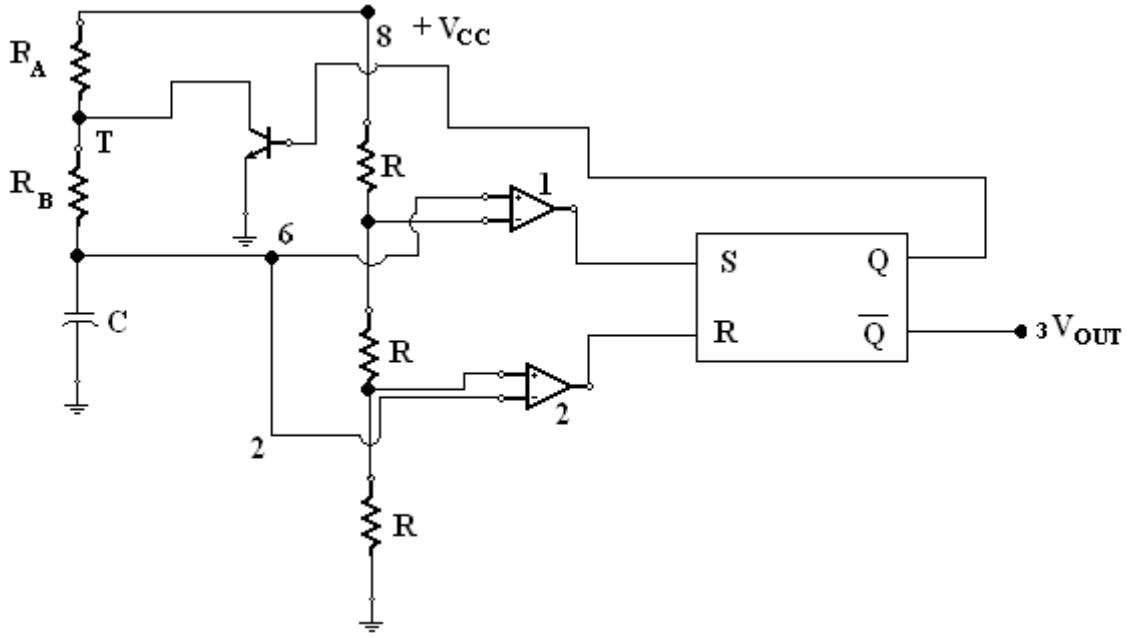
$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2} \qquad (5.23)$$

b. Explain how the timer IC 555 can be operated as an astable multivibrator, using timing diagrams. (8)

Answer:



An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave generating circuit. The timing during which the output is either high or low is determined by the externally connected two resistors and a capacitor.



Internal Circuitary With External Connections

When Q is low, or output Vout is high, the discharging transistor is cut-off and capacitor C begins charging towards Vcc through resistances RA and RB. Because of this, the charging time constant is (RA + RB)C. Eventually, the threshold voltage exceeds + 2/3 *Vcc*, comparator 1 has a high output and triggers the flip-flop so that its Q is high and the timer output is low. With Q high, the discharge transistor saturates and pin-7 grounds so that the capacitor C discharges through resistance RB, trigger voltage at inverting input of comparator-2 decreases. When it drops below 1/3 *Vcc*. The output of comparator 2 goes high and this reset the flip-flop so that Q is low and the timer output is high.

8.4 ASTABLE OPERATION

The device is connected for astable operation as shown in Fig. 8.15. For batter understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in Fig. 8.16. Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply V_{cc} is connected, the external timing capacitor C charges towards V_{cc} with a time constant $(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{cc}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped *the* timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{cc} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, *makes* transistor Q_1 on and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{cc}/0.2$ where 0.2 A is the maximum current through the *on* transistor Q_1.

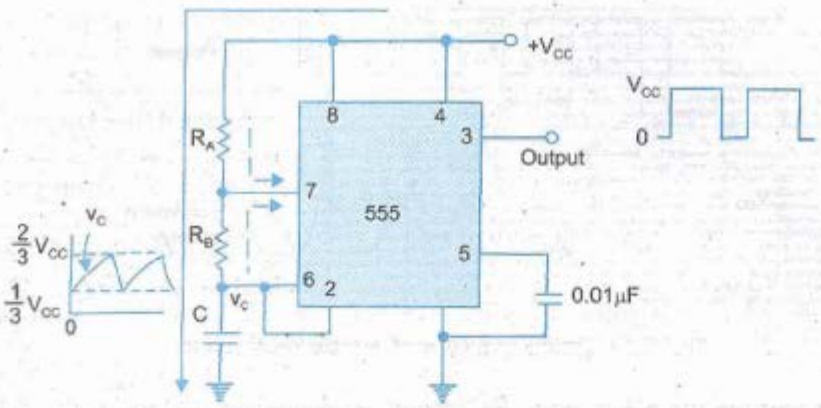


Fig. 8.15 Astable multivibrator using 555 timer

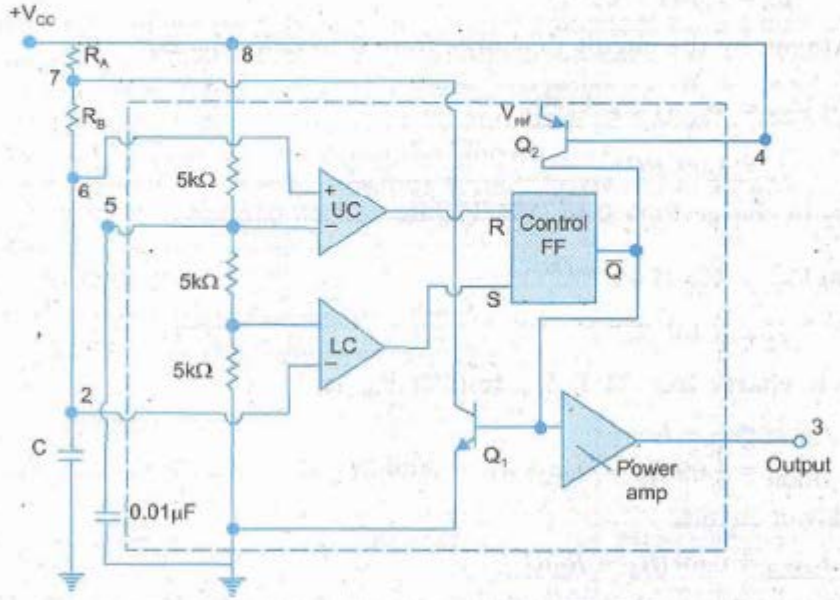


Fig. 8.16 Functional diagram of astable multivibrator using 555 timer

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{CC}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{CC} and (1/3) V_{CC} respectively. Figure 8.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{CC} to (2/3) V_{CC}. It may be calculated as follows:

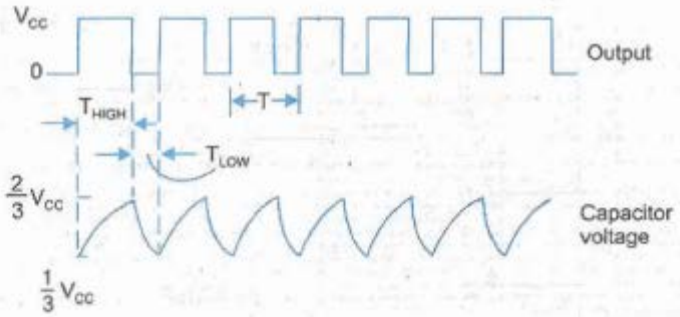


Fig. 8.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$(2/3)\,V_{CC} = V_{CC}\,(1 - e^{-t_1/RC}) \tag{8.9}$$

or, $$t_1 = 1.09\,RC$$

and the time t_2 to charge from 0 to (1/3) V_{CC} is,

$$(1/3)\,V_{CC} = V_{CC}\,(1 - e^{-t_2/RC}) \tag{8.10}$$

or, $$t_2 = 0.405\,RC$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$
$$t_{HIGH} = 1.09\,RC - 0.405\,RC = 0.69\,RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C \tag{8.11}$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$(1/3)\,V_{CC} = (2/3)V_{CC}\,e^{-t/RC}$$

Solving, we get $t = 0.69\,RC$

So, for the given circuit, $t_{LOW} = 0.69\,R_BC$ (8.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\,(R_A + 2R_B)\,C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{8.13}$$

Figure 8.18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is *on*, the output goes low. Hence,

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \quad (8.14)$$

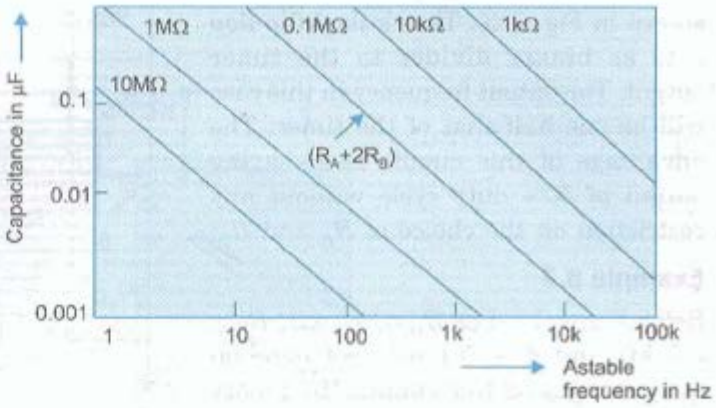


Fig. 8.18 Frequency dependence of R_A, R_B and C

With the circuit configuration of Fig. 8.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69(R_A + R_B)C$ will always be greater than $t_{LOW} = 0.69\ R_B C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{cc} and extra current will flow through Q_1 when it is *on*. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 8.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $t_{LOW} = 0.69\ R_B C \quad (8.15)$

$$T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C \quad (8.16)$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \quad (8.17)$$

and duty cycle $D = \dfrac{R_B}{R_A + R_B}$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistor are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is

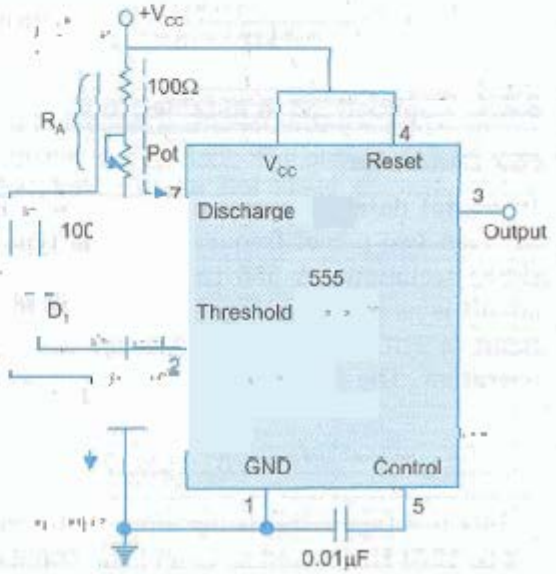


Fig. 8.19 Adjustable duty cycle rectangular wave generator

shown in Fig. 8.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

Q.9 (For Current Scheme students i.e. DE56)

a. Write the limitations of three terminal voltage regulators & explain the 723 general purpose voltage regulators with diagram. (8)

Answer:

The three terminal regulators discussed earlier have the following limitations:

1. No short circuit protection
2. Output voltage (positive or negative) is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

Figure 6.7(a) shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage V_{ref} applied at the NI input terminal. The error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. 6.7(b). The important features and electrical characteristics are given in Table 6.2.

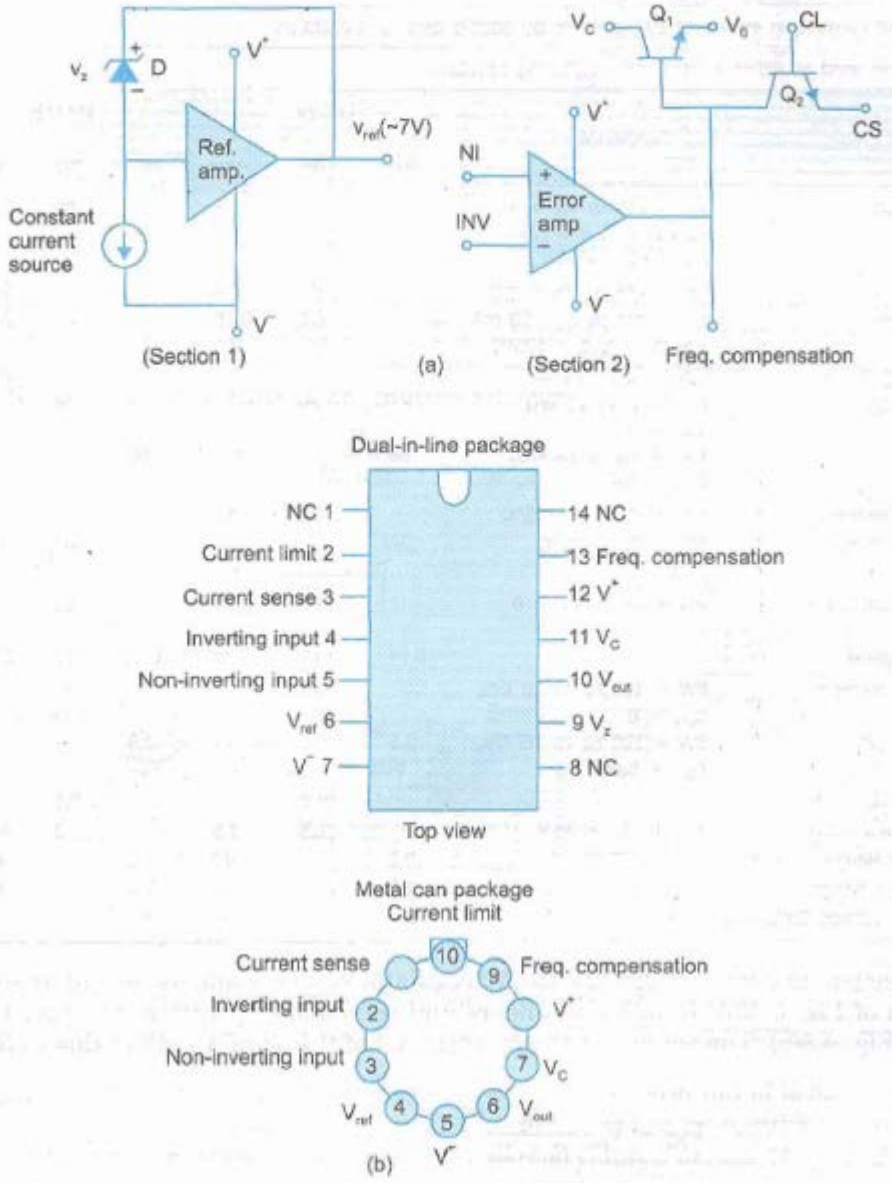


Fig. 6.7 (a) Functional block diagram of 723 regulator
(b) Pin diagram for 14-pin DIP and 10-pin metal-can

A simple positive low-voltage (2V to 7V) regulator can be made using 723 as shown in the schematic of Fig. 6.8(a). In order to understand the circuit operation, consider the detailed circuit of Fig. 6.8(b). The voltage at the NI terminal of the error amplifier due to R_1R_2 divider is,

$$V_{NI} = V_{ref}\frac{R_2}{R_1 + R_2} \tag{6.13}$$

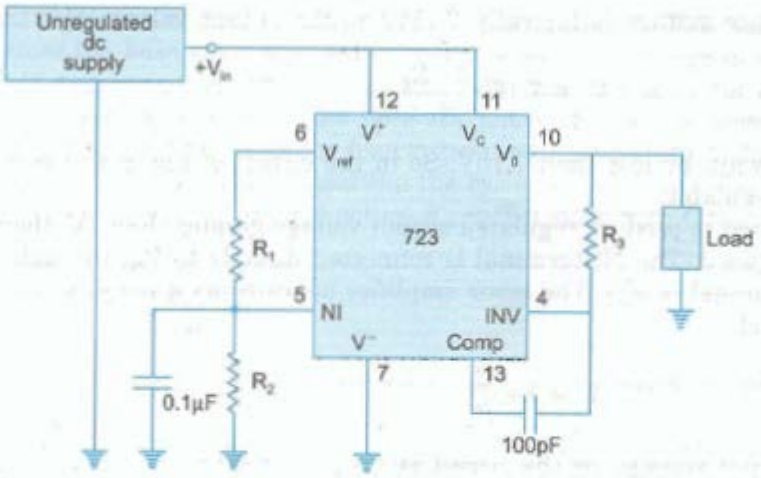


Fig. 6.8 (a) A low voltage regulator using 723 IC

The difference between V_{NI} and the output voltage V_o which is directly fed back to the INV terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q_1 so as to minimize the difference between the NI and INV inputs of error amplifier. Since Q_1 is operating as an emitter follower

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2} \qquad (6.14)$$

b. Write a short note on complementary emitter follower circuit. (4)

Answer:

19-4 CAPACITOR-COUPLED AND DIRECT-COUPLED OUTPUT STAGES

Complementary Emitter Follower

Two BJTs connected to function as emitter followers are shown in Fig. 19-17. Although one is *npn* and the other is *pnp*, the devices are selected to have similar parameters, so they are complementary transistors. The circuit is termed a *complementary emitter follower* or *push-pull emitter follower.*

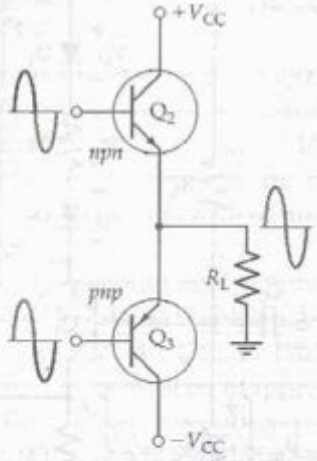


Figure 19-17 A complementary emitter follower uses an *npn* transistor and a *pnp* transistor that have similar characteristics.

A single-transistor emitter follower is essentially a small-signal circuit, because large signals can reverse-bias the transistor base-emitter junction when the input polarity is opposite to the transistor V_{BE} polarity. An *npn* emitter follower might not correctly reproduce the negative-going portion of a large signal, while a *pnp* emitter follower might not reproduce the positive-going portion. Complementary emitter followers have similar signals applied simultaneously to both device bases, as illustrated. Transistor Q_2 conducts during the positive half-cycle of the signal, and it *pulls* the output voltage up to follow the input. During this time, Q_3 base-emitter junction is reverse biased. For the duration of the negative half-cycle of the input, the Q_2 base-emitter junction is reversed and Q_3 conducts, pulling the output down to follow the input. Thus the complementary emitter follower is a large-signal circuit with the low output impedance typical of emitter followers.

c. Explain monolithic power amplifiers. (4)

Answer:

Monolithic Power Amplifiers

The general purpose op-amp 741 can deliver about 100 mW of power which is not sufficient for most of the applications. A wide range of IC power amplifiers are now commercially available. National Semiconductors produces two popular IC power amplifiers LM380 and LM384. The pin configuration, circuit diagram and typical applications are discussed.

LM380 Power Audio Amplifiers

The LM380 power audio amplifier is designed to deliver 2.5W (r.m.s) to a capacitively coupled 8-Ω load. Kg. 4.46(a) and (b) shows the pin configuration and block diagram of LM380 respectively. It is available in a 14-pin DIP package. A copper lead frame used with the center three pins on either side (3, 4, 5 on the left and 10, 11, 12 on *the* right) forms a heat sink. Thus there is no need to use a separate heat sink for the audio amplifier. The internal schematic diagram of LM380 is shown in Fig. 4.46(c).

It can be seen that it has four stages: (i) PNP emitter follower; (ii) differential amplifier (iii) common emitter and (iv) quasi complementary emitter follower.

The input is coupled through inverting input terminal (pin-6) and non-inverting input terminal (pin-2) to emitter follower stages composed of PNP input transistors Q_1 and Q_2. The output from Q_1 and Q_2 drives the PNP Q_3-Q_4 differential pair. Transistors Q_5 and Q_6 constitute the collector loads for the PNP differential pair. The current in the PNP differential pair Q_3-Q_4 is established by Q_7, R_3 and V_{cc}. The transistors Q_7 and Q_8 form the current mirror and establish current in Q_9 which forms the common emitter voltage gain stage. The output of the differential pair Q_3-Q_4 is taken at the junction of Q_4 and Q_6 and is applied as input to CE voltage gain stage. The capacitor C (10 pF) between base and collector of Q_9 provides internal compensation and establishes the upper cut-off frequency of 100 kHz at 2W for 8Ω loads. As Q_7-Q_8 form a current mirror, the current through diodes D_1 and D_2 is same as that through R_3. The output stage is a quasi (false) -complementary pair emitter follower formed by transistors Q_{10} and Q_{12}. In fact, the combination of PNP transistor Q_{11} and NPN transistor Q_{12} has the power capability of an NPN transistor but the characteristics of a PNP transistor. The diodes D_1 and D_2 are used to minimize cross-over distortion. The resistors R_6 and R_7 are used for current limiting. The quiescent output voltage is established at $V_{cc}/2$ by resistors R_3 and R_4. To decouple the input stages from the supply voltage V_{cc}, a bypass capacitor of the order of micro farads should be connected between the by-pass terminal (pin 1) and ground (pin 7).

Same of the important features of LM380 are listed below:

(i) Internally fixed gain *d50* (34 dB)
(ii) Wide supply voltage range (5V to 22V)
(iii) High peak current capability (1.3A max.)
(iv) Low total harmonic distortion (0.2%)
(v) Output automatically self-centering to one-half of the supply voltage
(vi) Output short circuit proof with internal thermal limiting
(vii) High input impedance (15° kΩ)
(viii) BW of 100 kHz at an output power of 2W and a load of 8Ω.

Another commonly used audio power amplifier is LM384. The internal diagram is similar to that of LM380, except that it is designed to deliver 5W power output.

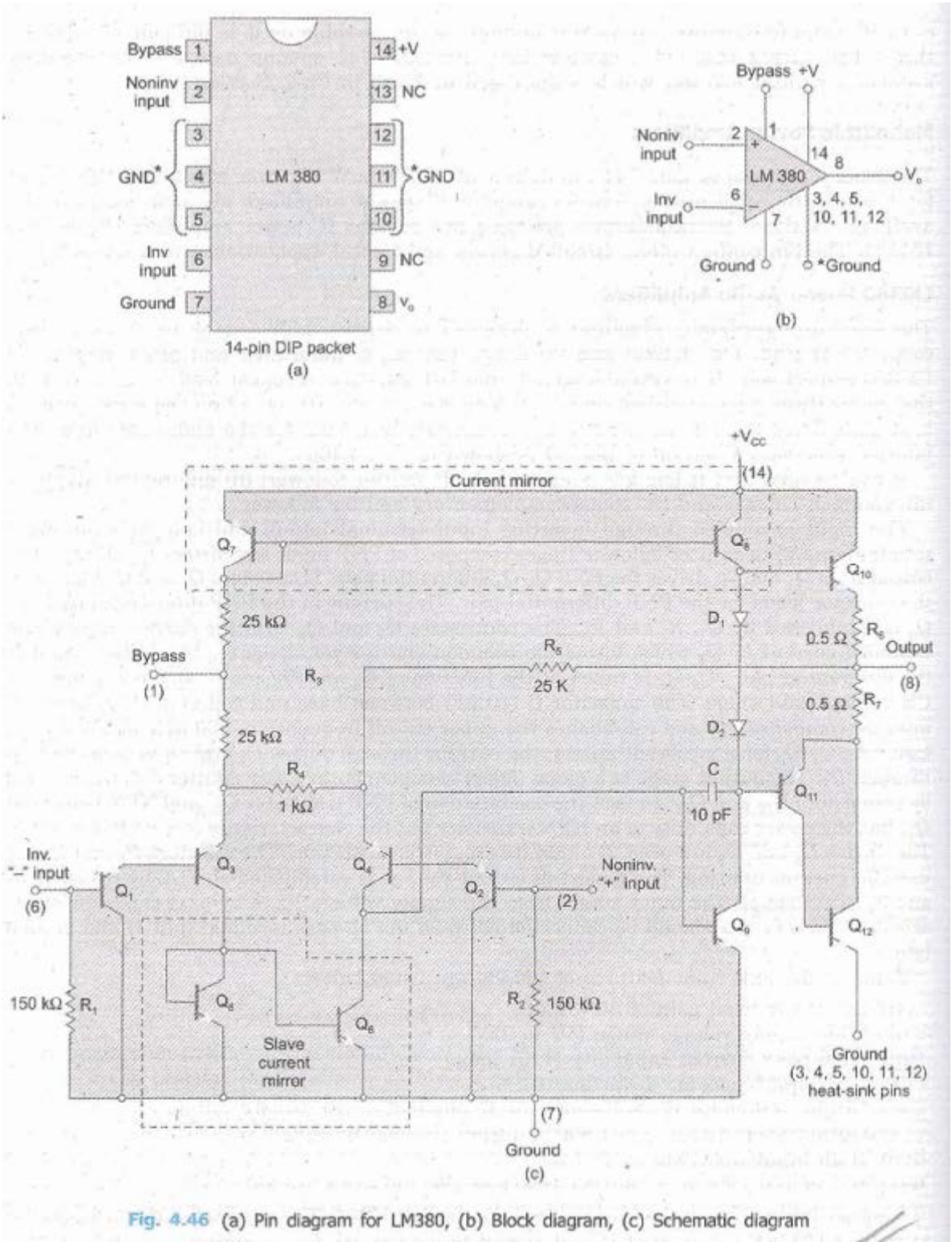


Fig. 4.46 (a) Pin diagram for LM380, (b) Block diagram, (c) Schematic diagram

Q.9 (For New Scheme students i.e. DE106)

a. Explain the concept of FET switching. (4)

Answer:

FET Switching

The direct-coupled JFET switching circuit in Fig. 9-28a is similar to the BJT switching circuit in Fig. 8-18a, but there are important differences in the operation and performance of the two circuits.

In Section 9-3, it is explained that a FET can be biased *on* to produce the lowest possible *drain-source on voltage* ($V_{DS(on)}$), which corresponds to $V_{CE(sat)}$ for a BJT. $V_{DS(on)}$ occurs when the device has a minimum channel resistance known as the *drain-source on resistance* ($r_{DS(on)}$). As illustrated in Fig. 9-28b, the output voltage is

$$V_{DS(on)} = I_D \times r_{DS(on)}$$

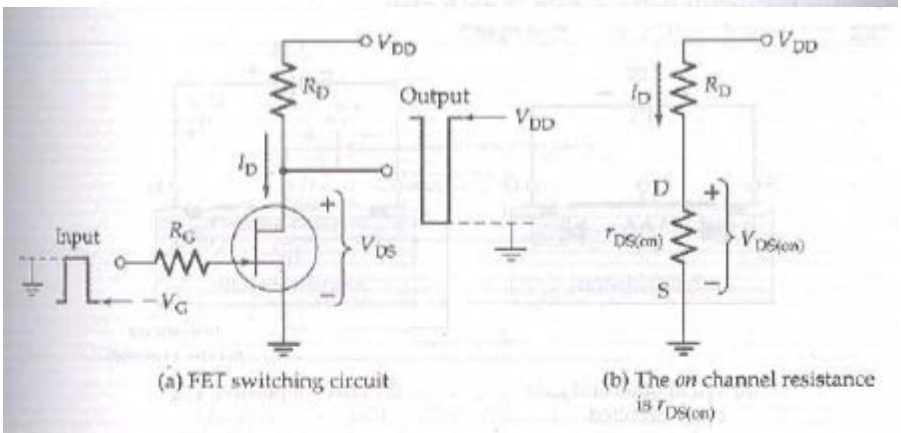


Figure 9-28 Direct-coupled *n*-channel JFET switching circuit. The output switches from V_{DD} to $I_D \times r_{DS(on)}$ when the input changes from $-V_G$ to zero.

Like a BJT switch, a FET switching circuit has turn-on and turn-off times that are made up of delay time, rise time, storage time, and fall time. FET switching times tend to be shorter than BJT times because a FET does not have a forward-biased junction with a diffusion capacitance (like the BJT base-emitter junction).

FET switching circuits are covered further in Section 10-11.

b. Write a short note on photo-diodes with applications. (4)

Answer:

Photodiode Operation

When a *pn*-junction is reverse biased, there is a small reverse saturation current because thermally generated holes and electrons are being swept across the junction as minority charge carriers (see Section 1-6). Increasing the junction temperature generates more hole-electron pairs, and so the minority carrier (reverse) current is increased. The same effect occurs if the junction is illuminated (see Fig. 21-17). Hole-electron pairs are generated by the incident light energy, and minority charge carriers are swept across the junction to

produce a reverse current flow. Increasing the junction illumination increases the number of charge carriers generated and, thus, increases the reverse current level. Diodes designed to be sensitive to illumination are known as *photodiodes*.

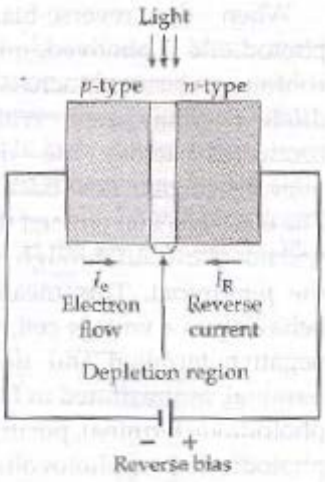


Figure 21-17 A photodiode has a reverse-biased *pn*-junction designed to be light-sensitive. There is a minority charge carrier current when the junction is illuminated.

Characteristics

Consider the typical photodiode illumination characteristics in Fig. 21-18. When the junction is dark, the *dark current* (I_D) would seem to be zero. Typically, I_D is around 2 nA. A 20 mW/cm^2 illumination level produces a reverse current of approximately 60 μA. Increasing the reverse voltage does not increase I_R significantly. So each characteristic is approximately a horizontal line.

Figure 21-19 shows a simple photodiode circuit using a 2 V reverse bias. (Note the device circuit symbol.) Assuming that D_1 has the characteristics in Fig. 21-18, the current at a 5 mW/cm^2 illumination level is approximately 13 μA. At 20 mW/cm^2, the diode current is around 60 μA. The device resistance at each illumination level is readily calculated: (at 5 mW/cm^2, R = 2 V/13 μA = 154 kΩ), (at 20 mW/cm^2, R = 2 V/60 μA = 33 kΩ). The resistance changes by a factor of approximately 5 from the low to the high illumination level, showing that a photodiode can be used as a photoconductive device.

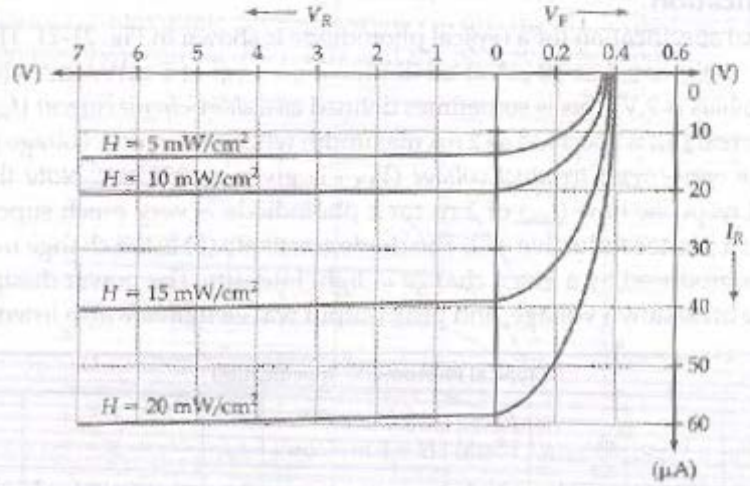


Figure 21-18 Typical photodiode characteristics. The reverse current remains substantially constant for each level of illumination.

When the reverse-bias voltage across a photodiode is removed, minority charge carriers continue to be swept across the junction while the diode is illuminated. With an external circuit connected across the diode terminals, the minority carriers flow back to their original sides. The electrons that crossed the junction from *p* to *n* will now flow out through the *n*-terminal and into the *p*-terminal. This means that the device is behaving as a voltage cell, with the *n*-side as the negative terminal and the *p*-side the positive terminal, as illustrated in Fig. 21-20. In fact, a voltage can be measured at the photodiode terminal, positive on the *p*-side and negative on the *n*-side. So the photodiode is a photovoltaic device as well as a photoconductive device. The characteristics in Fig. 21-18 show that, when illuminated, the photodiode actually has to be forward biased to reduce the reverse current to zero.

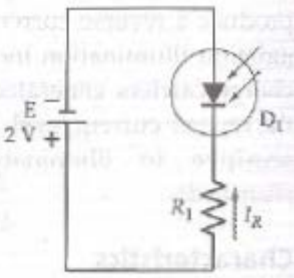


Figure 21-19 Photodiode circuit with a reverse-bias voltage.

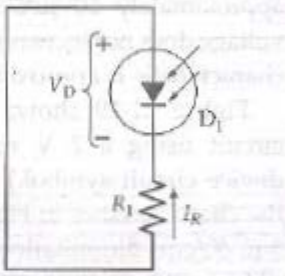


Figure 21-20 An illuminated photodiode without an external bias operates as a photovoltaic device.

It should be noted that V_R and V_F have different scales on the photodiode characteristics shown in Fig. 21-18. A dc load line that crosses between the forward- and reverse-biased regions cannot be drawn on these characteristics. Equal scales must be used for each part of the characteristics to draw such a load line.

Specification

A partial specification for a typical photodiode is shown in Fig. 21-21. The *light current* (I_L) is listed as 10 μA at an illumination level of 5 mW/cm^2 when the reverse bias is 2 V. This is sometimes defined as a *short-circuit current* (I_{SC}). The *dark current* (I_D) is specified as 2 nA maximum when the reverse voltage is 20 V, and the *open-circuit terminal voltage* (V_{OC}) is given as 350 mV. Note that the typical response time (t_{res}) of 2 ns for a photodiode is very much superior to that for a photoconductive cell. The diode *sensitivity* (*S*) is the change in diode current produced by a given change in light intensity. The power dissipation, reverse breakdown voltage, and peak output wavelength are also listed.

Typical Photodiode Specification

P_D	V_{OC}	$BV_{R(max)}$	$I_{D(max)}$ (dark)	I_L [V_R = 2 V, H = 5 mW/cm^2]	t_{res}	S	λ_p
100 mW	350 mV	100 V	2 nA	10 μA	2 ns	7 μA/mW/cm^2	900 nm

Figure 21-21 Partial specification for a low-current photodiode.

Construction

Figure 21-22a shows the cross-section of a diffused photodiode. It is seen that a thin, heavily-doped *p*-type layer is situated at the top, where it is exposed to incident light. The junction depletion region penetrates deeply into the lightly-doped *n*-type layer. This is in contact with a lower, heavily-doped *n*-type layer, which connects to a metal film contact. A ring-shaped contact is provided at the top of the *p*-type layer. Low-current photodiodes (also called *signal photodiodes*) are usually contained in a TO-type can with a lens at the top (see Fig. 21-22b). Transparent plastic encapsulation is also used (Fig. 21-22c).

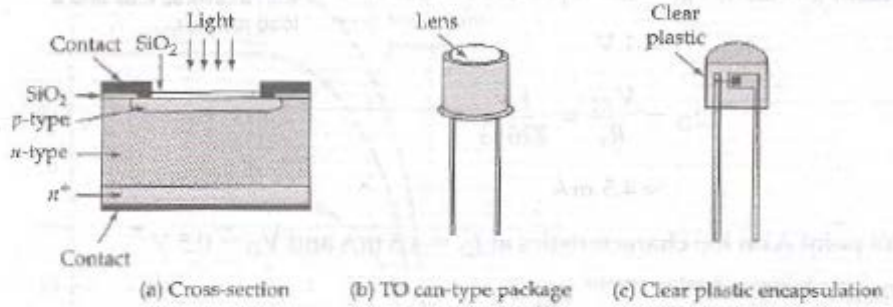


Figure 21-22 Photodiode cross-section and typical packages.

Photodiode Applications

Photodiodes can be used as photoconductive devices in the type of circuits discussed in Section 21-4. They can also be used in circuits, where they function as photovoltaic devices. Figure 21-23 shows typical photodiode characteristics plotted in the first and second quadrants for convenience. When the device is operated with a reverse voltage, it functions as a photoconductive device. When operating without the reverse voltage, it operates as a photovoltaic device. In some circuits the photodiode can change between the photoconductive mode and the photovoltaic mode.

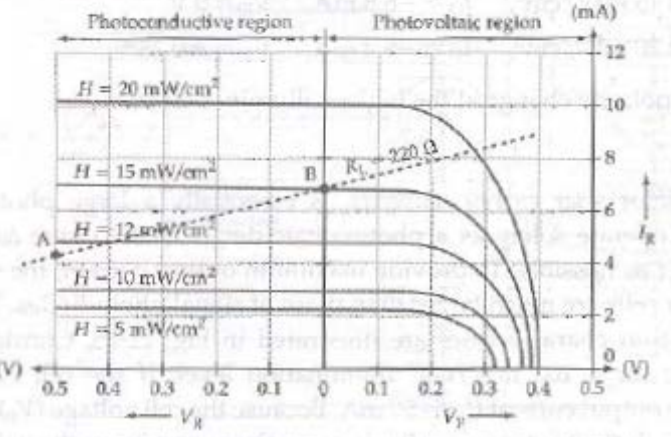


Figure 21-23 Photodiode characteristics have a photoconductive region and a photovoltaic region.

c. Draw the functional diagram of Counter Type ADC & explain its operation. (8)

Answer:

10.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ± (1/2) LSB to the analog input V_a which is to be cohverted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when *the* DAC output has come within ± (1/2) LSB to V_a.

A 3-bit counting ADC based upon the above principle is shown in Fig, 10.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the *AND* gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output ia a staircase of the type shown in Fig. 10.11 (b). The analog output V_d of DAC is compared to the analog input V_a by the comparator, If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the dock pulses to the counter. When $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a. For a new value of analog input V_a, a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again

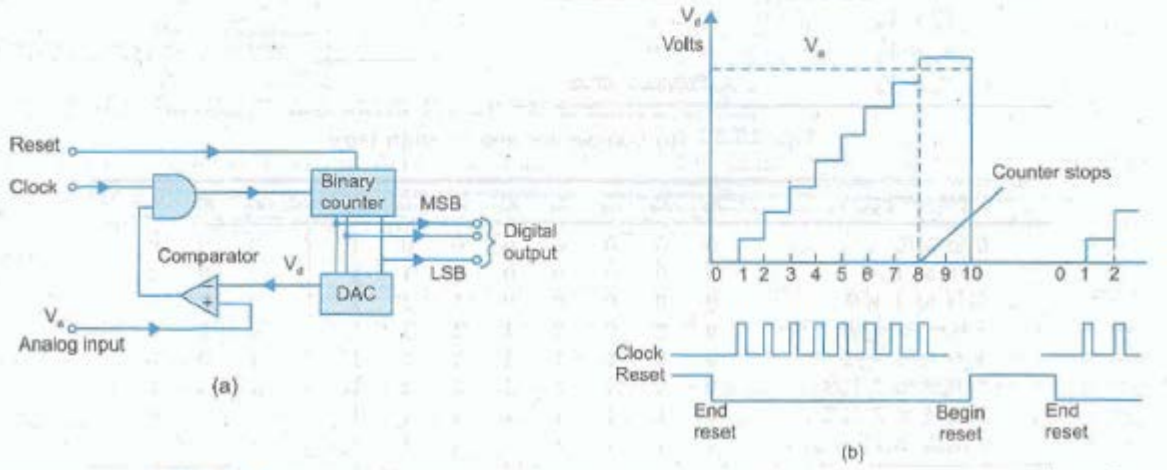


Fig. 10.11 (a) A counter type A/D converter (b) D/A output staircase waveform

as shown in Pig. 10.11 (b). The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond. Low speed is the most serious drawback of this method. The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input voltage V_a. For instance, a 12-bit system with 1 MHz clock frequency, the counter will take $(2^{12} - 1)$ μs = 4.095 ms to convert a full scale input.

If the analog input voltage varies with time, the input signal is sampled, using a sample and hold circuit before it is applied to the comparator. If the maximum value of the analog voltage is represented by n-pulses and if the clack period is T seconds, the minimum interval between samples is nT seconds.

TEXT BOOK

I. Electronic Devices and Circuits, Fourth Edition, David A Bell, PHI (2006)

II. Linear Integrated Circuits, Revised Second Edition, D. Roy Choudhury, Shail B. Jain, New Age International Publishers