Q.1 a. Why MOS technology has become dominant technology in IC industry?

Answer:

The prime reason being the Scaling Ability of MOSFET device, Less leakage Currents and low power consumption.

- It offers High Noise Margin
- High Packing Density
- High Input Impedance.

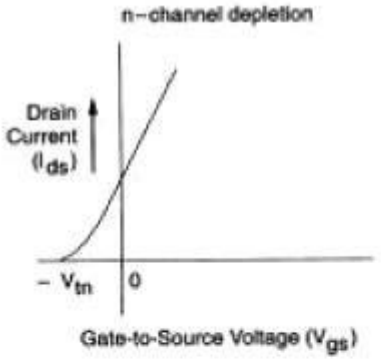
b. What is the use of SiO_2 layer in MOSFET devices?

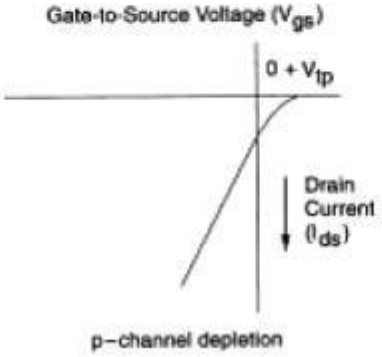
Answer:

The Silicon Di-Oxide (SiO2) layer is used as insulator in semiconductors. In MOSFETS, the SiO2 layer forms the Gate region. Other than these uses, there is another VLSI process called SOI (Silicon on Insulator). This uses the SiO2 as the base insulating layer on which the other layers (Drain, Source, etc) are grown.

c. Draw the graph of V_{GS} and I_{DS}, for a fixed V_{DS} of p-channel & n-channel depletion transistors.

Answer:





d. List the all second order effects of MOSFET.

Answer:

Following are the list of second order effects of MOSFET.

Threshold voltage – Body effect, Subthreshold region, Channel length modulation, Mobility variation, Fowler_Nordheim Tunneling, Drain Punchthrough, Impact Ionization – Hot Electrons.

e. With the help of example, explain Mealy and Moore machine.

Answer:

f. List all the Sources of Power Dissipation in MOS devices.

Answer:

Three components:

Dynamic Capacitive (Switching) Power:

- Charging and Discharging the capacitance.
- Still dominant component in current technology.

Short-circuit Power:

- Due to current flow from Vdd to Vss.
- Worst in case of slow transition.

Leakage Current:

- Diodes Leakage around transistor and N-well.
- Increases 20 times for each new technology.
- Becoming insignificant to the dominant factor.

g. List the electrical faults in turn can be translated into logical faults **(7x4)**

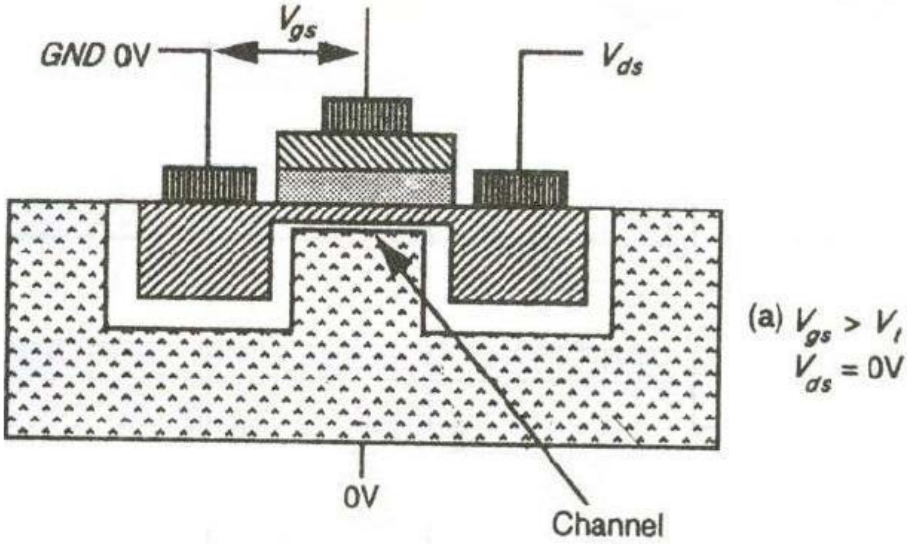
Answer:

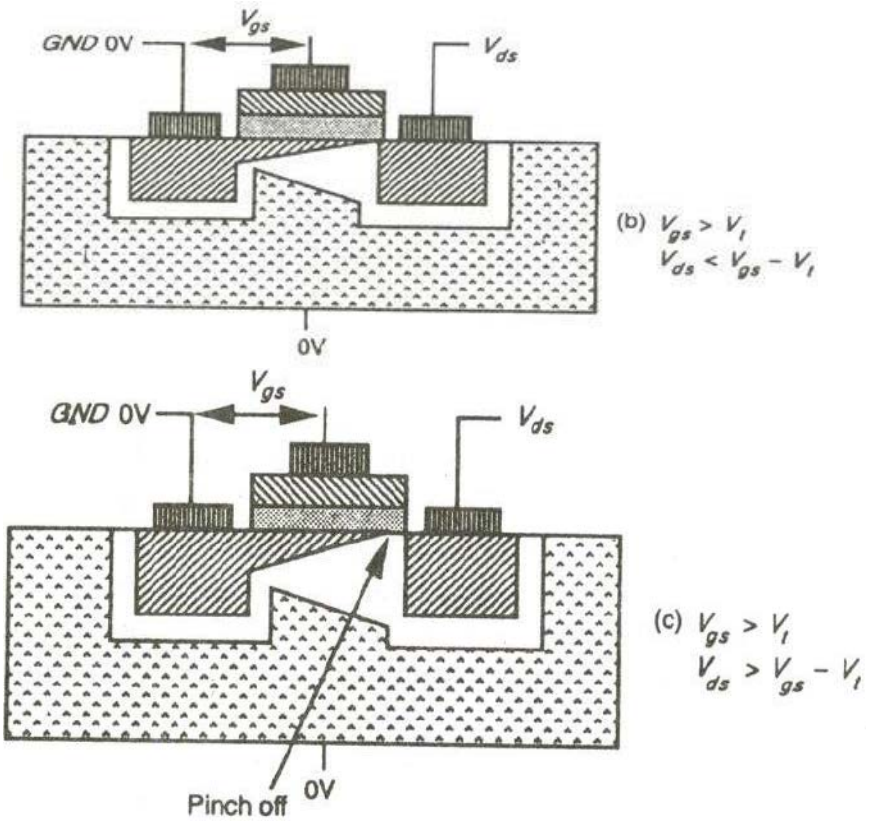
The logical faults include:

1. Logical stuck –at-0 and Logical stuck-at-1
2. Slower Transition (Delay Fault)
3. AND-bridging, OR-bridging.

Q.2 a. Explain the enhancement mode MOS transistor action. **(4)**

Answer:





To establish the channel between the source and the drain a minimum voltage (Vt) must be applied between gate and source. This minimum voltage is called as ―Threshold Voltage‖. The complete working of enhancement mode transistor can be explained with the help of diagram a, b and c.

a) Vgs > Vt
Vds = 0

Since Vgs > Vt and Vds = 0 the channel is formed but no current flows between drain and source.

b) Vgs > Vt

Vds < Vgs - Vt

This region is called the non-saturation Region or linear region where the drain current increases linearly with Vds. When Vds is increased the drain side becomes more reverse biased (hence more depletion region towards the drain end) and the channel starts to pinch. This is called as the pinch off point.

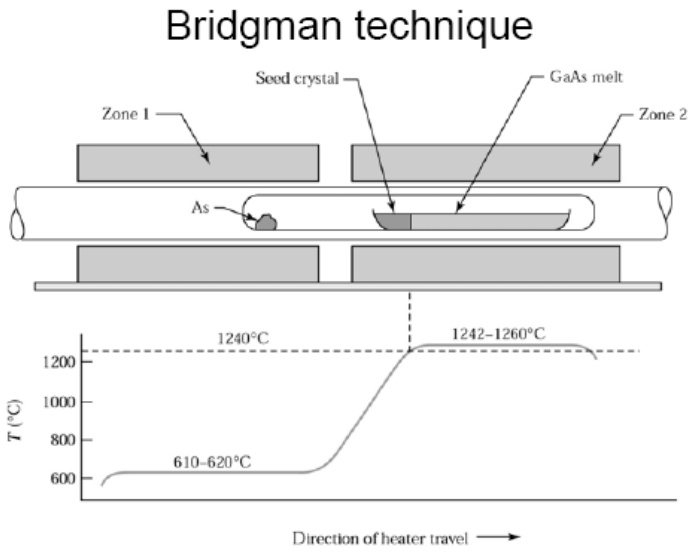
c) Vgs > Vt

Vds > Vgs - Vt

This region is called Saturation Region where the drain current remains almost constant. As the drain voltage is increased further beyond (Vgs-Vt) the pinch off point starts to move from the drain end to the source end. Even if the Vds is increased more and more, the increased voltage gets dropped in the depletion region leading to a constant current. The typical threshold voltage for an enhancement mode transistor is given by Vt = 0.2 * Vdd.

b. Explain with neat sketch, Bridgman Technique of crystal growth. (8)

Answer:



c. Calculate the threshold voltage V_{TO} at V_{SB} = 0 for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping $N_A = 10^{16}cm^{-3}$, polysilicon gate doping density $N_D = 2\times10^{20}cm^{-3}$, gate oxide thickness t_{ox} = 500 Å and oxide interface fixed charge density $N_{OX} = 4\times 10^{10}cm^{-3}$. (6)

Answer:

First, calculate the Fermi potentials for the p-type substrate and for the n-type polysilicon gate:

$$\phi_F(substrate) = \frac{kT}{q}\ln\left(\frac{n_i}{N_A}\right) = 0.026\text{ V}\cdot\ln\left(\frac{1.45\cdot10^{10}}{10^{16}}\right) = -0.35\text{ V}$$

Since the doping density of the polysilicon gate is very high, the heavily doped n-type gate material is expected to be degenerate. Thus, we may assume that the Fermi potential of the polysilicon gate is approximately equal to the conduction band potential, i.e., $\phi_F(gate) = 0.55$ V. Now, calculate the work function difference between the gate and the channel:

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) = -0.35\text{ V} - 0.55\text{ V} = -0.90\text{ V}$$

The depletion region charge density at $V_{SB} = 0$ is found as follows:

$$\begin{aligned} Q_{B0} &= -\sqrt{2\cdot q\cdot N_A\cdot\varepsilon_{Si}\cdot|-2\phi_F(substrate)|} \\ &= -\sqrt{2\cdot1.6\cdot10^{-19}\cdot10^{16}\cdot11.7\cdot8.85\cdot10^{-14}|-2\cdot0.35|} \\ &= -4.82\cdot10^{-8}\text{ C/cm}^2 \end{aligned}$$

The oxide-interface charge is:

$$Q_{ox} = q\cdot N_{ox} = 1.6\cdot10^{-19}\text{ C}\times4\cdot10^{10}\text{ cm}^{-2} = 6.4\cdot10^{-9}\text{ C/cm}^2$$

The gate oxide capacitance per unit area is calculated using the dielectric constant of silicon dioxide and the oxide thickness t_{ox}.

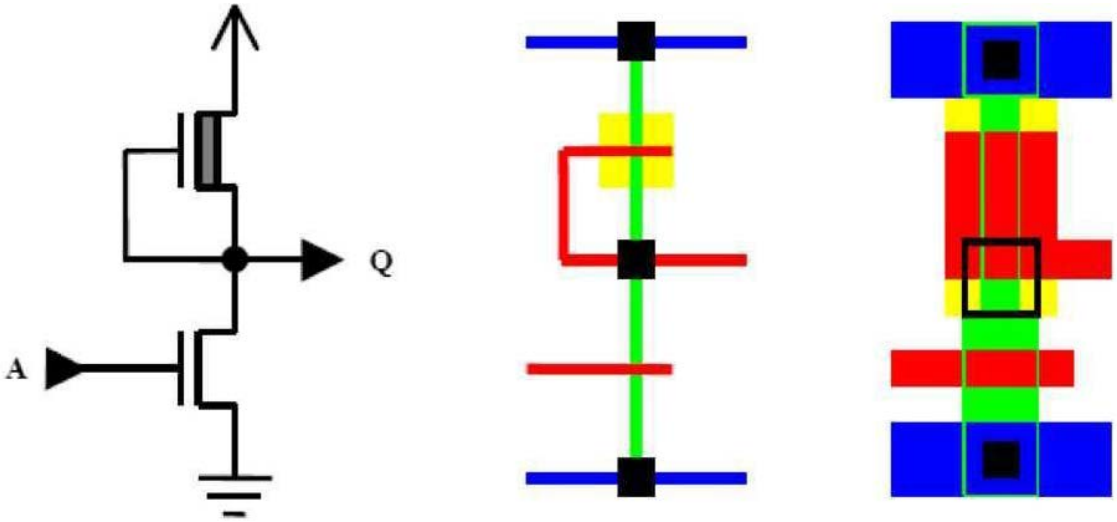
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97\cdot8.85\cdot10^{-14}\text{ F/cm}}{500\cdot10^{-8}\text{ cm}} = 7.03\cdot10^{-8}\text{ F/cm}^2$$

Now, we can combine all components and calculate the threshold voltage.

$$\begin{aligned} V_{TO} &= \Phi_{GC} - 2\phi_F(substrate) - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\ &= -0.90 - (-0.70) - (-0.69) - 0.09 = 0.40\text{ V} \end{aligned}$$

Q.3 a. Draw and explain Schematic, Stick Diagram and Layout of n-MOS depletion load inverter. (10)

Answer:



b. Explain the wafer shaping techniques used after crystal growth. (8)

Answer:

Wafer shaping

- Remove ends of ingot
- Grind the ingot to a well defined diameter
- Grind "flats" to mark crystal orientation
- Slice into wafers
- Lap and polish

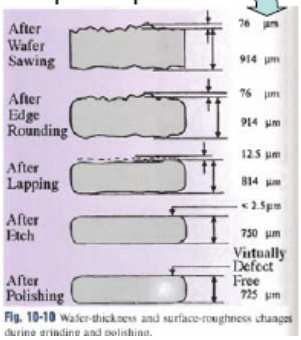
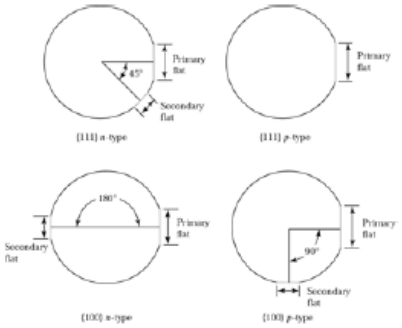


Fig. 10-10 Wafer-thickness and surface-roughness changes during grinding and polishing.



Q.4 a. Define port mode of the interface and describe all Port modes of an Entity. (6)

Answer:

The *Port Mode* of the interface describes the direction in which data travels with respect to the c*omponent*

• **In**: Data comes in this port and can only be read within the entity. It can appear **only on the right side** of a signal or variable assignment.

• **Out**: The value of an output port can only be updated within the entity. **It cannot be read**. It can only appear **on the left side** of a signal assignment.

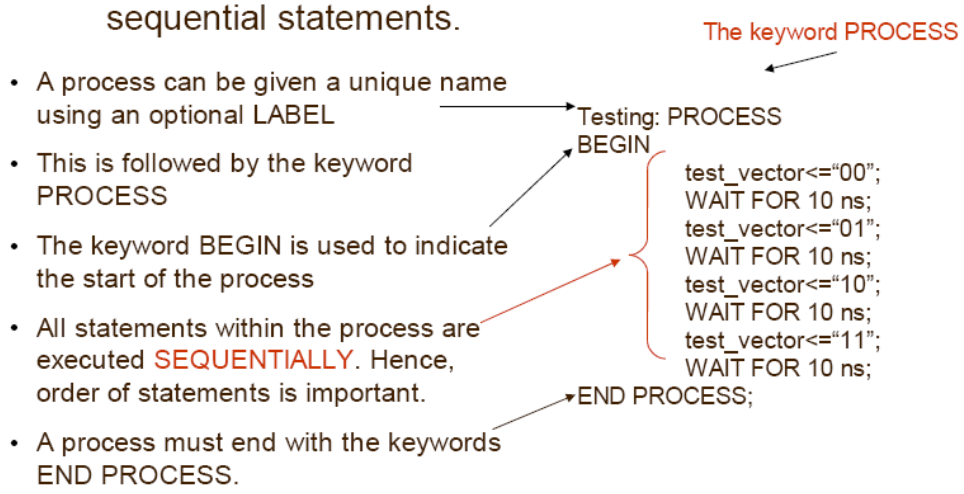
• **Inout**: The value of a bi-directional port can be read and updated within the entity model. It can appear on **both sides** of a signal assignment.

• **Buffer:** Used for a signal that is an output from an entity. The value of the signal can be used inside the entity, which means that in an assignment statement the signal can appear on the left and right sides of the <= operator.

b. What is a Process? Explain the process block execution of statements. (8)

Answer:

- A process is a sequence of instructions referred to as sequential statements.



c. Write a behavioural modelling of one-bit comparator. (4)

Answer:

Q.5 a. Discuss the Limitations of Scaling in VLSI Designs. (8)

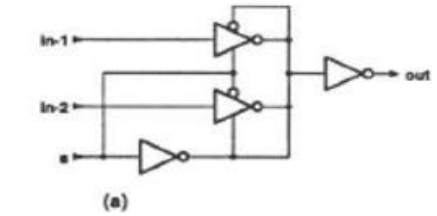
Answer:

Effects, as a result of scaling down- which eventually become severe enough to prevent further miniaturization.

- Substrate doping
- Depletion width
- Limits of miniaturization
- Limits of interconnect and contact resistance
- Limits due to sub threshold currents
- Limits on logic levels and supply voltage due to noise
- Limits due to current density

b. Explain Structured Design Approach – Regularity with example. (10)

Answer:



2-input MUX

DFF

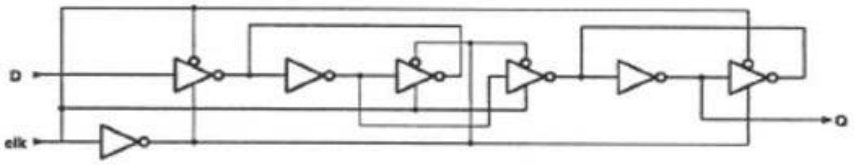


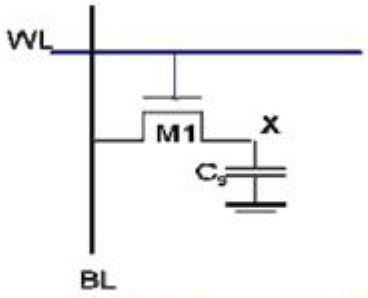
Figure5-.Structured Design Approach –Regularity

- Design of array structures consisting of identical cells.-such as parallel multiplication array.
- Exist at all levels of abstraction:
  transistor level-uniformly sized.
  logic level- identical gate structures
- 2:1 MUX, D-F/F- inverters and tri state buffers
- Library-well defined and well-characterized basic building block.
- Modularity: enables parallelization and allows plug-and-play
- Locality: Internals of each module unimportant to exterior modules and internal details remain at local level.

Q.6 a. Write the circuit of one transistor dynamic RAM cell and explain briefly read and write functions. (10)

Answer:

Circuit diagram



1T Dynamic RAM Cell

Working

- Row select (RS) = high, during write from R/W line Cm is charged
- data is read from Cm by detecting the charge on Cm with RS = high
- cell arrangement is bit complex.
- solution: extend the diffusion area comprising source of pass transistor, but Cd<<< Cgchannel
- another solution : create significant capacitor using poly plate over diffusion area.
- Cm is formed as a 3-plate structure
- with all this careful design is necessary to achieve consistent readability

Dissipation

- no static power, but there must be an allowance for switching energy during read/write

b. Explain the optimization of CMOS Inverters. (8)

Answer:

10.1.1 Optimization of nMOS and CMOS Inverters*

The approximate calculations presented here should be useful from a qualitative point of view and are intended to give the reader some appreciation of basic CMOS and nMOS circuit optimization problems.

For a more rigorous treatment of circuit optimization methods, refer to the articles cited at the end of the chapter.

10.1.1.1 The CMOS inverter

The area of a basic CMOS inverter is proportional to the total area occupied by the p- and n-devices.

$$A \propto (W_p L_p + W_n L_n)$$

where

W_p = width of the p-device
L_p = length of the p-device
W_n = width of the n-device
L_n = length of the n-device

Minimum area can be achieved by choosing minimum dimensions for W_p, L_p, W_n and L_n, that is

$$W_p = L_p = W_n = L_n = 2\lambda \text{ (minimum)}$$

Hence

$$\frac{W_p}{W_n} = 1$$

*The authors are indebted to Professor K.S. Trivedi of Duke University for providing this material on inverter optimization.

Switching power dissipation, P_{sd}, can be approximated by $C_L V_{DD}^2 f$ where

C_L = load capacitance at the inverter output
V_{DD} = power supply voltage
f = frequency of switching

For fixed V_{DD} and f, minimizing P_{sd} requires minimizing C_L which can be achieved by minimizing the area A since C_L is proportional to the gate areas comprising A.

Asymmetry in rise and fall times, t_r and t_f (transition times between 10% and 90% logic levels), can be equalized by using $\beta_n = \beta_p$. (Notice that t_r and t_f are proportional to the average resistance of the device which is approximately given by $\frac{2}{\beta V_{DD}}$ where $\beta = \beta_n$ or β_p). This requires tha

$$\frac{W_p}{L_p} = \left(\frac{\mu_n}{\mu_p}\right)\frac{W_n}{L_n}$$

to compensate for the lower hole mobility μ_p, compared to electron mobility μ_n.

Assuming $L_p = L_n = 2\lambda$, $\frac{\mu_n}{\mu_p} \doteq 2$, we require $\frac{W_p}{W_n} \doteq 2$. This yields $t_r = t_f$.

Note that equalizing rise and fall times is not possible in nMOS or pseudo-nMOS inverters because of the ratio requirement.

Asymmetry in noise margins, NM_H and NM_L, can be equalized by choosing $\beta_n = \beta_p$ and hence $\frac{W_p}{W_n} \doteq 2$ for $L_p \simeq L_n$. This yields $NM_H = NM_L$. (See Figure 10.4(b).)

Basic inverter pair delay—Consider a basic inverter pair shown in Figure 10.2 where C_L is the capacitive load driven by the two identical inverters, inverter pair delay $D(= t_r + t_f)$ is proportional to $(R_p + R_n)C_L$ where $R_p = 2/(\beta_p V_{DD})$ and $R_n = 2/(\beta_n V_{DD})$ are the average resistances of the p- and n-transistors respectively.

lso

$$C_L = C_E + (W_p L_p + W_n L_n)C_g$$

where

C_E = lumped parasitic capacitance
C_g = gate capacitance per unit area

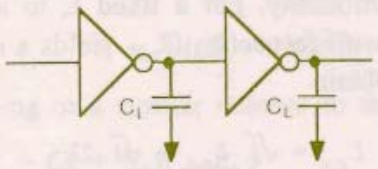


FIGURE 10.2 Inverter pair.

Hence

$$D = D_0\left[\left(\frac{2}{\beta_p V_{DD}} + \frac{2}{\beta_n V_{DD}}\right)(C_E + (W_p L_p + W_n L_n)C_g)\right]$$

where D_0 is a constant of proportionality. Assuming $\frac{\mu_n}{\mu_p} \doteq 2$

$$D = D_0\left[C_E\left(\frac{2L_p}{W_p} + \frac{L_n}{W_n}\right) + C_g\left(2L_p^2 + 2L_pL_n\frac{W_n}{W_p} + L_pL_n\frac{W_p}{W_n} + L_n^2\right)\right]$$

Since D increases with L_n and L_p, for minimum D choose $L_n = L_p = 2\lambda$ (minimum). Minimizing D with respect to W_p yields a solution

$$W_p/W_n = \sqrt{2}\left[1 + \frac{C_E}{C_g L_n W_n}\right]^{1/2}$$

$$W_p/W_n \doteq \sqrt{2} \text{ for } C_E \ll C_g L_n W_n \text{ (normal case)}$$

However, D does not vary significantly with W_p/W_n in the range $1 \le \frac{W_p}{W_n} \le 2$ (see Figure 10.3). Hence simultaneous optimization of various parameters mentioned above seems to be easily achievable in the CMOS inverter, without greatly increasing the delay D.

Q.7 a. Explain different aspects of CAD Design Tools. (8)

Answer:

10.12 ASPECTS OF DESIGN TOOLS

10.12.1 Graphical Entry Layout

Textual entry of layouts was at one time quite widely used and special textual entry editors are in existence and may well be used for small subsystem layout. However, such tools have been virtually swept aside by a much more convenient and highly interactive method of producing layouts for which monochrome or color graphics terminals are used, and on which the layout is built up and displayed during the design process. Such systems are mostly

'menu driven', in that menus of possible actions at various stages of the design are displayed on the screen beside the display of the current layout detail. Some form of cursor allows selection and/or placement of geometric features, etc., and the cursor may also allow selection of menu items or, alternatively, these may also be selected from a keyboard. Positioning of the cursor may be effected from the keyboard in simple systems and/or cursor position may be controlled from a bitpad digitizer or from a 'mouse', etc.

Two of the earliest available graphical entry layout packages were KIC developed at the University of California, Berkeley, and PLAN, originally developed at the University of Adelaide. PLAN makes use of low-cost monochrome, well as color, graphics terminals and is marketed by Integrated Silicon Design Pty Ltd, Adelaide. The use of an early version of PLAN to generate layouts illustrated in Figures 10.21 to 10.25 and it is hoped that the inclusion of these figures, which show various stages of design, is sufficient to convey an idea of the nature of the layout process using this class of software tools.

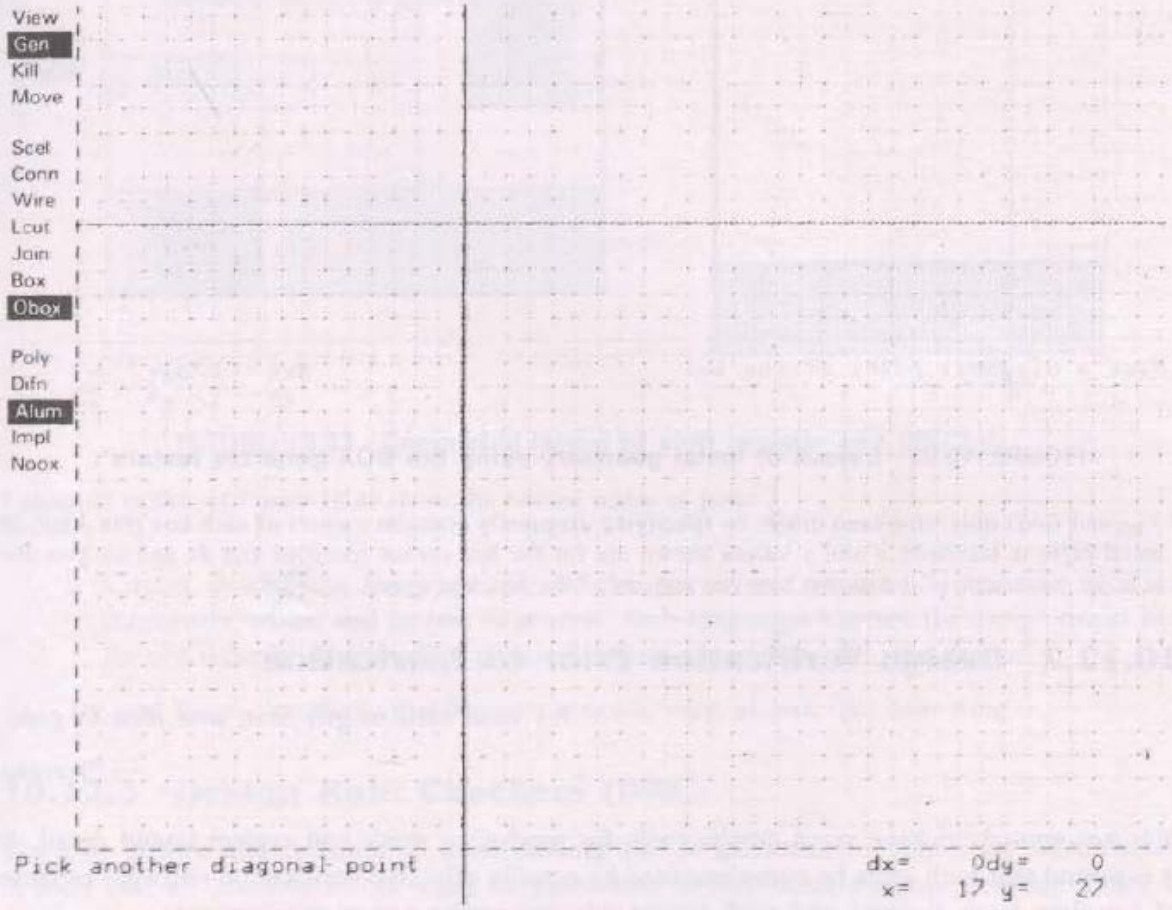


FIGURE 10.21 Basic PLAN design environment.*

* Figure shows λ grid, cross hair cursor, and menu (selected items in inverse video). x and y values of current or previous cursor position may also be displayed as shown. OBOX is selected to establish an outline (bounding) box. Then a name, (SRCL), is allocated to the enclosed cell.

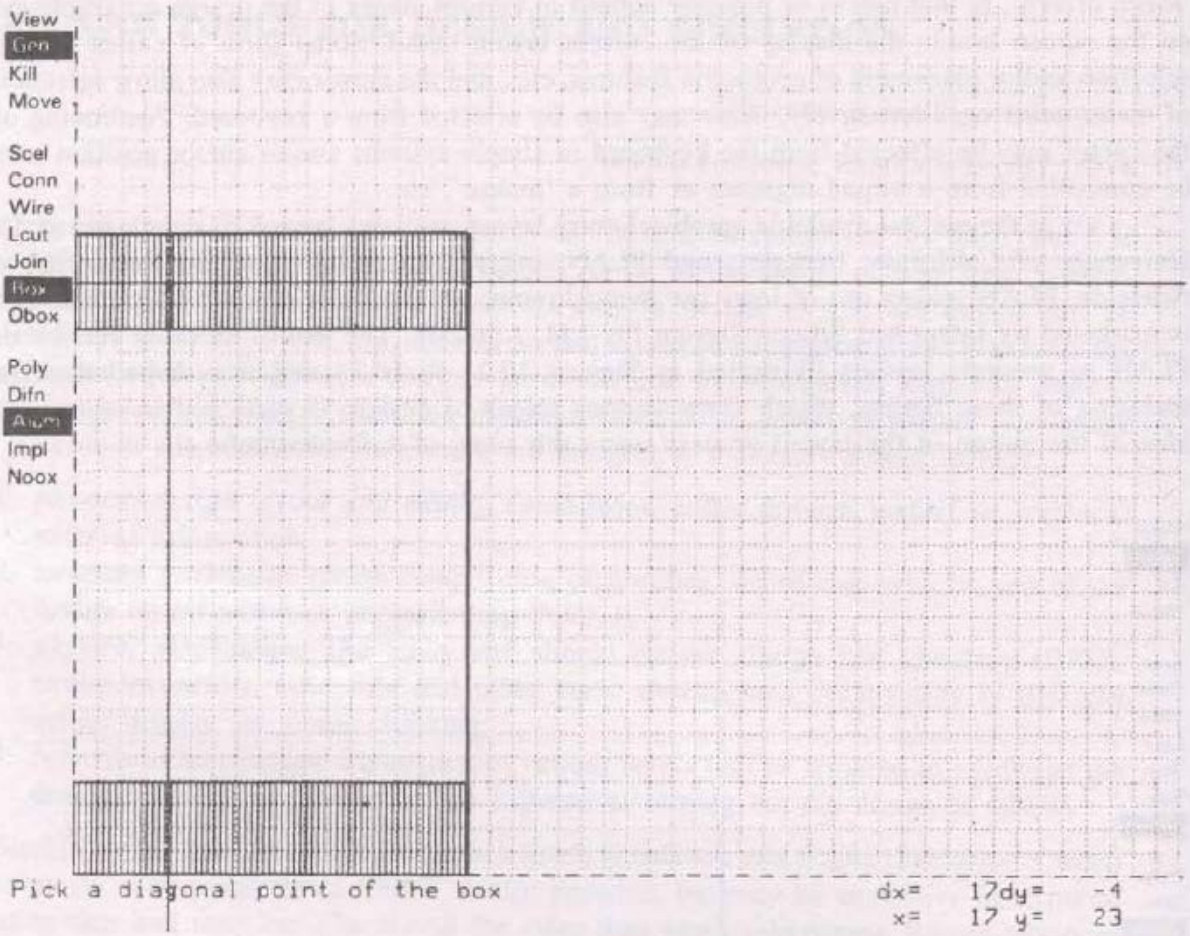


FIGURE 10.22 Layout of metal geometry using the BOX generate feature*.

* V_{DD} and *GND* rails have been drawn by specifying diagonally opposite corners of each box (the Alum or metal layer is selected). *x* and *y* values shown are for the last corner specified and *dx* and *dy* give the relative movement of the cursor between corners of the last box drawn.

10.12.2 Design Verification Prior to Fabrication

Try your skill in gilt first, and then in gold.

— PROVERB

It is not enough to have good design tools for producing mask and system layout detail. It is essential that such tools be complemented by equally effective verification software capable of handling large systems and with reasonable computing power requirements.

The nature of the tools required will depend on the way in which an integrated circuit design is represented in the computer. Two basic approaches are:

1. Mask level layout languages, such as CIF, which are well suited to physical layout description but not for capturing the design intent.

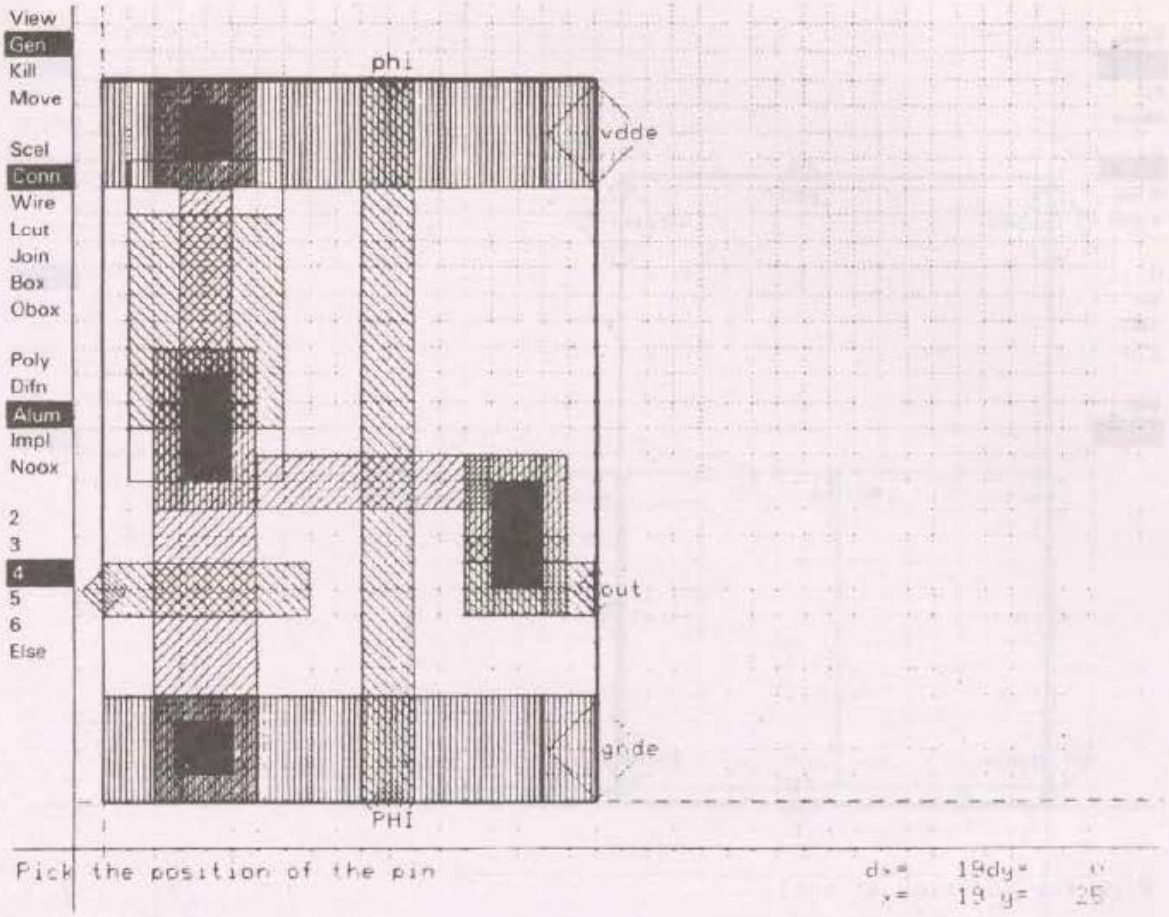


FIGURE 10.23 Completed layout of shift register cell (SRCL)*.

* Identical to that of Figure 10.20. Note the labeled nodes or pins.

2. Circuit description languages where the primitives are circuit elements such as transistors, wires, and nodes. In general, such languages capture the design intent but do not directly describe the physical layout associated with the design.

By and large, therefore, the designer's needs may include the following.

10.12.3 Design Rule Checkers (DRC)

The cost in time and facilities in mask-making and in fabricating a chip from those masks is such that all possible errors must be eliminated before mask-making proceeds. Once a design has been turned into silicon there is little that can be done if it doesn't work.

The wise designer will check for errors at all stages of the design, namely:

1. at the pencil and paper stage of the design of leaf-cells;
2. at the leaf-cell level once the layout is complete (e.g. when the CIF code for that leaf-cell has been generated);

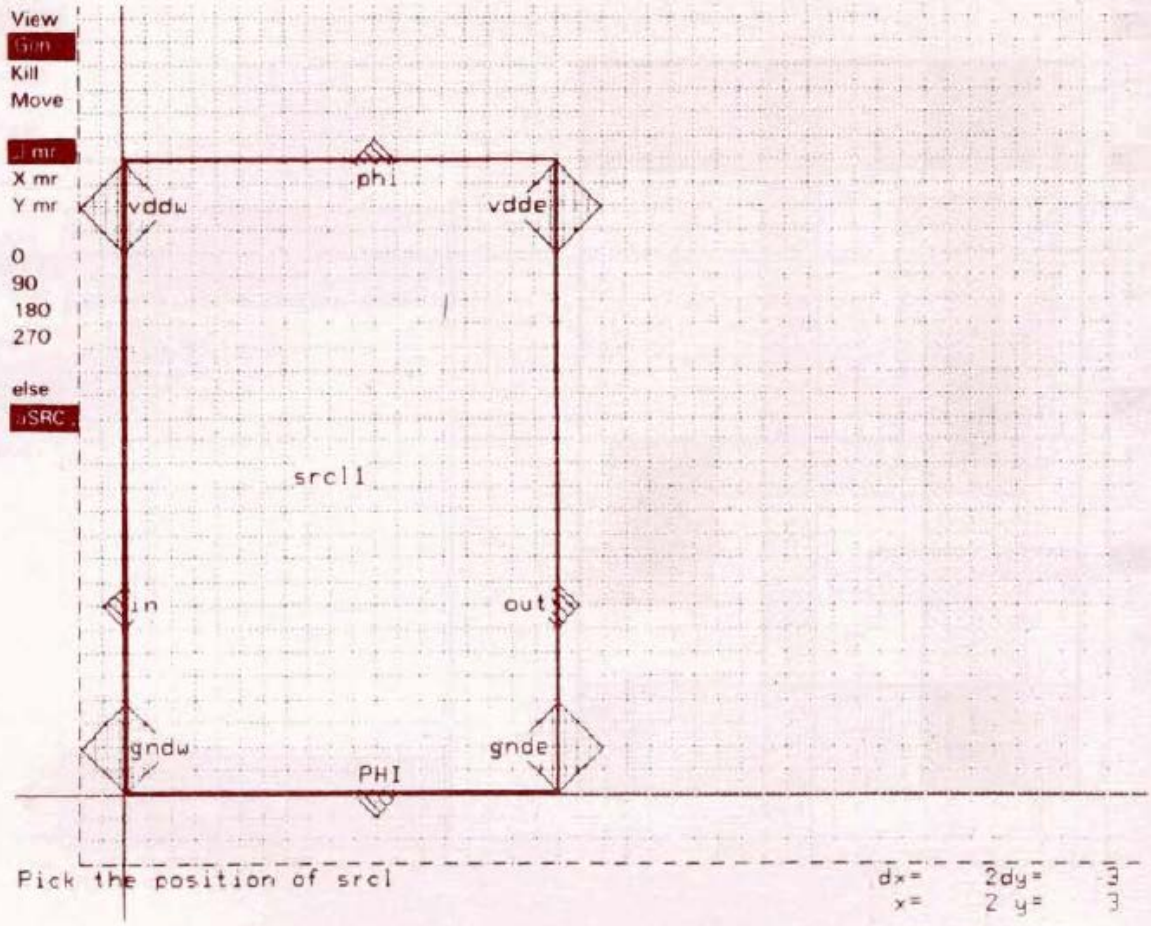


FIGURE 10.24 Bounding (outline) box representation of SRCL*.

* From now on, SRCL may be instanced from the SCEL item on the previous menu and placed as required as shown. Note that the cell is shown now as a bounding box with pins.

3. at the subsystem level to check that butting together and wiring up of leaf-cells is correctly done;
4. once the entire system layout has been completed.

The nature of physical layout verification 'design rule checking (DRC)' software may depend on whether the design rules are absolute or lambda-based, or on whether or not the layout is on a fixed or virtual grid.

A number of DRC programs, based on various algorithms, are available to the designer (e.g. the CHECK program from Integrated Silicon Design Pty Ltd),

10.12.4 Circuit Extractors

If design information exists in the form of physical layout data (as in CIF code form), then a circuit extractor program which will interpret the physical layout in circuit terms is required.

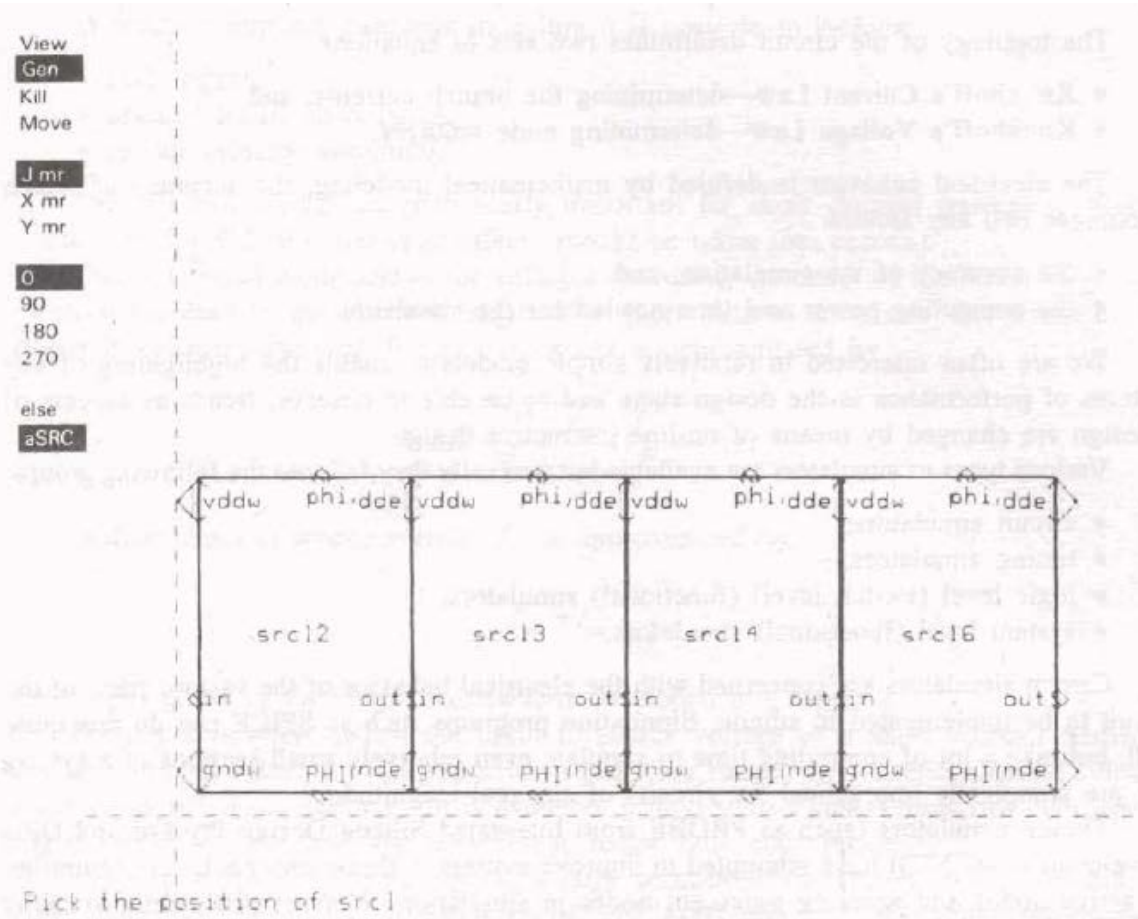


FIGURE 10.25 Instancing SRCL to form a register*.

* Several instances of SRCL may be set out as shown to form a complete register (2-bits only shown) and a bounding box, and a name can be given to the whole structure.

Although the designer could use the extracted data to check against his or her design intent, it is normally fed directly into a simulator so that the computer may be used to interpret the findings of the extractor. (An example of a circuit extractor program is NET from Integrated Silicon Design Pty Ltd.)

10.12.5 Simulators

In this section we very briefly consider the important topic of simulation prior to the VLSI design being committed to silicon.

From mask layout detail it is possible to extract a circuit description in a form suitable for input to a simulator. Programs that do this are referred to as circuit extractors. The circuit description contains information about circuit components and their interconnections. This information is subsequently transfonned by the simulator into a set of equations from which the predictions of behavior are made.

In order to improve transistor modeling it is possible to include:

- body effect;
- channel length modulation;
- carrier velocity saturation.

The last two effects are particularly important for short channel transistors, that is, channel lengths ≤ 3 μm, and their effects should be taken into account.

Channel length modulation—for voltages exceeding the onset of saturation there is an effective decrease in the channel length of a short channel transistor. For example, the change in channel length ΔL for an n-transistor is approximated by

$$\Delta L = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{qN_A}(V_{ds} - V_t)}$$

The resultant drain to source current I'_{ds} is approximated by

$$I'_{ds} = I_{ds}\frac{L}{\Delta L}$$

where I_{ds} is given by the simple expressions developed in Chapter 2.

Velocity saturation—when the drain to source voltage of a short channel transistor exceeds a critical value, the charge carriers reach their maximum scattering limited velocity before pinch off. Thus, less current is available from a short channel transistor than from a long channel transistor with similar width to length ratio and processing.

Logic level simulators can cope with large sections of the layout at one time but, of course, the performance is assessed in terms of logic levels with no or little timing information. However, there may be large sections of a system which can be satisfactorily dealt with and verified this way, provided that leaf-cell elements have been subjected to a more rigorous treatment.

When considering complete systems, logic simulators may be replaced by simulators which operate at the register transfer level. In all cases, the designer should carefully consider the availability of all such tools when choosing VLSI design software.

b. Explain Advantages & Disadvantages of implementing BIST include. (10)

Answer:

Advantages of implementing BIST include:

1) Lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated
2) Better fault coverage, since special test structures can be incorporated onto the chips
3) Shorter test times if the BIST can be designed to test more structures in parallel
4) Easier customer support and
5) Capability to perform tests outside the production electrical testing environment. The last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

Disadvantages of implementing BIST include:

1) Additional silicon area and fab processing requirements for the BIST circuits
2) Reduced access times
3) Additional pin (and possibly bigger package size) requirements, since the BIST circuitry need a way to interface with the outside world to be effective and
4) Possible issues with the correctness of BIST results, since the on-chip testing hardware itself can fail.

TEXT BOOK

I. Kang S. M. and Leblebici, Y. "CMOS Digital Integrated Circuit: Analysis and Design", Mc.Graw Hill, 1996
II. S. M. Sze, "Semiconductor Devices", 2nd Edition, John Wiley & Sons, 2002