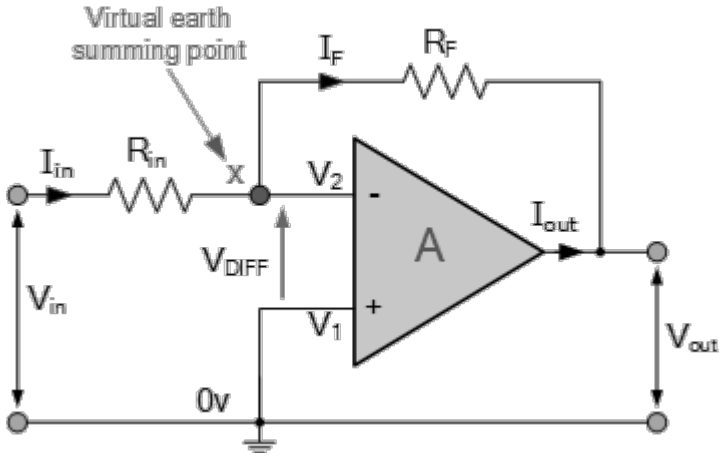
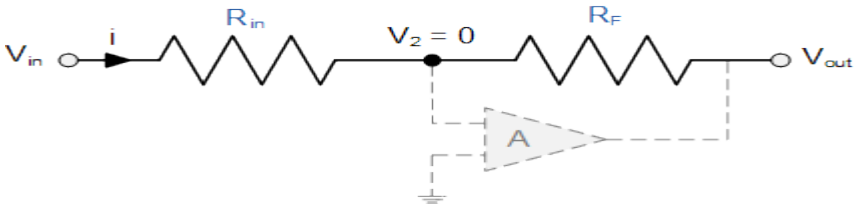
Q.2 a. Draw the inverting Operational amplifier and derive the expression for the voltage gain. (10)

Answer:

Inverting Operational Amplifier Configuration



Current (i) flows through the resistor network as shown.



$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

$$\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

b. Explain the ideal characteristics of operational amplifier. (6)

Answer:
ideal characteristics of operational amplifier

Infinite input impedance
Zero output impedance
Zero common-mode gain
infinite common-mode rejection
Infinite open-loop gain A
Infinite bandwidth.

Q.3 a. Define slew rate, input offset voltage, input bias current and input offset current of the operational amplifier. (8)

Answer:

(i) Slew Rate:- It is defined as the maximum rate at which the output voltage of an OPAMP can change It is expressed in V per μ sec. For μA741, \slew rate (S) = 0.5 V/μ sec. It is a large signal phenomenon and occurs mainly due to the input stage of the OPAMP going into saturation. This happens when a relatively large signal is applied at the input terminals (signal > 2VT in magnitude).

(ii) Input offset voltage:- Due to mismatch in the 2 transistors forming the differential stage of the input part of an OPAMP, a slight output voltage appears even when the applied input is 0. This output voltage divided by the closed loop gain of the OPAMP gives a voltage corresponding to the input terminals which when balanced by an equal & opposite voltage would lead to the output voltage being 0. This voltage is termed as input offset voltage.

(iii) Input bias current:- The base currents of the two transistors constituting the differential input stage of an OPAMP are termed as input bias currents.

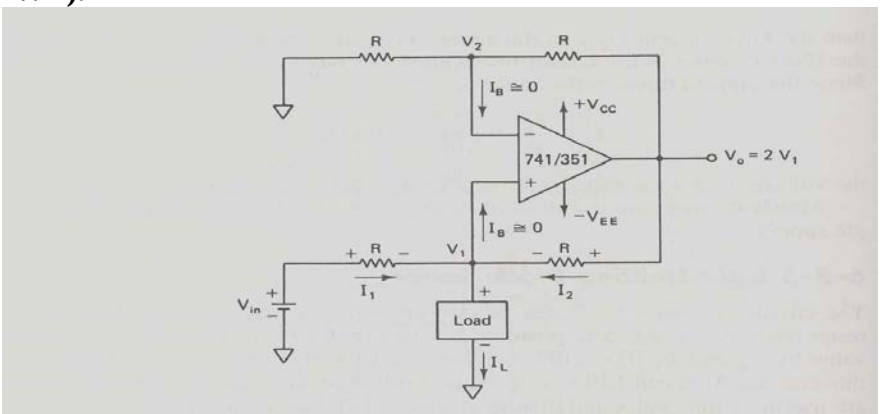
(iv) Input offset current:-

Due to mismatch in 2 input transistors, the base currents are not same. This mismatch in base current leads to an output offset voltage being developed. The difference in the base currents of the two input transistors is termed as input offset current**.**

b. Draw and explain the voltage to current converter circuit using operational amplifier. (8)

Answer:

The concept of the voltage-to-current converter may seem quite radical at first because, in general, everyone agrees that if a resistance increases then the current naturally decreases (I=V/R).



But with the voltage to current converter, an increase or decrease in the load resistance has nothing to do with the amount of current flowing through it. The non-inverting input (V+=V_1 in the figure) will change with the load resistance, but the current through the load will change only according to V_{in} and/or R. See the KCL analysis below: [3,5]

$$\frac{V_{out}-V-}{R}=\frac{V-}{R} \quad \rightarrow \quad V_{out} = 2V- = 2V+ = 2V_1$$

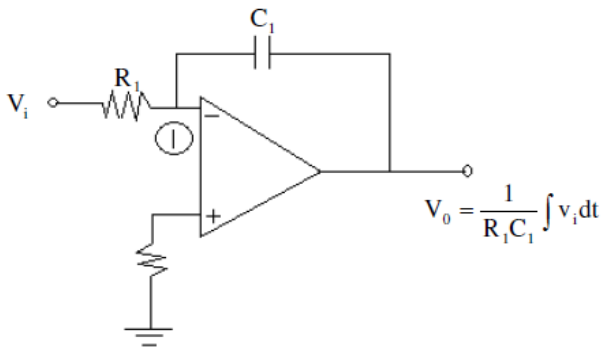
$$\frac{V_{in}-V+}{R}+\frac{V_{out}-V+}{R}=\frac{V+}{R_{load}}$$

Substituting 2V+ for V_{out} we get,

$$\frac{V_{in}}{R}=\frac{V+}{R_{load}}=I_{load} \qquad [3,5]$$

Q.4 a. Draw and explain the ideal integrator circuit by deriving the suitable expression. (8)

Answer:



The circuit shown realizes the mathematical operation of integration.

Writing modal equation at node (1)

$$\frac{v_i}{R_1}+C_1\frac{dv_o}{dt}=o \;\; or \;\; \frac{dv_o}{dt}=-\frac{1}{R_1C_1}v_i$$

Integrating both sides

$$\int_0^t dv_o=-\frac{1}{R_1C_1}\int_o^t v_i\,dt$$

$$v_o(t)=-\frac{1}{R_1C_1}\int_o^t v_i(t)\,dt+v_o(0)$$

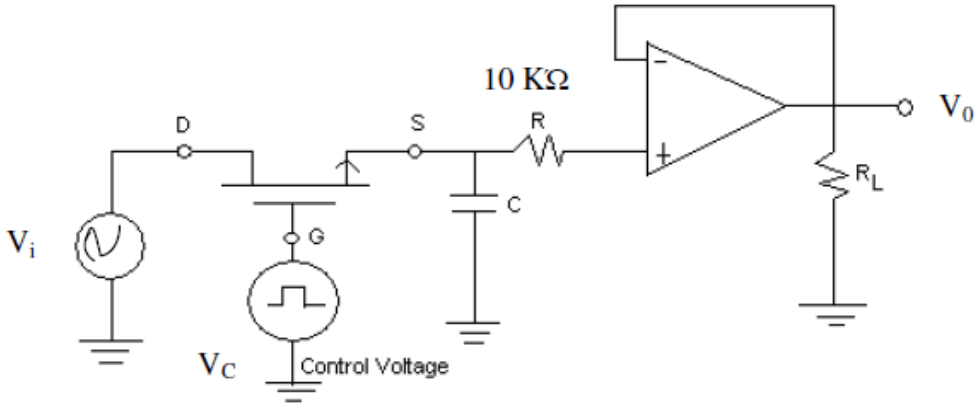
Where $\mathbf{v_o(0)}$ is the initial voltage on $\mathbf{C_1}$ therefore this is initial output voltage.

This circuit provides an output voltage that is proportional to integration of the input voltage with $\mathbf{v_o}$ being the initial condition of integration and $\mathbf{C_1R_1}$ the integration time constant.

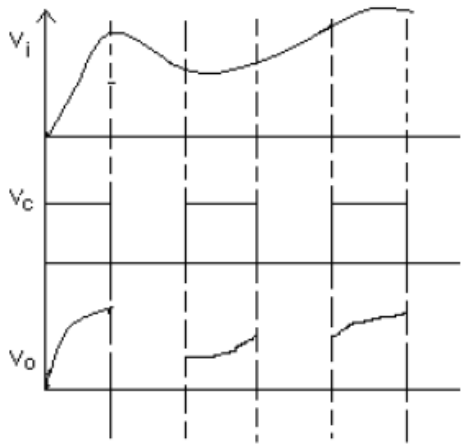
When $\mathbf{v_i = 0}$ the above integrator works as an open loop amplifier. This is because the capacitor $\mathbf{C_1}$ acts as an open circuit ($\mathbf{X_{C1}} = \infty$) to the input offset voltage $\mathbf{v_{io}}$. Thus the input offset voltage v_{io} and the part of input current charging capacitor $\mathbf{C_1}$ produces the error voltage at the output of the integrator. Therefore, in the practical integrator to reduce the error voltage at the output, a resistor R_F is connected in parallel to capacitor $\mathbf{C_1}$.

b. Explain the operation of sample & hold circuit. Discuss its applications. (8)

Answer:



Here, the MOSFET is used as a switch and OPAMP as a buffer. The switch is put on by applying a positive pulse on the gate. The capacitor gets charged with the required value with RC time constant. Sample & hold circuit can be used to produce samples of analog voltage which can be used in a analog to digital converter (ADC). The input voltage V_i to be sampled is applied at the drain. When control voltage is high MOSFET is ON and capacitor is charged up to the value of input signal, and the same voltage is available at the output. When Vc is zero the MOSFET is OFF and acts as open circuit. The only discharge path of capacitor is through OPAMP. However the input impedance of voltage follower is very high, hence the voltage across capacitor is retained.



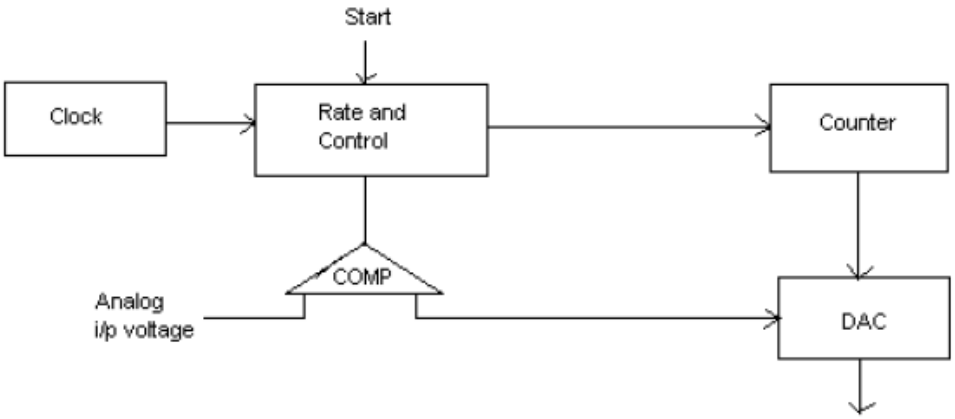
WAVEFORMS

Q.5 a. What is an ADC? Draw the schematic of an ADC that uses a binary counter and explain its operation. (8)

Answer:

A counter based ADC uses a simple binary counter. The digital output signals are taken from this counter ('n' bit) where 'n' is the desired number of bits. The output of counter is connected to a DAC. If clock is applied to the counter, the output of DAC is a stair-case waveform. This waveform is exactly the reference

voltage signal for the comparator. First the counter is reset to all 0's. Then, when a convert signal appears, the gate opens and allows the pulses to the counter. The staircase wave form is produced by the DAC. When the reference voltage exceeds the input analog voltage, the gate is closed, the counter stops and conversion is complete. The number stored in the counter is the digital equivalent of analog input voltage. The counter based ADC provides a very good conversion method.

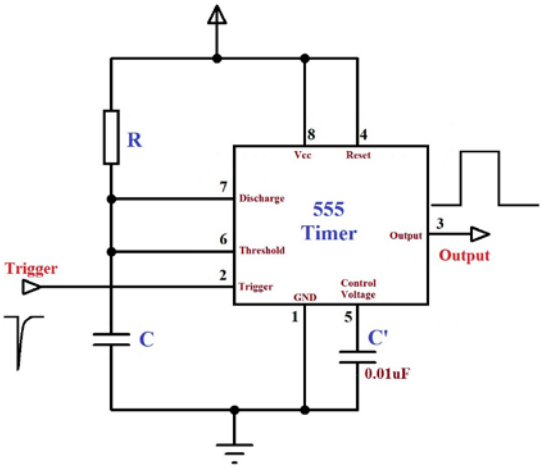


Counter Type ADC

b. Explain with suitable circuit diagram the working principle of monostable-multivibrator circuit operation using IC 555. (8)

Answer:

Monostable Multivibrator is also known as One Short Multivibrator. As its name indicates it has one stable state and it switches to unstable state for a predetermined time period T when it is triggered. The time period T is determined by the RC time constant in the circuit. Monostable mode of 555 Timer is commonly used for generating Pulse Width Modulated (PWM) waves.



This is the circuit diagram of 555 Timer wired in Monostable mode. 8th pin and 1st pin of the 555 timer are used to given power Vcc and Ground respectively. 4th pin is the Reset pin of 555 Timer, which is active low so it is connected to Vcc to avoid accidental resets. 5th pin is the Control Voltage pin used to provide external reference voltage to internal comparators. Since it is not used here, it is grounded via a capacitor C' (0.01µF) to avoid high frequency noises. When a negative trigger is applied on the Trigger input of 555, output goes high and capacitor starts

charging through resistor R. When the capacitor voltage becomes greater than 2/3 Vcc, ouput goes low and capacitor starts discharging through the Discharge pin of 555 Timer. Time period of the unstable state is given the tye expression, T = 1.1RC.

Working

The Monostable Multivibrator will be in its stable state (Output LOW) until it is triggered. When a negative trigger is applied to the Trigger pin of 555 Timer, output of lower comparator will become HIGH and output of upper comparator will be LOW, since the capacitor voltage is zero. This makes the output HIGH. The Discharge transistor turns OFF and the capacitor starts charges through resistor R to Vcc.

After the negative trigger, output of lower comparator becomes LOW and that of upper comparator remains LOW. Since both inputs of the SR Flip Flop are LOW, output will not change, so the output is HIGH.

PART B
Answer at least TWO questions. Each question carries 16 marks.

Q.6 a. Enlist the advantages of digital system over analog. (6)

Answer:

Advantages of digital system over analog.

1. Digital systems are generally easier to design
2. Information storage is easy.
3. Accuracy and precision are easier to maintain throughout the system.
4. Operation can be programmed.
5. Digital circuits are less affected by noise.
6. More digital circuitry can be fabricated on IC chips.

b. (i) What is the total range of decimal values that can be represented in eight bits?

(ii) How many bits are needed to represent decimal values ranging from 0 to 12,500? (4)

Answer:

(i) 2^8-1=255 decimal values.

(ii) With 13 bits, we can count from decimal 0 to 2^13 – 1 = 8191With 14 bits, we can count from 0 to 2^14 – 1 = 16383 Clearly, 13 bits aren't enough, but 14 bits will get us up beyond 12,500.Thus, the required number of bits is 14.

c. Make the following conversion (steps are necessary): (6)

(i) $(874)_{10}$ to BCD
(ii) 0110100000111001 (BCD) to its decimal equivalent.
(iii) $(2AF)_{16}$ to decimal

Answer:

(i)

8	7	4	(decimal)
↓	↓	↓	
1000	0111	0100	(BCD)

(ii)

Divide the BCD number into four-bit groups and convert each to decimal.

$$\underbrace{0110}_{6}\ \underbrace{1000}_{8}\ \underbrace{0011}_{3}\ \underbrace{1001}_{9}$$

(iii)

$$\begin{aligned} 2AF_{16} &= 2 \times 16^2 + 10 \times 16^1 + 15 \times 16^0 \\ &= 512 + 160 + 15 \\ &= 687_{10} \end{aligned}$$

Q.7 a. Simplify the following : (6)

(i) $\overline{A}BCD + ACD$ **(ii)** $(\overline{A} + B)(A + B)$

Answer:

(i)

Solution

Factoring out the common variables CD, we have

$$x = CD(A + \overline{A}B)$$

Utilizing theorem (15a), we can replace $A + \overline{A}B$ by $A + B$, so

$$\begin{aligned} x &= CD(A + B) \\ &= ACD + BCD \end{aligned}$$

(ii)

Solution

The expression can be expanded by multiplying out the terms [theorem (13)]:

$$z = \overline{A} \cdot A + \overline{A} \cdot B + B \cdot A + B \cdot B$$

Invoking theorem (4), the term $\overline{A} \cdot A = 0$. Also, $B \cdot B = B$ [theorem (3)]:

$$z = 0 + \overline{A} \cdot B + B \cdot A + B = \overline{A}B + AB + B$$

Factoring out the variable B [theorem (13)], we have

$$z = B(\overline{A} + A + 1)$$

Finally, using theorems (2) and (6),

$$z = B$$

b. Minimize the logic function F (A, B, C, D) = $\sum m(1,3,5,8,9,11,15) + d(2,13)$ **using K-maps and realize using NAND gates. (10)**

Answer:

Ans:

Minimization of the logic function F(A, B, C, D) = ∑ m(1,3,5,8,9,11.15) + d(2,13) using K-maps and Realization using NAND and NOR Gates

(i) Karnaugh Map for the logic function is given in table 4.1

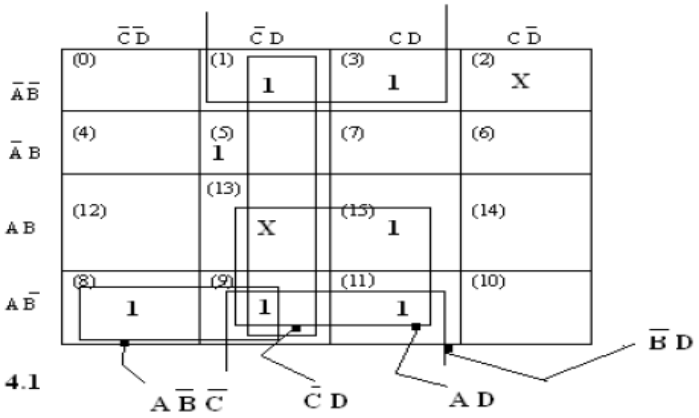
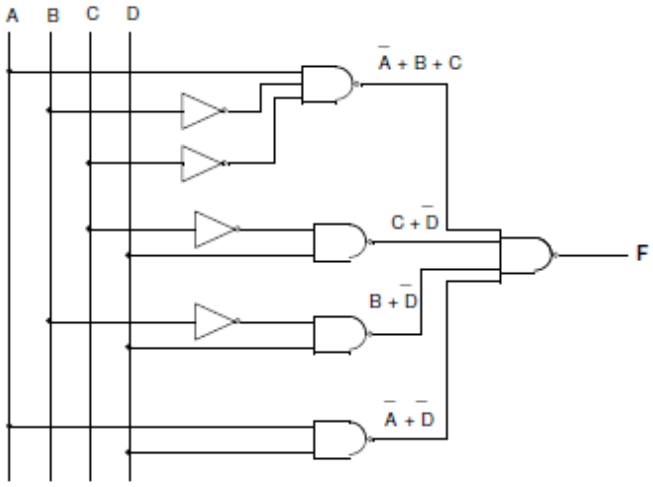


Table 4.1

The minimized logic expression in SOP form is F = A $\overline{B}$ $\overline{C}$ + $\overline{C}$D + $\overline{B}$D + AD

The minimized logic expression in POS form is F = (A + $\overline{B}$ + $\overline{C}$) ($\overline{C}$ +D) ($\overline{B}$ +D) (A+D)



Q.8 a. What is a half-adder? Explain a half-adder with the help of truth-table and logic diagram. (8)

Answer:

Half Adder: A logic circuit for the addition of two one-bit numbers is referred to as an half-adder. The addition process is illustrated in truth table. Here A and B are the two inputs and S (SUM) and C (CARRY) are two outputs.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the truth table, we obtain the logical expressions for S and C outputs as

$S = \overline{A}B + A\overline{B}$

$C = AB$

The logic diagram for an Half-adder using gates is shown in fig.6(a)

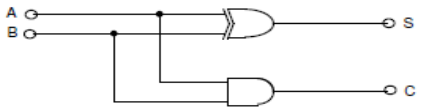


Fig.6(a) Logic Diagram for an Half-adder

b. What is a digital multiplexer? Illustrate its functional diagram. Write the scheme of a 4-input multiplexer using basic gates (AND/OR/NOT) and explain its operation. (8)

Answer:

Multiplexer: MUX or data selector is a logic circuit selects binary information from one of many input and directs it to a single output line. Selection of the particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and correspondingly n selection lines.

There are 4 inputs I_1 I_0 I_2 I_3 and two selection line S_0 and S_1. Depending upon the bit combination of S_0 and S_1 one of the input is transferred to the output. Basically there is a decoder circuit with one input for each bit of information and one OR gate connected to the output. If S_o, S_i = 00 ,then first AND gate will have the two inputs as one output will depend on I_0. At the same time outputs of all other AND gates are Zero.

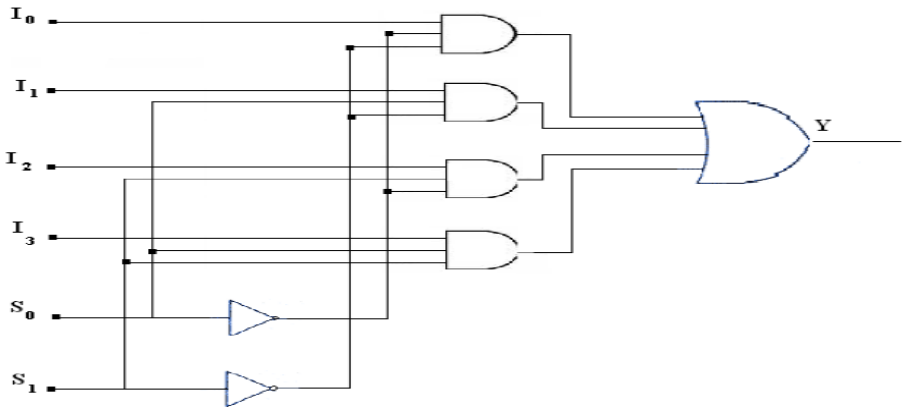
The multiplexer is a combinational circuit which is one of the most widely used standard circuit in digital design. It has N select lines 2^N inputs and a single output.

Multiplexer:-

$$Y = \overline{S}_1\overline{S}_0I_0 + \overline{S}_1S_0I_1 + S_1\overline{S}_0I_2 + S_1S_0I_3$$

Truth table of 4x1 Mux

Select inputs		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Circuit Diagram of 4 X 1 MUX using basic gate

Q.9 a. With the help of clocked JK flip flops and waveforms, explain the working of a three bit binary ripple counter. (8)

Answer:

3-Bit Binary Ripple Counter: In Ripple Counters, all the Flip-Flops are not clocked simultaneously and the flip-flops do not change state exactly at the same time. A 3-bit Binary Counter has maximum of 2^3 states i.e., 8 states, which requires 3 Flip-Flops. The word Binary Counter means a counter which counts and produces binary outputs 000,001,010--111.It goes through a binary sequence of 8 different states (i.e, from 0 to 7). Fig.8(a) shows the logic circuit of a 3-bit Binary Ripple Counter consisting of 3 Edge Triggered JK flip-flops. As indicated by small circles at the CLK input of flip-flops, the triggering occurs when CLK input gets a negative edge. Q_0 is the Least Significant Bit (LSB) and Q_2 is the Most Significant Bit (MSB). The flip-flops are connected in series. The Q_0 output is connected to CLK terminal of second flip-flop. The Q_1 output is connected to CLK terminal of third flip-flop. It is known as a Ripple Counter because the carry moves through the flip-flops like a ripple on water.

Working: Initially, CLR is made Low and all flip-flops Reset giving an output Q = 000. When CLR becomes High, the counter is ready to start. As LSB receives its clock pulse, its output changes from 0 to 1 and the total output Q = 001. When second clock pulse arrives, Q_0 resets and carries (i.e., Q_0 goes from 1 to 0 and, second flip flop will receive CLK input). Now the output is Q = 010. The third CLK pulse changes Q_0 to 1 giving a total output Q = 011. The fourth CLK pulse causes Q_0 to reset and carry and Q_1 also resets and carries giving a total output Q = 100 and the process goes on. The action is shown is Table 8.1.The number of output states of a counter are known as Modulus (or Mod). A Ripple Counter with 3 flip-flops can count from 0 to 7 and is therefore, known as Mod-8 counter.

Counter State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Table.8.1 Counting Sequence of a 3-bit Binary Ripple Counter

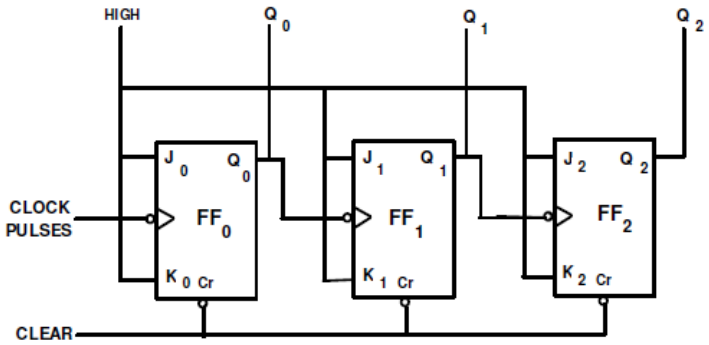


Fig.8(a) Logic Diagram of 3-Bit Binary Ripple Counter

Ripple counters are simple to fabricate but have the problem that the carry has to propagate through a number of flip flops. The delay times of all the flip flops are added. Therefore, they are very slow for some applications. Another problem is that unwanted pulses occur at the output of gates.

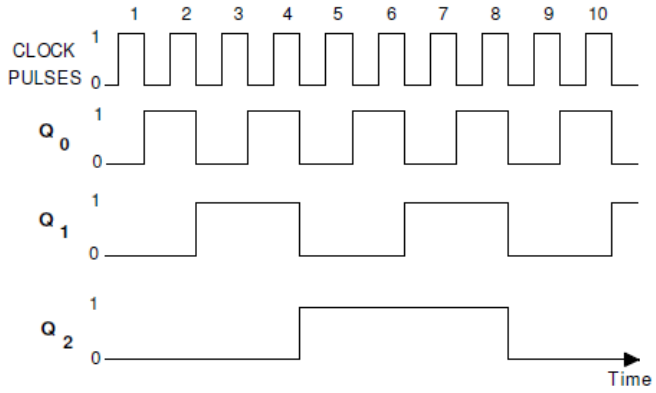


Fig.8(b) Timing Diagram of 3-bit Binary Ripple Counter

The timing diagram is shown in *Fig.8(b).* FF_0 is LSB flip flop and FF_2 is the MSB flip flop. Since *FF0* receives each clock pulse, Q_0 toggles once per negative clock edge as shown in Fig. 8*(b).*The remaining flip flops toggle less often because they receive negative clock edge from preceding flip flops. When Q_0 goes from 1 to 0, FF_1 receives a negative edge and toggles. Similarly, when Q_1 changes from 1 to 0, FF_2 receives a negative edge and toggles. Finally when Q_2 changes from 1 to 0, FF_3 receives a negative edge and toggles. Thus whenever a flip flop resets to 0, the next higher flip flop toggles.
This counter is known as ripple counter because the 8th clock pulse is applied, the trailing edge of 8th pulse causes a transition in each flip flop. Q_0 goes from High to Low, this causes Q_1 go from High to Low which causes Q_2 to go from High to Low which causes Q_3

to go from High to Low. Thus the effect ripples through the counter. It is the delay caused by this ripple which result in a limitation on the maximum frequency of the input signal.

b. Using D-Flip flops and waveforms explain the working of a 4-bit SISO shift register. (8)

Answer:

Ans:

Serial In - Serial Out Shift Register: Fig.9(a) shows a 4 bit serial in - serial out shift register consisting of four D flip flops FF_0, FF_1, FF_2 and FF_3. As shown it is a positive edge triggered device. The working of this register for the data 1010 is given in the following steps.

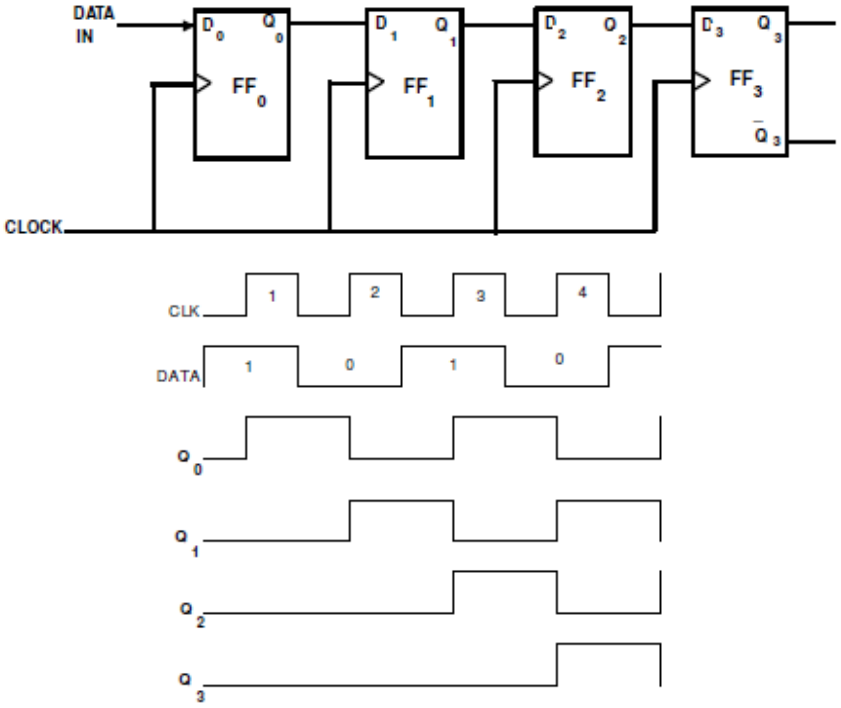


Fig.9(b) Output Waveforms of 4-bit Serial-in Serial-out Register

1. Bit 0 is entered into data input line. $D_0 = 0$, first clock pulse is applied, FF_0 is reset and stores 0.
2. Next bit 1 is entered. $Q_0 = 0$, since Q_0 is connected to D_1, D_1 becomes 0.
3. Second clock pulse is applied, the 1 on the input line is shifted into FF_0 because FF_0 sets. The 0 which was stored in FF_0 is shifted into FF_1.
4. Next bit 0 is entered and third clock pulse applied. 0 is entered into FF_0, 1 stored in FF_0 is shifted to FF_1 and 0 stored in $FF1$ is shifted to FF_2.
5. Last bit 1 is entered and 4th clock pulse applied. 1 is entered into FF_0, 0 stored in FF_0 is shifted to FF_1, 1 stored in FF_1 is shifted to FF_2 and 0 stored in $FF2$ is shifted to FF_3.

   This completes the serial entry of 4 bit data into the register. Now the LSB 0 is on the output Q_3.
6. Clock pulse 5 is applied. LSB 0 is shifted out. The next bit 1 appears on Q_3 output.
7. Clock pulse 6 is applied. The 1 on Q_3 is shifted out and 0 appears on Q_3 output.
8. Clock pulse 7 is applied. 0 on Q_3 is shifted out. Now 1 appears on Q_3 output.
9. Clock pulse 8 is applied. 1 on Q_3 is shifted out.
10. When the bits are being shifted out (on CLK pulse 5 to 8) more data bits can be entered in.

TEXT BOOK

I. Linear Integrated Circuits, Revised Second Edition, D Roy Choudhury, Shail B. Jain, New Age International Publishers

II. Digital Systems – Principles and Applications, Ninth Edition, Ronald J Tocci, Neal S Widmer and Gregory L. Moss, Pearson Education, 2008