Q.2 a. By using Norton's theorem, find the current in the load resistor R_L for the circuit shown in Fig.1. (8)

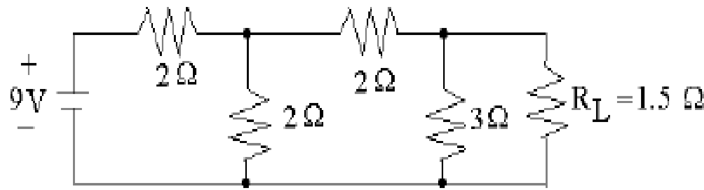
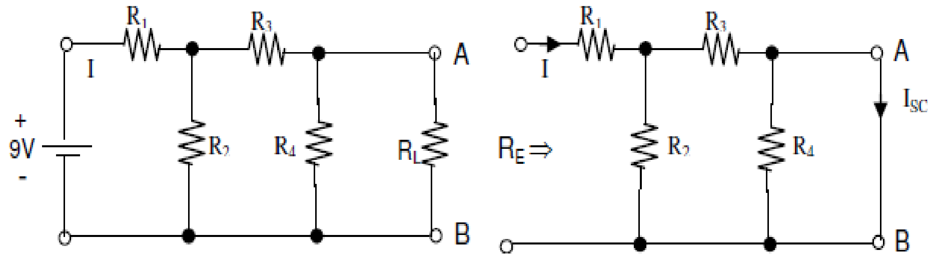


Fig.1

Answer:

Ans:

To find the short circuit current I_{sc}, first find the equivalent resistance from Fig

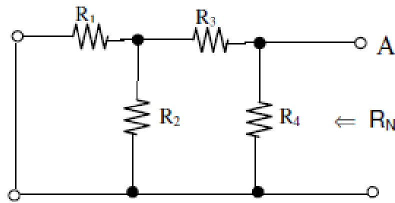


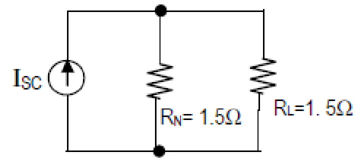
$$R_E = R_1 + \frac{R_2 R_3}{R_2 + R_3}, \qquad \text{Given } R_1 = 2\Omega, R_2 = 2\Omega, R_3 = 2\Omega, R_4 = 3\Omega, R_L = 1.5\Omega$$

$$= 2 + \frac{2\times 2}{4} = 2 + 1 = 3\Omega$$

$$\therefore I = \frac{V}{R_E} = \frac{9}{3} = 3 Amp.$$

$$\therefore \quad Short\ Circuit\ Current\ I_{sc} = I\left[\frac{R_2}{R_2 + R_3}\right] = 3\left[\frac{2}{2+2}\right] = \frac{6}{4} = 1.5 \text{ Amp.}$$





$$R_N = \frac{R_4\left[R_3 + \frac{R_2 R_1}{R_1 + R_2}\right]}{R_4 + R_3 + \frac{R_2 R_1}{R_1 + R_2}} = \frac{3\times(2 + \frac{2\times 2}{2+2})}{3 + 2 + \frac{2\times 2}{2+2}} = \frac{3\times 3}{6} = \frac{9}{6} = 1.5\Omega$$

$$I_L = I_{SC} \times \frac{R_N}{R_N + R_4} = \frac{1.5\times 1.5}{1.5 + 1.5} = 0.75 \text{Amp}$$

b. Explain Z parameters and also draw an equivalent circuit of the Z parameter model of the two port network. (8)

Answer:

In a Z parameter model, the voltage of the input port and the voltage of the output port are expressed in terms the current of the input port and the current of the output port. The equations are given by

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

When the output terminal is open circuited, $I_2 = 0$, we can determine Z_{11} and Z_{21}, where Z_{11} is the input impedance expressed in ohms and Z_{21} is the forward transfer impedance.

$$\left. \begin{aligned} V_1 &= Z_{11}I_1 \\ V_2 &= Z_{21}I_1 \end{aligned} \right|_{when\ I_2=0}$$

$Z_{11} = \frac{V_1}{I_1}$ ohms and $Z_{21} = \frac{V_2}{I_1}$ ohms

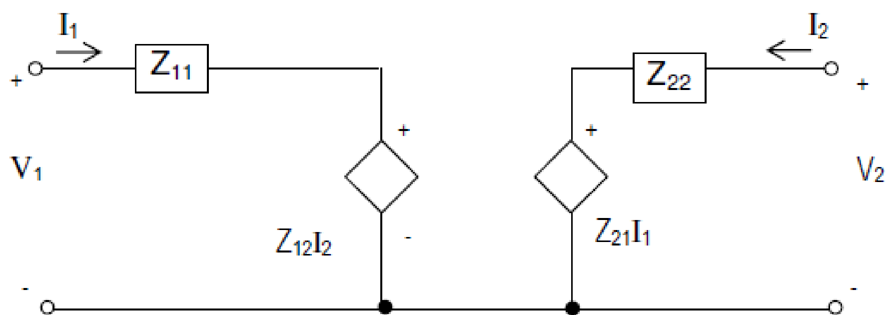
When the input terminal is open circuited, $I_1 = 0$, we can determine Z_{12} and Z_{22}, Where Z_{12} is the reverse transfer impedance and Z_{22} is the output impedance expressed in ohms.

$$\left. \begin{aligned} V_1 &= Z_{12}I_2 \\ V_2 &= Z_{22}I_2 \end{aligned} \right|_{when\ I_1=0}$$

$Z_{12} = \frac{V_1}{I_2}$ Ohms and $Z_{22} = \frac{V_2}{I_2}$ Ohms

The equivalent circuit of the Z parameter representation is shown in Fig 3.b

Where $Z_{12}I_2$ is the controlled voltage source and $Z_{21}I_1$ is the controlled voltage source.



Q.3 a. An AC supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ratio 5:1. Assume the diode is an ideal one. The load resistance is 300Ω. Find (a) dc output voltage (b) PIV (c) maximum value of power delivered to the load (d) average value of power delivered to the load. (8)

Answer:

Solution:

(a) The transformer secondary voltage = 230/5 = 46V.

Maximum value of secondary voltage,

$V_m = \sqrt{2}$ x 46 = 65V.

Therefore, dc output voltage, $V_{dc} = \frac{V_m}{\pi} = \frac{65}{\pi} = \mathbf{20.7\ V}$

(b) **PIV of a diode : V_m = 65V**

(c) **Maximum value of load current,**

$$I_m = \frac{V_m}{R_L} = \frac{65}{300} = \mathbf{0.217\ A}$$

Therefore, maximum value of power delivered to the load,

$\mathbf{P_m} = I_m^2 \text{ x } R_L = (0.217)^2 \text{ x } 300 = \mathbf{14.1W}$

(d) The average value of load current,

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300} = \mathbf{0.069A}$$

Therefore, average value of power delivered to the load,

$$\mathbf{P_{dc}} = I_{dc}^2 \text{ x } R_L = (0.069)^2 \text{ x } 300 = \mathbf{1.43W}$$

b. Define drift and diffusion current in PN junction diode. (4)

Answer:

Drift current: When an electric field is applied across the semiconductor, the holes move towards the negative terminal of the battery and electron move towards the positive terminal of the battery. This drift movement of charge carriers will result in a current termed as drift current.

Diffusion current: A concentration gradient exists, if the number of either electrons or holes is greater in one region of a semiconductor as compared to the rest of the region. The holes and electron tend to move from region of higher concentration to the region of lower concentration. This process in called diffusion and the current produced due this movement is diffusion current.

c. For PN diode, the reverse saturation current at a bias of 20V is 20nA. It is 5μA at 75 volts. Calculate DC resistances at these points. (4)

Answer:

Solution: -

DC resistance $R_D = \frac{V_D}{I_D}$

Case (i)

$V_D = -20$ V, $I_D = -20$nA.

$$R_D = \frac{V_D}{I_D} = \frac{-20}{-20 \times 10^{-9}} = 10^9 \Omega = 1000 M\Omega$$

Case (ii)

$V_D = -75$V, $I_D = -5\mu A$

$$R_D = \frac{V_D}{I_D} = \frac{-75}{-5 \times 10^{-6}} = 15 \times 10^6 = 15 M\Omega$$

Q.4 a. Compare common emitter, common base and common collector configurations of amplifier. (6)

Answer:

Characteristic	Common Base	Common Emitter	Common Collector
Input impedance	Low	Medium	High
Output impedance	Very High	High	Low
Phase Angle	0°	180°	0°
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

b. Explain the construction of Enhancement MOSFET with neat diagrams and also draw the output or drain characteristics. (10)

Answer:

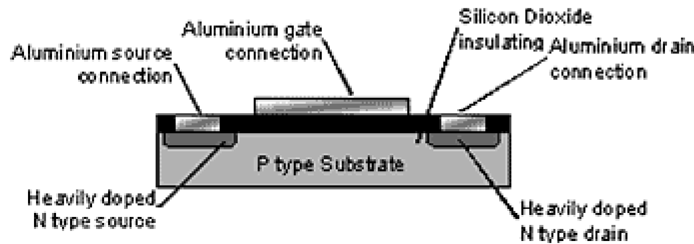
Enhancement Mode MOSFET

The Metal Oxide Silicon FET (MOSFET) or Metal Oxide Silicon Transistor (M.O.S.T.) has an even higher input resistance (typically 1012 to 1015 ohms) than that of the JFET. In this device the gate is completely insulated from the rest of the transistor by a very thin layer of metal oxide (Silicon dioxide SiO2). Hence the general name applied to any device of this type, the IGFET or Insulated Gate FET.

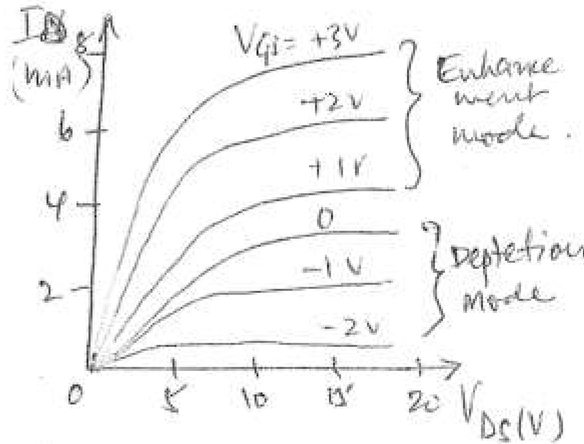
Construction

The layers are laid down one by one, by diffusing various semiconductor materials with suitable doping levels and layers of insulation into the

surface of the device under carefully controlled conditions at high temperatures. Parts of a layer may be removed by etching using photographic masks to make the required pattern of the electrodes etc. before the next layer is added. The insulating layers are made by laying down very thin layers of silicon dioxide; conductors are created by evaporating a metal such as aluminum on to the surface. The transistors produced in this way have a much higher quality than is possible using other methods, and many transistors can be produced at one time on a single slice of silicon, before the silicon slice is cut up into individual transistors or integrated circuits.

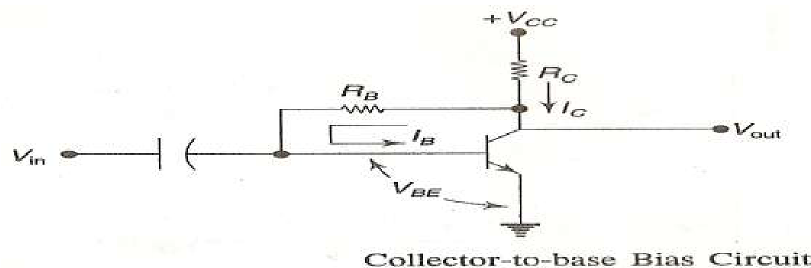


Output characteristics of E-MOSFET



Q.5 a. Explain collector to base bias or collector feedback biasing method in detail and discuss the stability of the circuit. (8)

Answer:



Collector-to-base Bias Circuit

$V_{CE} = I_B R_B + V_{BE}$

- $I_B = \left(\dfrac{V_{CE} - V_{BE}}{R_B} \right)$

- If the collector current increases due to increase in temperature or the transistor is replaced by one with higher β, the voltage drop across R_C increases.

- So, less V_{CE} and less I_B, to compensate increase in Ic i.e., greater stability

$$V_{CC} = I_B + I_C \;\; R_C + I_B R_B + V_{BE} \qquad - \qquad (1)$$

$$= I_B R_C + I_C R_C + I_B R_B + V_{BE}$$

$$= I_B \;\; R_C + R_B \;\; + I_C R_C + V_{BE}$$

Or $$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{RC + RB} \qquad - \qquad (2)$$

$$\frac{d_{IB}}{d_{IC}} = \frac{R_C}{R_C + R_B} \qquad - \qquad (3)$$

Stability Factor:

$$S = \frac{1+\beta}{1-\beta\left(\dfrac{dI_B}{dI_C}\right)}$$

Putting the value of dI_B / dI_C from equation (3)

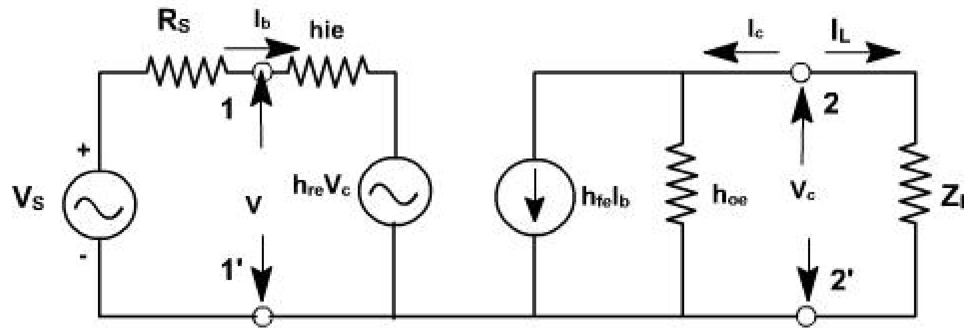
$$S = \frac{1+\beta}{1-\beta\left(\dfrac{-R_C}{R_C+R_B}\right)} = \frac{1+\beta}{1+\beta\left(\dfrac{R_C}{R_C+R_B}\right)}$$

Note: 1) Value of S is less than that of fixed bias (which is S = 1+β)

2. S can be made small and stability improved by making R_B small or R_C large.
If Rc is small S = 1 + β, i.e., stability is poor.

b. Draw the h parameters model of common emitter and derive the expression for current gain. (8)

Answer:



Current gain: For the transistor amplifier stage, Ai is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_b} = \frac{-I_C}{I_b} \qquad (I_L + I_c = 0. \quad \therefore I_L = -I_c)$$

$$I_C = h_{fe} I_b + h_{oe} V_c$$

$$V_c = I_L Z_L = -I_c Z_L$$

$$\therefore I_c = h_{fe} I_b + h_{oe} (-I_c Z_L)$$

$$\text{or } \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_i = -\frac{h_{fe}}{1 + h_{oe} Z_L}$$

Input Impedence: The impedence looking into the amplifier input terminals (1,1') is the input impedence Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Q.6 a. Draw & explain the Frequency response of amplifier and define 3 dB bandwidth. (8)

Answer:

Frequency response of amplifiers

Midband:

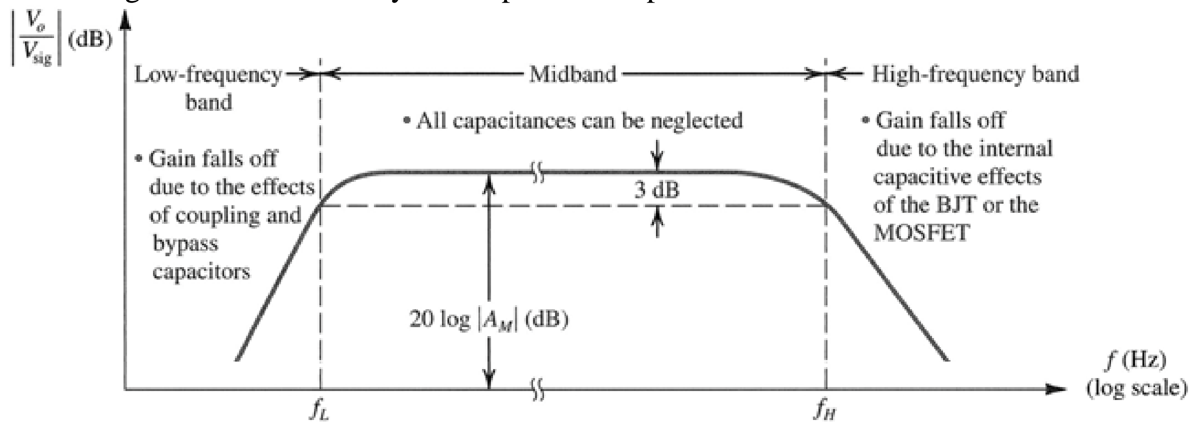
- The frequency range of interest for amplifiers
- Large capacitors can be treated as short circuit.
- small capacitors can be treated as open circuit
- Gain is constant and can be obtained by small-signal analysis

Low-frequency band:

- Gain drops at frequencies lower than f_L
- Large capacitors can no longer be treated as short circuit
- The gain roll-off is mainly due to coupling and by-pass capacitors

High-frequency band:

- Gain drops at frequencies higher than f_H
- Small capacitors can no longer treated as open circuit
- The gain roll-off is mainly due to parasitic capacitances of the BJTs



b. Derive the expression to calculate the higher cut-off frequency of the emitter follower amplifier. (8)

Answer:

The emitter follower:

- Low-frequency (midband) gain and output resistance:

$$A_M \approx \frac{R_L}{R_L + r_e} \approx 1$$

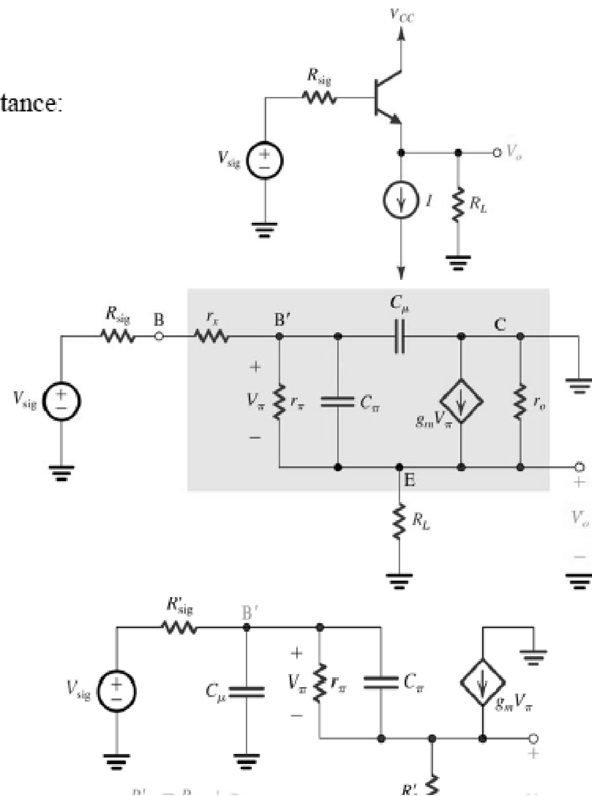
$$R_o = R_L \,||\, r_o \,||\, [r_e + R'_{sig}/(1+\beta)]$$

- High-frequency characteristics:
  - High-frequency zero:
    - ➔ Output becomes 0 at $s = s_Z = -1/C_\pi r_e$
    - ➔ High-frequency zero: $\omega_Z = 1/C_\pi r_e$
    - ➔ $f_Z \cong f_T$ (transistor's unity-gain frequency)
  - The 3-dB frequency f_H:

$$R_\mu = R'_{sig} \,||\, [r_\pi + (\beta+1)R'_L]$$

$$R_\pi = \frac{R'_{sig} + R'_L}{1 + \frac{R'_{sig}}{r_\pi} + \frac{R'_L}{r_e}}$$

$$f_H = \frac{1}{2\pi}(C_\mu R_\mu + C_\pi R_\pi)$$



Q.7 a. The permissible range of a power transistor is defined $P(\max) = 10W$, $I_c(\max) = 1A, V_{CE}(\max) = 100V, V_C(\min) = 2V$

(i) Select an approximate operating point for operation in the circuit of Fig.2. Note that R_E has been considered to be negligible.

(ii) Specify R_L for maximum power output.

(iii) Calculate total dc power in, maximum signal power out, and overall efficiency. (8)

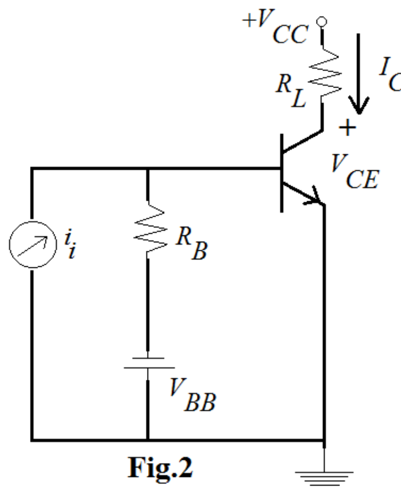


Fig.2

Answer:

Solution (a) $P_D = i_C v_{CE} = 10$ W(max), curve is drawn in Figure 5.12. The load line (for max ac output) is also drawn in the figure, which specifies the Q-point as

$$V_{CEQ} = 46 \text{ V}, I_{CQ} = 210 \text{ mA}, V_{CC} = 92 \text{ V}$$

(b) Q-point selected in part (a) gives R_L for maximum power output.

$$R_L = \frac{V_{CC}}{I_C(\text{peak})} = \frac{V_{CEQ}}{I_{CQ}} = \frac{46}{0.21} = 219\ \Omega$$

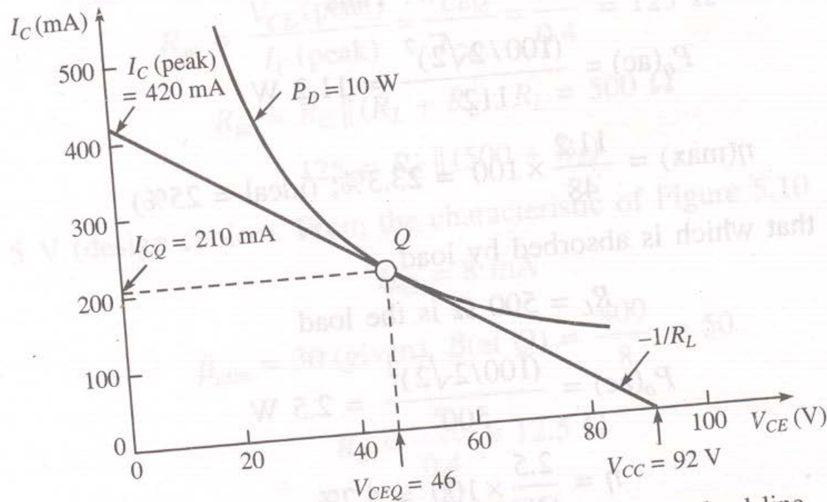


FIGURE 5.12 Example 5.3—P_D curve and ac load line.

(c) $P_i(\text{dc}) = V_{CC} I_{CQ} = 92 \times 0.21 = 19.32$ W

$$P_o(\text{ac})(\text{max}) = \left(\frac{i_C(\text{p-p})}{2\sqrt{2}}\right)^2 \times R_L = \left(\frac{0.42}{2\sqrt{2}}\right)^2 \times 219 = 4.8 \text{ W}; \ i_C(\text{p-p}) = 0.42$$

$$\eta = \frac{4.8}{19.32} \times 100 = 24.8 \approx 25\% \text{ (as expected)}$$

b. Show that the maximum efficiency of series fed class A power amplifier is 25%. (8)

Answer:

For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}(V_{CC}/R_C)}{8} = \frac{V_{CC}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2} = \frac{V_{CC}^2}{2R_C}$$

$$\text{maximum } \%\,\eta = \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\% = 25\%$$

Q.8 a. The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. Given that feedback fraction = 0.01. (4)

Answer:

Solution. $A_v = 3000, \quad m_v = 0.01$

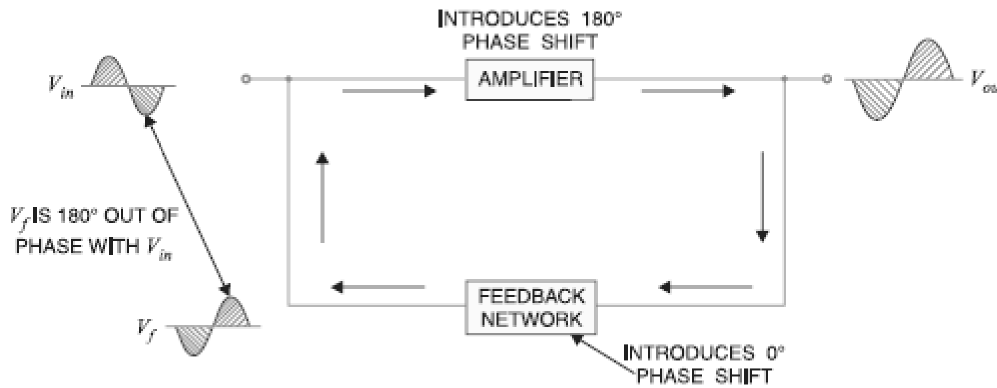
∴ Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v} = \frac{3000}{1 + 3000 \times 0.01} = \frac{3000}{31} = 97$$

b. Define negative feedback in amplifiers. (4)

Answer:

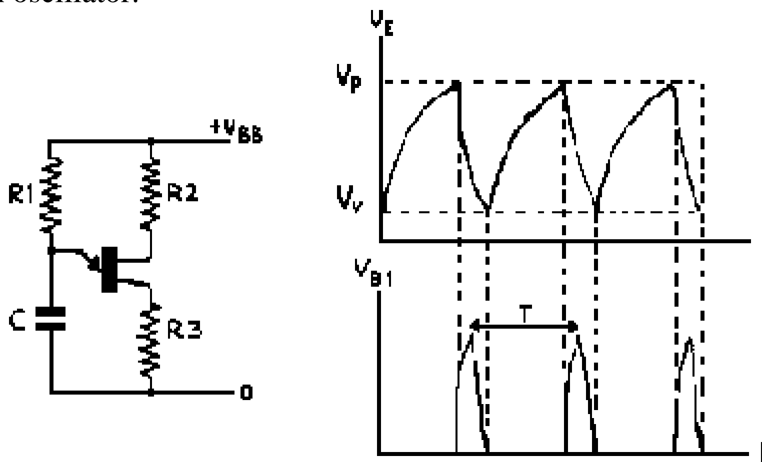
When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called negative feedback. This is illustrated in Fig. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage Vf is 180° out of phase with the input signal Vin.



c. Draw and explain Unijunction oscillator. (8)

Answer:

Ans: Unijunction transistor(UJT) can be used in a single stage oscillator circuit to provide a pulse signal suitable for digital circuit applications. The UJT can be used in relaxation oscillator.



The operation of the circuit is as follows: C1 charges through R1 until the voltage across it reaches the peak point. The emitter current then rises rapidly, discharging C1 through the base 1 region and R3. The sudden rise of current through R3 produces the voltage pulse. When the current falls to IV the UJT switches off and the cycle is repeated. Oscillator operating frequency $f_o = 1/\{R_T C_T \ln[1/(1-\eta)]\}$ where, η is intrinsic standoff ratio, typically the value of it is between 0.4 and 0.6. Using $\eta = 0.5$, $f_o = 1.5 / R_T C_T$

Capacitor is charged through resistor R_T toward supply voltage V_{BB}. As long as the capacitor voltage V_E is below a stand – off voltage (V_P) set by the voltage across B_1-B_2 and the transistor stand – off ratio η.

- $V_P = \eta V_{B1} V_{B2} – V_D$.

When the capacitor voltage exceeds this value, the UJT turns ON, discharging the capacitor. When the capacitor discharges, a voltage rise is developed across R3. The signal at the emitter of UJT / across the capacitor is saw tooth, at the base 1 are positive going pulses and at the base 2 are negative going pulses.

Q.9 a. What do you mean by epitaxial growth in IC fabrication? Explain the steps involved in epitaxial growth. (8)

Answer:

Epitaxy is used to deposit N on N+ silicon, which is impossible to accomplish by diffusion. It is also used in isolation between bipolar transistors wherein N- is deposited on P. the sequence of operation involved in the process:

1. Heat wafer to 1200°C.
2. Turn on H_2 to reduce the SiO_2 on the wafer surface.
3. Turn on anhydrous HCl to vapor-etch the surface of the wafer. This removes a small amount of silicon and other contaminants.
4. Turn off HCl.
5. Drop temperature to 1100°C.
6. Turn on silicon tetrachloride ($SiCl_4$).
7. Introduce dopant.

b. Explain the various steps involved in planar technology for device fabrication. (8)

Answer:

FABRICATION PROCESS

Oxidation

The process of oxidation consists of growing a thin film of silicon dioxide on the surface of the silicon wafer.

Diffusion

This process consists of the introduction of a few tenths to several micrometers of impurities by the solid-state diffusion of dopants into selected regions of a wafer to form junctions.

Ion Implantation

This is a process of introducing dopants into selected areas of the surface of the wafer by bombarding the surface with high-energy ions of the particular dopant.

Photolithography

In this process, the image on the reticle is transferred to the surface of the wafer.

Epitaxy

Epitaxy is the process of the *controlled growth* of a crystalline doped layer of silicon on a single crystal substrate.

Metallization and interconnections

After all semiconductor fabrication steps of a device or of an integrated circuit are completed, it becomes necessary to provide metallic interconnections for the integrated circuit and for external connections to both the device and to the IC.

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TEXT BOOK

I. Electronic Devices and Circuits, 2009, I. J. Nagrath, PHI

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