Q.2 a. **An intrinsic silicon bar is 4mm long and has a rectangular cross section 60x100 (µm) ^{2}. At 300K, find the electric field intensity in the bar and voltage across the bar when a steady state current of 1µA is measured. (Resistivity of intrinsic silicon at 300K is 2.3 x 10^3 Ω−m.** **(6)**

Answer:

Length=4mm

A=60 x 100 (µm) ^{2}

Current I =1µA

Resistivity r = 2.3 x 10^3 Ωm

$J = \sigma E$

$E = J / \sigma = (I/A)(1/\sigma) = (I/A) r$

$E = (1 \times 10^{-6}/ (60 \times 10^{-6} \times 100 \times 10^{-6})) \times 2.3 \times 10^3$

$= 383.33 \times 10^3$ V/m

$V = EL = 383.33 \times 10^3 \times 4mm = 1.53 \times 10^3$ V

b. **What types of doping should be used in a switching diode? What is reverse recovery time?** **(5)**

Answer:

In switching diodes a lightly doped neutral region is made whose length is shorter than a minority carrier diffusion length. In this case the stored charge for forward conduction is very small since most of the injected carriers diffuse through the lightly doped region to end contact. When such a diode is switched to reverse conduction, very little time is required to eliminate the stored charge in the narrow neutral region. A second approach is to add efficient recombination centres to the bulk material. For Si diode, Au doping is useful for this purpose. To a good approximation the carrier the carrier lifetime varies with the reciprocal center concentration. The total time required for the reverse current to decay to 10% of its maximum magnitude is defined as recovery time.

c. **Distinguish between avalanche and zener breakdown in p-n junction diode.** **(5)**

Answer:

Both avalanche breakdown and zener breakdown occur under reverse biased condition of p-n junction and the common cause is the electric field accelerating a carrier which collides with an ion and breaks the covalent bond releasing one or more extra carriers. In the case of avalanche breakdown, the carriers are thermally generated ones accelerating under externally applied large electric field in reverse bias and the process is cumulative giving rise to more and more pairs of carriers by multiple collision of ions. The result is destructive.

On the other hand, in a zener diode, the breaking of ionic bond and generation of extra carriers is by the intense electric field across a very narrow depletion region at the junction, due mainly to rather heavy doping of both p and n regions of the diode. The resulting process gives rise to large reverse current and is reversible. This phenomenon is called 'Zener breakdown'.

Q.3   **a.** **Sketch the circuit of a bridge rectifier and describe its operation. Derive expressions for rectification efficiency and ripple factor of the circuit. If a capacitor is added to the circuit, show the output voltage waveform of the rectifier.**   **(8)**

Answer:

The bridge rectifier circuit is as shown in Fig.
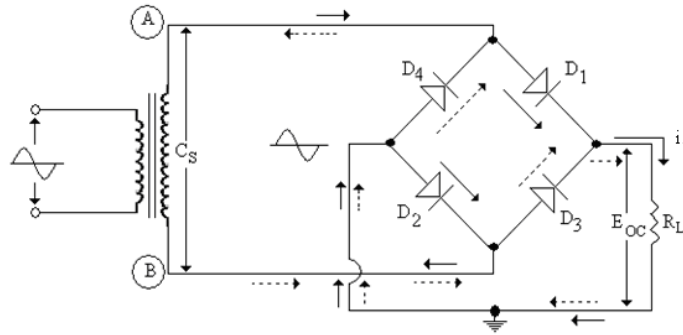
Operation: During positive half cycle of the input voltage point A becomes positive. Diodes D1 and D2 will be forward biased and D3 and D4 reverse biased. D1 and D2 conduct in series with the load and the current flows in the direction as shown in figure1 by solid arrows. In the next half cycle, when the polarity of the ac voltage reverses, 'B' becomes positive D3 and D4 are forward biased, while D1 and D2 are reverse biased. D3 and D4 conduct in series with the load and the current flows as shown by dotted arrows. During both the half cycles of input signal, the current through RL is in same direction and is as shown in Fig.
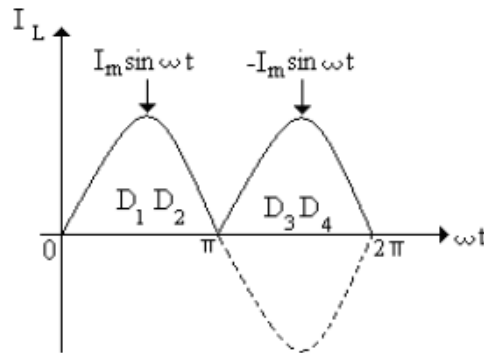
Expression for efficiency and ripple factor:

$$i_L = I_m \sin \omega t \quad 0 \le \omega t \le \pi$$

$$i_L = -I_m \sin \omega t \quad \pi \le \omega t \le 2\pi$$

$$I_{dc} = (1/\pi) \int_0^\pi I_m \sin \omega t \, d(\omega t)$$

$$I_{dc} = 2I_m / \pi \text{ and } E_{dc} = 2E_m / \pi$$

$$I_{RMS} = \sqrt{\left(\frac{1}{2\pi} \int_0^{2\pi} i_L^2 \, d\omega t\right)} = \sqrt{\left(\frac{2}{2\pi} \int_0^{\pi} (I_m \sin \omega t)\right)^2 d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi} \int_0^{\pi} [(1 - \cos 2\omega t)/2] \, d(\omega t)} = I_m/\sqrt{2}$$

In bridge rectifier, in each half cycle two diodes conduct simultaneously. Hence maximum value of load current is

Im = Em / (Rs+2Rf+RL), where Rs = transformer secondary winding resistance.

PDC = IDC^{2}RL = (2Im/p) ^{2} RL

PAC = Irms^2 (2Rf+Rs+RL) = (Im/Ö2)^2 (2Rf+Rs+RL)

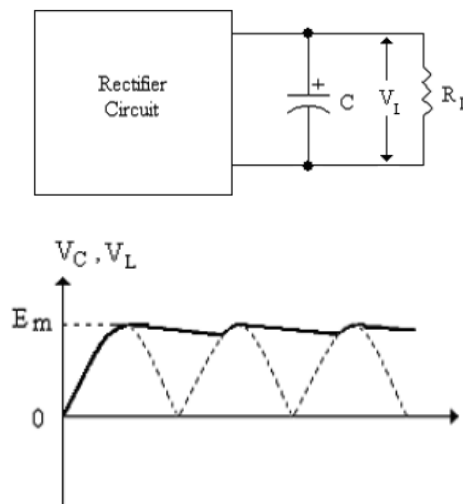$$\text{rectification efficiency} = P_{DC}/P_{AC} = \frac{[(4I_m^2/\pi^2) R_L]}{I_m^2/2 \, (2R_f + R_s + R_L)} \approx \frac{8R_L}{\pi^2 R_L} \quad (\text{since } 2R_f + R_s << R_L)$$

$$= 8/\pi^2 = 81.05\%$$
$$= 8/\pi^2 = 81.05\%$$

$$\text{Ripple factor} = \sqrt{(I_{rms}/I_{DC})^2 - 1}$$
$$= \sqrt{[(I_m/\sqrt{2})/ (2I_m/\pi)]^2 - 1} = \sqrt{(\pi^2/8) - 1} = 0.48.$$

The Fig. shows how a capacitor filter is connected to the rectifier output and the output voltage waveform of the rectifier across the load, with capacitor filter.

The dotted line in Fig. shows the rectifier output without filter and solid line shows the output across the capacitor filter.

   b. **Design a series voltage regulator to supply 1A to a load at a constant voltage of 9V. The supply voltage to regulator is 15V±10%. The minimum zener current is 12mA. For the transistor to be used, assume VBE=0.6V and β=50.**

                                                                    (8)

Answer:

$$I_B = \frac{I_c}{\beta} = \frac{1A}{50} = 20mA$$

$$V_{out} = V_z - V_{BE}$$

$$9 = V_z - 0.6$$

$$V_z = 9.6v$$

Voltage drop in resistor $R = V_{in} - V_Z = 15 - 9.6 = 5.4v$

Current through resistor R, $I = I_B + I_Z = 20 + 12 = 32mA$

$$\therefore \quad R = \frac{Voltage\ drop\ in\ resistor\ R}{I} = \frac{5.4}{32mA}$$

$$R = 168.75\Omega.$$

Q.4   **a. Draw a figure to show the output V-I characteristic curves of a BJT in CE configuration. Indicate thereon, the saturation, active and cut off regions. Explain how, using these characteristics, one can determine the value of h_{fe} or β_F.**   **(8)**

Answer:

a. Fig. shows the characteristics of BJT in CE configuration. To find hfe, draw a constant VCE line (vertical) going through desired Q point. Choose constant IB lines suitably, which cut the constant Vce line at X and Y.
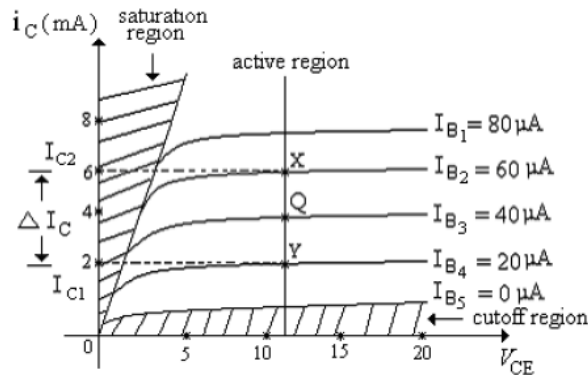
$h_{fe} = \Delta I_C / \Delta I_B$. From fig $h_{fe} = (I_{C2} - I_{C1}) / (I_{B4} - I_{B2})$
$= (6-2)$ mA $/ (60-20)$ μA $= 100$.

b. **The transistor in the feedback circuit shown below has β=200. Determine (i) feedback factor (ii) feedback ratio (iii) voltage gain without feedback (iv) voltage gain with feedback in the circuit. In the transistor, under the conditions of operation, VBE may be assumed to be negligible.(8)**
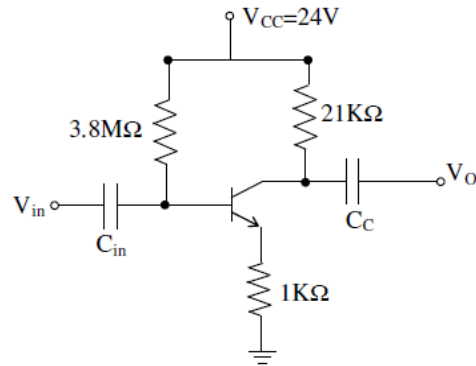
Fig.1

Answer:

$V_{cc} = 24V$, $R_B = 3.8M\Omega$, $\beta = 200$, $R_E = 1k\Omega$

$$I_E = \frac{V_{cc}}{\frac{R_B}{\beta} + R_E} = \frac{24}{\frac{3.8 \times 10^6}{200} + 1 \times 10^3}$$

$I_E = 1.2mA$

AC Emitter resistance, $r_{e'} = \frac{25mv}{I_E} = \frac{25mv}{1.2mA}$

$$r_{e'} = 20.83\Omega$$

Voltage gain without feedback,

$$A = \frac{R_G}{r_{e'}} = \frac{21 \times 10^3}{20.83}$$

A = 1008.16

Feedback ratio $\beta = \frac{R_E}{R_C} = \frac{1 \times 10^3}{21 \times 10^3}$

$$\beta = 0.0476$$

Feedback factor $= \beta A = 0.0476 \times 1008.16$

Feedback factor $= 48.0076$

Voltage gain with feedback,

$$A_f = \frac{A}{1 + \beta A} = \frac{1008.16}{1 + 48.0076}$$

$A_f = 20.57$

Q.5   **a. Draw the block diagram of Series Voltage negative feedback and derive the expression for overall voltage gain with negative feedback.**   **(8)**

Answer:

13-1 SERIES VOLTAGE NEGATIVE FEEDBACK

Negative Feedback Concept

In a negative feedback amplifier, a small portion of the output voltage is fed back to the input. When the feedback voltage is applied in series with the signal voltage, the arrangement is *series voltage feedback*. The instantaneous polarity of the feedback voltage is normally opposite to the signal voltage polarity (they are in *series opposition*). So the feedback voltage is *negative* with respect to the signal voltage; hence the term *negative feedback (NFB)*.

Consider the illustration in Fig. 13-1a. An amplifier with two input terminals and one output is shown (in triangular representation). The amplifier has a voltage gain (A_v), and its output voltage (v_o) is applied to a feedback network that reduces v_o by a factor (B) to produce a feedback voltage (v_f). The feedback network may be as simple as the resistive voltage divider shown in Fig. 13-1b. At the amplifier input, the instantaneous level of v_f is applied negative with respect to v_s, so that the amplifier input terminal voltage is

$$v_i = v_s - v_f$$

Because the amplifier input voltage is lower than the signal voltage, the output voltage is lower than that produced when negative feedback is not used. This means, of course, that the overall voltage gain (v_o/v_s) is reduced by negative feedback. However, as will be demonstrated, the stability of the voltage gain is greatly improved with negative feedback.

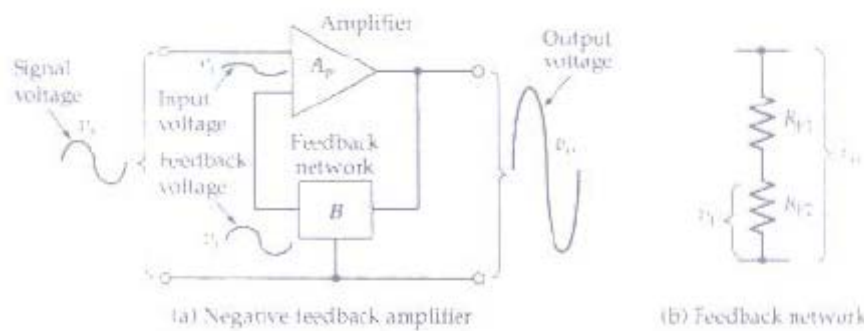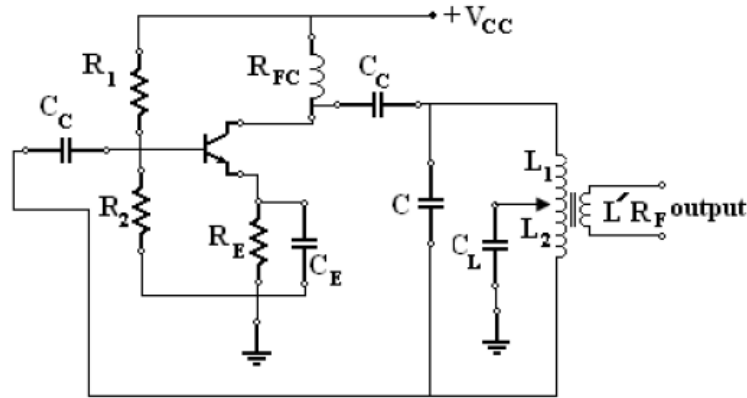(a) Negative feedback amplifier   (b) Feedback network

Figure 13-1 In a negative feedback amplifier, a portion of the output is fed back to the input. The instantaneous polarity of the feedback voltage (v_f) is negative with respect to the signal voltage (v_s).

       b. Draw the circuit of Hartley oscillator and derive an expression for its frequency of oscillation. **(8)**

Answer:

The Hartley oscillator widely used as a local oscillator in radio receivers.

$$h_{ie}(Z_1 + Z_2 + Z_3) + Z_1 Z_2(1 + h_{fe}) + Z_2 Z_3 = 0 \qquad \text{--------(1)}$$

Here $Z_1 = jwL_1 + jwM$, $Z_2 = jwL_2 + jwM$ and $Z_3 = \dfrac{1}{jwc} = -j/wc$

Substituting these values in equation (1), we get

$$h_{ie}\left[(jwL_1 + jwM) + (jwL_2 + jwM) - \frac{j}{wc}\right] + (jwL_1 + jwM)(jwL_2 + jwM)(1 + h_{fe}) + (jwL_2 + jwM)\left(-j/wc\right) = 0$$

$$jwh_{ie}\left[L_1 + L_2 + 2M - \frac{1}{w^2 c}\right] - w^2(L_2 + M)\left[(L_1 + M)(1 + h_{fe}) - \frac{1}{w^2 c}\right] = 0$$

Equating imaginary parts of above equation to zero we get,

While $\left[L_1 + L_2 + 2M - \dfrac{1}{w^2 c}\right] = 0$

Or $L_1 + L_2 + 2M - \dfrac{1}{w^2 c} = 0$ ∴ $wh_{ie} \neq 0$

$$w^2 c = \frac{1}{L_1 + L_2 + 2M}$$

Or $f = \dfrac{w}{2\pi} = \dfrac{1}{2\pi\sqrt{c(L_1 + L_2 + 2M)}}$

Q.6 a. Compare the memory devices RAM and ROM? Explain why ROM is a non volatile memory and dynamic RAMs require refreshing? **(8)**

Answer:
Comparison of Semi-conductor Memories ROM and RAM

The advantages of ROM are:
1. It is cheaper than RAM.
2. It is non-volatile. Therefore, the contents are not lost when power is switched off.
3. It is available in larger sizes than RAM. '
4. It's contents are always known and can be easily tested.
5. It does not require refreshing.
6. There is no chance of any accidental change in its contents.

The advantages of RAM are:
1. It can be updated and replaced.

2. It can serve as temporary data storage.
3. It does not require lead time (as in ROM) or programming time (as in PROM).
4. It does not require any programming equipment

ROM: ROM is Read Only Memory and is a Permanent or Semi-permanent Memory. In Permanent ROM, the data is permanently stored and cannot be changed. It can only be read from the memory. There cannot be a write operation because the specified data is programmed into the device by the manufacturer or the user. In Semi-permanent ROM also there is no write operation, but the data can be altered, to a limited extent, by special methods. Programming of ROM involves making of the required interconnections at the time of fabrication and therefore, its contents are unaffected, even when the power is OFF. Thus it is a Non-Volatile Memory.

RAM: RAM is Random Access Memory. Because of the charge's natural tendency to distribute itself into a lower energy-state configuration (i.e., the charge stored on capacitors leak-off with time), dynamic RAMs require periodic charge refreshing to maintain data storage.

b. **Convert the decimal number 82.67 to its binary, hexadecimal and octal equivalents.** (8)

Answer:
Conversion of Decimal number 82.67 to its Binary Equivalent

Considering the integer part 82 and finding its binary equivalent

2	82	
2	41	Remainder ----- 0 (LSB)
2	20	Remainder ----- 1
2	10	Remainder ----- 0
2	5	Remainder ------0
2	2	Remainder ----- 1
2	1	Remainder ---- 0
	0	Remainder ---- 1 (MSB)

The Binary equivalent is $(1010010)_2$.
Now taking the fractional part i.e., 0.67

Fraction	Fraction X 2	Remainder New Fraction	Integer
0.67	1.34	0.34	1
0.34	0.68	0.68	0
0.68	1.36	0.36	1
0.36	0.72	0.72	0
0.72	1.44	0.44	1
0.44	0.88	0.88	0
0.88	1.76	0.76	1
0.76	1.52	0.52	1

It is seen that, it is not possible to get a zero as remainder even after 8 stages. The process continued further on an approximation can be made and the process is terminated here. The binary equivalent is 0.10101011.

Therefore, the binary equivalent of decimal number **82.67 is (1010010.10101011)₂**.

(i)   **Conversion of the binary equivalent of decimal number 82.67 into**

 Hexadecimal:

The binary equivalent of decimal number 82.67 is $(1010010.10101011)_2$
Convert each 4-bit binary into an equivalent hexadecimal number i.e.

$$0101 \quad 0010 \quad .1010 \quad 1011$$
$$5 \qquad 2 \qquad A \qquad B$$

Therefore, the hexadecimal equivalent of decimal number 82.67 is (52.AB)₁₆

(ii)   **Conversion of the binary equivalent of decimal number 82.67 into Octal number:**

The binary equivalent of decimal number 82.67 is $(1010010.10101011)_2$
Convert each 3-bit binary into an equivalent octal number i.e.

$$001 \quad 010 \quad 010 \quad .101 \quad 010 \quad 110$$
$$1 \quad 2 \quad 2 \quad .5 \quad 2 \quad 6$$

Therefore, the Octal equivalent of decimal number 82.67 is (122.526)₈

Q.7   a. **Prove the following Boolean identities.**   **(6)**

(i) $XY + YZ + \bar{Y}Z = XY + Z$
(ii) $A.B + \bar{A}.B + \bar{A}.\bar{B} = \bar{A} + B$

Answer:

(i) Prove the Boolean Identity $XY + YZ + \overline{Y}Z = XY + Z$

$$L.H.S = XY + YZ + \overline{Y}Z$$
$$= XY(Z + \overline{Z}) + YZ + \overline{Y}Z \; (\because Z + \overline{Z} = 1)$$
$$= XYZ + XY\overline{Z} + YZ + \overline{Y}Z$$
$$= YZ(1+X) + XY\overline{Z} + \overline{Y}Z$$
$$= YZ + XY\overline{Z} + \overline{Y}Z \; (\because 1+X = 1)$$
$$= Z(Y + \overline{Y}) + XY\overline{Z}$$
$$= Z + XY\overline{Z} \; (\because Y + \overline{Y} = 1)$$
$$= Z + XY \; (\because Z + XY\overline{Z} = Z + XY)$$
$$= R.H.S \; \textbf{(Hence Proved)}$$

(ii) Prove the Boolean Identity $AB + \overline{A}B + \overline{A}\,\overline{B} = \overline{A} + B$

$$R.H.S = \overline{A} + B$$
$$= \overline{A}(B + \overline{B}) + B(A + \overline{A}) \; (\because B + \overline{B} = 1 \; \& \; A + \overline{A} = 1)$$
$$= \overline{A}(B + \overline{B}) + B(A + \overline{A})$$
$$= \overline{A}B + \overline{A}\,\overline{B} + BA + B\overline{A}$$
$$= \overline{A}B + \overline{A}\overline{B} + BA \; (\overline{A}B + \overline{A}B = \overline{A}B)$$
$$= L.H.S \; \textbf{(Hence Proved)}$$

b. Minimize the logic function $Y(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$. Use Karnaugh map. Draw logic circuit for the simplified function. **(10)**

Answer:

Fig. 5(i) shows the Karnaugh map. Since the expression has 4 variables, the map has 16 cells. The digit 1 has been written in the cells having a term in the given expression. The decimal number has been added as subscript to indicate the binary number for the concerned cell. The term ABC D cannot be combined with any other cell. So this term will appear as such in the final expression. There are four groupings of 4 cells each. These correspond to the min terms (0, 1, 2, 3), (0, 1, 8, 9), (1, 3,5,7) and (1, 3, 9, 11). These are shown in the map. Since all the terms (except 14) have been included in groups of 4 cells, there is no need to form groups of two cells.
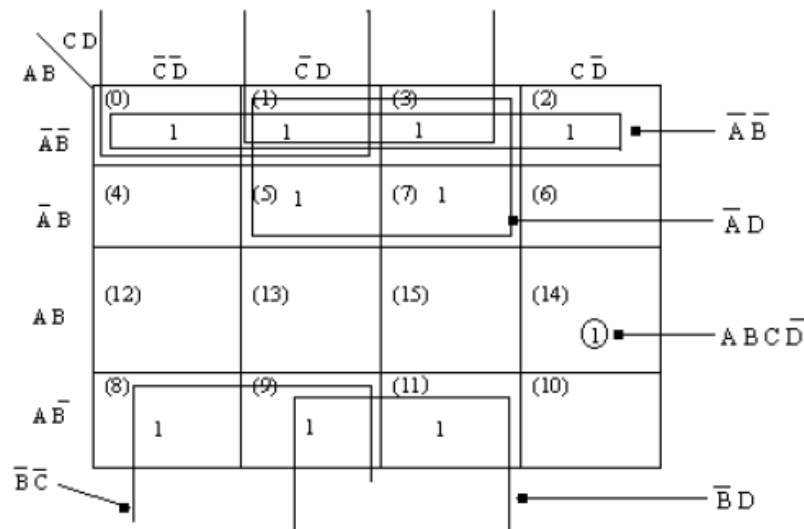

Fig.5(i)

The simplified expression is $Y(ABCD) = ABC\bar{D} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{B}D + \bar{A}D$ Fig.5(ii) shows the logic diagram for the simplified expression

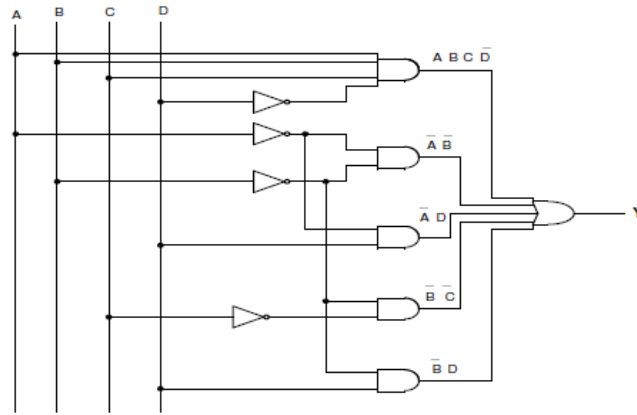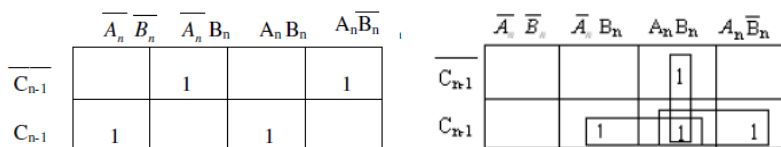$$Y(ABCD) = ABC\bar{D} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{B}D + \bar{A}D$$

Fig.5(ii)

Q.8   a. Discuss in detail, the logic and working of Full Adder. Also realize circuit by NAND-NAND Logic.   **(8)**

Answer:

Full-Adder: A half-adder has only two inputs and there is no provision to add a carry from the lower order bits when multibit addition is performed. For this purpose, a third input terminal is added and this circuit is used to add An, Bn, and Cn-1, where An and Bn are the nth order bits of the numbers, A and B respectively and Cn-1 is the carry generated from the addition of (n-1)th order bits. This circuit is referred to as full adder and its truth table is given in Table
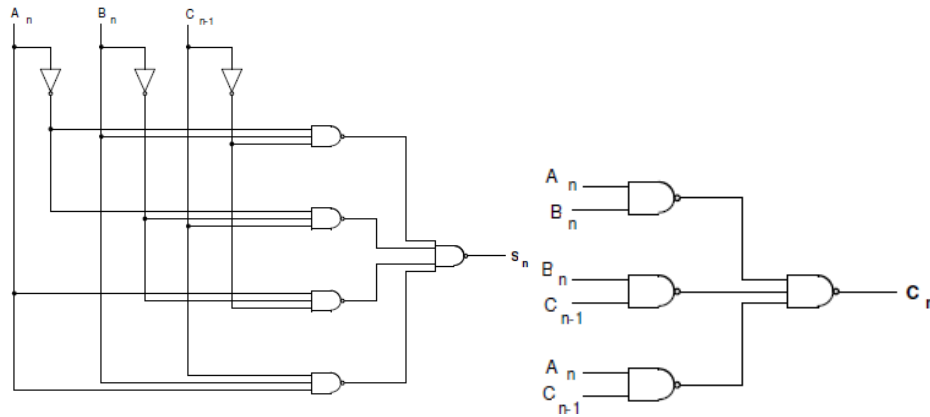
	Inputs			Outputs	
A_n	B_n	C_{n-1}	S_n		C_n
0	0	0	0		0
0	0	1	1		0
0	1	0	1		0
0	1	1	0		1
1	0	0	1		0
1	0	1	0		1
1	1	0	0		1
1	1	1	1		1

	$\bar{A}_n\bar{B}_n$	$\bar{A}_n B_n$	$A_n B_n$	$A_n\bar{B}_n$
$\bar{C}_{n-1}$		1		1
C_{n-1}	1		1	

	$\bar{A}_n\bar{B}_n$	$\bar{A}_n B_n$	$A_n B_n$	$A_n\bar{B}_n$
$\bar{C}_{n-1}$			1	
C_{n-1}		1	1	1

The K-maps for the outputs Sn and Cn are given above respectively and the minimized expressions are given below, the NAND-NAND realization of which, is also given

$$S_n = \overline{A_n}\, B_n\, \overline{C_{n-1}} + \overline{A_n}\ \overline{B_n}\ C_{n-1} + A_n\, \overline{B_n}\ \overline{C_{n-1}} + A_n\, B_n\, C_{n-1}$$

$$C_n = A_n\, B_n + B_n\, C_{n-1} + A_n\, C_{n-1}$$

b. **Design a 4 to 1 Multiplexer by using the three variable function given by(8)**
F(A,B,C) = ∑m(1,3,5,6).

Answer:

The function $F(A,B,C) = \sum m(1,3,5,6)$ can be implemented with a 4-to-1 multiplexer as shown in Fig.. Two of the variables, B and C are applied to the selection lines in that order, i.e., B is connected to S1 and C to S0. The inputs of the multiplexer are 0, I, A, and A'. When BC = 00, output F = 0 since I0 = 0. Therefore, both minterms m0 = A' B' C' and m4 = A B' C' produce a 0 output, since the output is 0 when BC = 00 regardless of the value of A.

When BC = 01, output F = 1, since I1 = 1. Therefore, both minterms m1 =A' B'C and m5 = AB'C produce a 1 output, since the output is 1. when BC = 01 regardless of the value of A.

When BC = 10, input I2 is selected. Since A is connected to this input, the output will be equal to 1 only for minterm m6 = ABC', but not for minterm m2 = A' BC', because when A' = I, then A = 0, and since I2 = 0, we have F = 0.

Finally, when BC = 11, input I3 is selected. Since A' is connected to this input, the output will be equal to 1 only for minterm m3 = A' BC, but not for m7 = ABC. This is given in the Truth Table shown in Table

Minterm	A	B	C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0
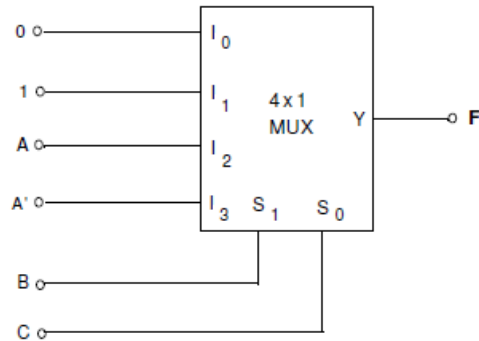
Q.9 a. Explain the working of master-slave JK flip flop. **(8)**
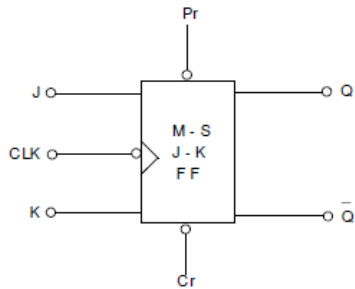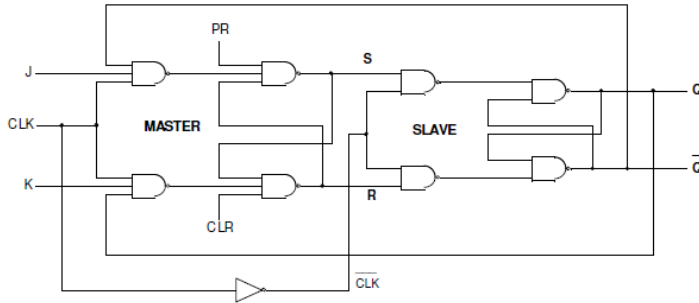**Answer:**

Master-Slave *J-K* FLIP-FLOP: A master-slave *J-K* FLIP-FLOP is a cascade of two *SR* FLIP-FLOPS. One of them is known as Master and the other one is slave. Fig. shows the logic circuit. The master is positively clocked. Due to the presence of inverter, the slave is negatively clocked. This means that when clock is high, the master is active and the slave is inactive. When the clock is low, the master is inactive and the slave is active. Fig. shows the symbol. This is a level locked Flip-Flop. When clock is high, any changes in J and K inputs can affect S and R outputs. Therefore, J and K are kept constant during positive half of clock. When clock is low, the master is inactive and J and K inputs can be allowed to be changed. The different conditions are Set, reset, and Toggle. The race condition is avoided because of feedback from slave to master and the slave being inactive during positive half of clock.

SET State: Assume that Q is low (and $\bar{Q}$ is high). For high J, low K and high CLK, the

Master goes to SET state giving High S and Low R. Since Slave is inactive, Q and $\bar{Q}$ do not change. Then CLK becomes Low, the Slave becomes to Set state giving High Q (and

low $\bar{Q}$).

RESET State: At the end of Set State Q is High (and $\bar{Q}$ low). Now if J is low, K is high

and CLK is high, the Master Resets giving Low S and High R. Q and $\bar{Q}$ do not change because Slave is inactive. When CLK becomes Low, the Slave becomes active and resets

giving Low Q (and High $\bar{Q}$).

Toggle State: If both J and K are High, the Slave copies the Master. When the CLK is High, the Master toggles once. Then the Slave toggles once when CLK is low. If the Master toggles into Set state, the slave copies the Master and toggles into Set state. If the Master toggles into Reset state, the slave again copies the Master and toggles into Reset state. Since the second FLIP-FLOP simply follows the first one, it is referred to as the *slave* and the first one as the *master*. Hence, this configuration is referred to as *masterslave (M-S) FLIP*-FLOP. Truth Table of JK Master Slave Flip-Flop in Table shows that a Low PR and Low CLR can cause race condition. Therefore, PR and CLR are kept High when inactive. To clear, we make CLR Low and to preset we make PR Low. In both cases we change them to High when the system is to be run. Low J and Low K produce inactive state irrespective of clock input. If K goes High, the next clock pulse

resets the Flip-Flop. If J goes High by itself, the next clock pulse sets the Flip-Flop. When both J and K are High, each clock pulse produces one toggle.

		Inputs			Output
PR	CLR	CLK	J	K	Q
0	0	X	X	X	Race Condition
0	1	X	X	X	1
1	0	X	X	X	0
1	1	X	0	0	No change
1	1	⎍	0	1	0
1	1	⎍	1	0	1
1	1	⎍	1	1	Toggle

b. Define a register. Explain how a shift register can be used as a ring counter giving the wave forms at the output of the flip flops. **(8)**

Answer:

Register: A register consists of a group of flip-flops and gates that effect their transition. The flip flops hold the binary information and the gates control when and how new information is transformed into the register.

Shift Register as a Ring Counter: A Ring Counter is a Circular Shift Register with only one flip-flop being set at any particular time; all other are cleared. The single bit is shifted from one flip-flop to the other to produce the sequence of timing signals. Fig shows a 4-bit shift register connected as a ring counter. The initial value of the register is 1000, which produces the variable T_0. The single bit is shifted right with every clock pulse and circulates back from T_3 to T_0. Each flip-flop is in the 1 state once every four clock pulses and produces one of the four timing signals shown in Fig. Each output becomes 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock pulse.
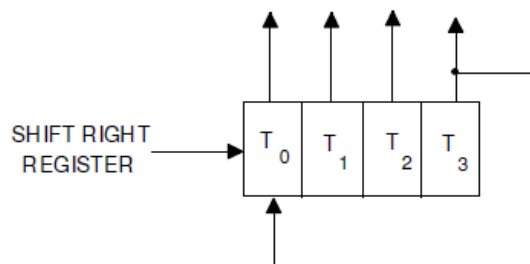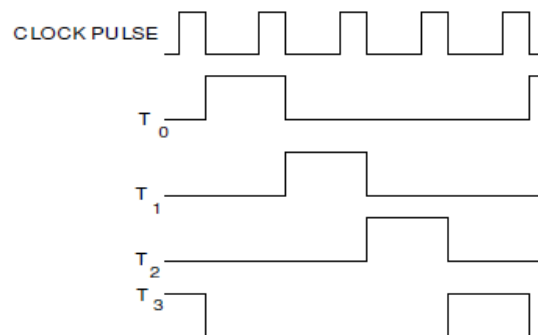
Fig. 4-bit shift register connected as a ring counter

Fig. Waveforms at the output of Flip-Flops

CODE AC103/AT103   SUBJECT ANALOG & DIGITAL ELECTRON

(Marking Scheme)

PART A – ANALOG Electronics
PART B – DIGITAL Electronics

(A) Formulea – 2 Marks
     Calculations – 4 Marks } (6) Marks

(b) Dopings – 3 Marks
     Reverse Recovery time – 2 Marks } (5) Marks   (16) Marks.

(c) Distinction between
     Avalanche & Zener breakdown } (5) Marks

(a) Bridge Rectifier ckt diagram – 2 Marks
         Explanation   – 2 Marks
         Derivations   – 3 Marks   } (8) Marks
         Waveform   – 1 Mark
                                                          (16) Marks

(b) Design equations – 3 Marks
     calculations   – 3 Marks   } (8) Marks.
     final diagram   – 2 Marks

(a) Figure   – 2 Marks
     Explanation – 6 Marks   } (8) Marks
                                      (16) Marks.

(b) Formulea – 3 Marks
     Calculations – 5 Marks } (8) Marks

(a) Block diagram – 3 Marks } 8 Marks
    Derivation – 5 Marks   } 16 Marks

(b) Diagram – 3 Marks } 8 Marks
    Derivation – 5 Marks

(a) Comparison – 2 Marks }
    explanation – 3 Marks } 8 Marks
    lettering – 3 Marks   } 16 Marks

(b) Binary, hexadecimal
    & octal conversions } 8 Marks

(a) (i) Proof } 2×3 = 6 Marks
    (ii)   } 16 Marks

(b) K map diagram – 3 Marks }
    Correct entries – 4 Marks } 10 Marks
    Final Answer – 3 Marks

(a) Working of full adder – 4 Marks }
    Realization by NAND-NAND – 4 Marks } 8 Marks
    Logic   } 16 Marks

(b) Simplification – 3 Marks }
    Design – 3 Marks } 8 Marks
    Diagram – 2 Marks

(a) Diagram – 3 Marks } 8 Marks
    Explanation – 5 Marks

(b) Register definition – 2 Marks }
    Diagram – 2 Marks } 8 Marks } 16 Marks
    Explanation – 4 Marks

TEXT BOOK

I.   Electronic Devices and Circuits, Fifth Edition, David A Bell, OXFORD University Press, Thirteenth Impression-2010

II. Digital Systems – Principles and Applications, Tenth Edition, Ronald J Tocci, Neal S Widmer and Gregory L. Moss, Pearson Education, 2011