Q.2   a. In a base-5 number system, 3 digit representations is used. Find out (i)   Number of distinct quantities that can be represented.(ii) Representation of highest decimal number in base-5.

Answer:

digits of representation $n = 3$

digits in base-5 would be – 0, 1, 2, 3, 4

(i) we have relation

$$\text{no of distinct quantities} = r^n$$
$$= 5^3 = 125$$

So, 125 distinct levels (quantities) can be represented.

(ii) Highest decimal Number can be represented by $n(r - 1)$s *i.e.,* by three 4s.

Since, r=5   So, highest decimal Number $= 444$

b. In a signed representation given binary string is $(11101)_2$. What will be the sign and magnitude of the number represented by this string in signed magnitude, 1's complement and 2's complement representation?

Answer:
The number N $= (11101)_2$
since MSB $= 1$ the given number is negative.

(i) In signed Magnitude MSB denotes sign and rest of the bits represent magnitude. So,

$$\left(\underset{\text{sign}}{1} \;\; \underset{\text{Magnitude}}{\underline{1 \;\; 1 \;\; 0 \;\; 1}}\right)_2 = -13$$

(ii) In 1's complement if number is negative (*i.e.,* MSB = 1) then the magnitude is obtained by taking 1's complement of given number.

$$\text{1's complement of } (11101)_2 = (00010)_2$$
$$\text{so } (11101)_2 = -2 \text{ in 1's complement.}$$

(iii) In 2's complement if number is negative (*i.e.,* MSB = 1) then magnitude is obtained by taking 2's complement of given number.

$$\text{2's complement of } (11101)_2 = (00011)_2$$
$$= 3$$
$$\text{so } (11101)_2 = -3 \text{ in 2's complement.}$$

c.Convert the hexadecimal 2AC5.D to decimal, octal and binary.

$$(2AC5.D)_{16} = (?)_2$$

$$2AC5 = 0010101011000101$$

$$D = 1101$$

$$(2AC5.D)_{16} = (10101011000101.1101)_2$$

$$(2AC5.D)_{16} = (?)_8$$

$$\underline{-10}\ \underline{,101}\ \underline{,011}\ \underline{,000}\ \underline{,101}\ \cdot\ \underline{,110}\ \underline{,1--}$$

$$\underline{010}\ \underline{,101}\ \underline{,011}\ \underline{,000}\ \underline{,101}\ \cdot\ \underline{,110}\ \underline{,100}$$

$$2\quad 5\quad 3\quad 0\quad 5\quad\quad 6\quad 4$$

$$(2AC5.D)_{16} = (25305.64)_8$$

$$(2AC5.D)_{16} = (?)_{10}$$

$$2AC5 = 2 \times 16^3 + 10 \times 16^2 + 12 \times 16^1 + 5 \times 16^0$$

$$= 2 \times 4096 + 10 \times 256 + 12 \times 16 + 5 \times 1$$

$$= 8192 + 2560 + 192 + 5$$

$$= 10949$$

$$D = 13 \times 16^{-1}$$

$$= 13 \times .0625$$

$$= .8125$$

$$(2AC5.D)_{16} = (10949.8125)_{10}$$

Q.3 a.   Obtain (a) minimal sum of product (b) minimal product of sum expression for the function F(w, x y, z) = Σ (0, 2, 3, 6, 7, 8, 10, 11, 12, 15).

The given function can also be written in product of minterm form as

$$F(w, x, y, z) = \prod (1, 4, 5, 9, 13, 14).$$

Squares with 1's are grouped to obtain minimal sum of product; square with 0's are grouped to obtain minimal product of sum, as shown.

(*a*) We draw a four variable map using minterms whose values in the function are equal to 1.

– Minterm 8 and 12. Four a pair.

– Minterms 0, 2, 8 and 10 form I quad.

– Minterms 3, 7, 11, 15 form II quad.

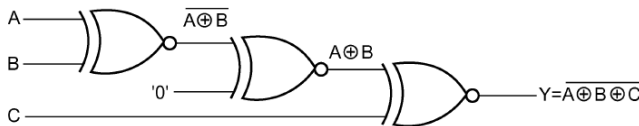– Minterms 2, 3, 6, 7 form III quad.

Therefore,

$$F = x'z + yz + w'y + wy'z'$$

↓	↓	↓	↓
Due to I quad.	II quad	III quad	Due to pair

(*b*) We draw a four variable map using minterms whose values in the function are equal to zero. These minterms are 1, 4, 5, 9, 13 and 14.

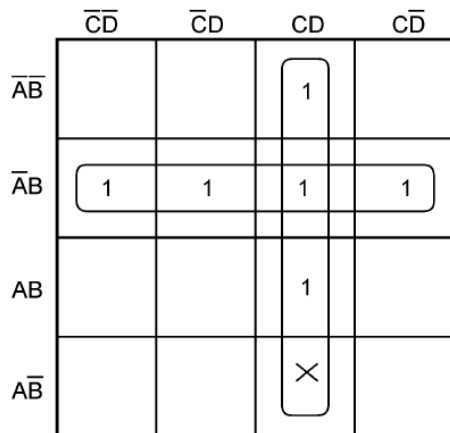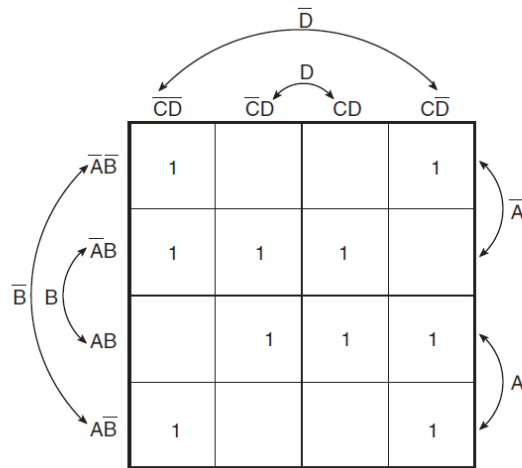**b.   Implement a three-input EX-NOR function using only two-input EX-NOR gates.**
Answer:

c.   A'B+C'D is a simplified Boolean expression of the expression A'B'C'D+A'B'C'D+A'B. Determine if there are any 'don't care' entries.

Answer:

Q.4   a.   The 100 kHz square waveform of Fig. 1(a) is applied to the clock input of the flip-flops shown in Figs. 1(b) and (c). If the Q output is initially '0', draw the Q output waveform in the two cases. Also, determine the frequency of the Q output in the two cases.   (8)

Fig.1(a)

4
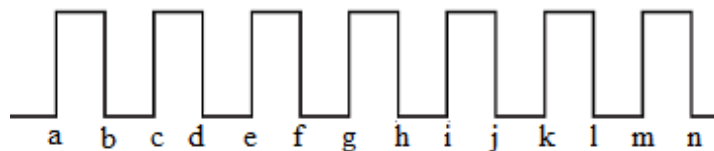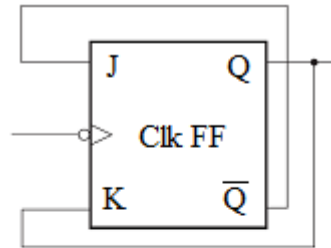
Fig.1(b)

Fig.1(c)

Answer:

(a)

b   d   f   h   j   l   n

(b)

a   c   e   g   i   k   m
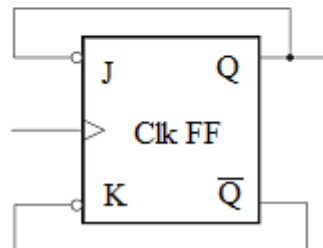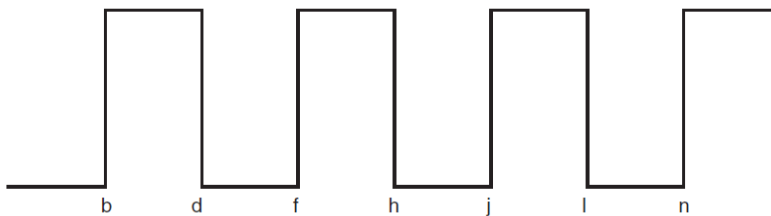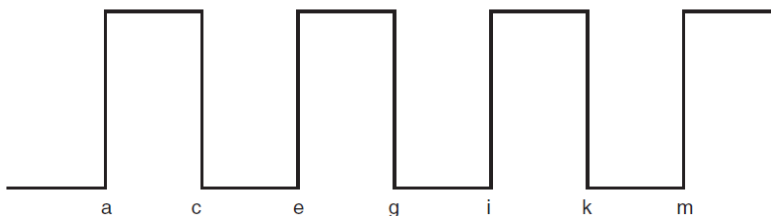
  **b.Design a mod-3 counter using JK flip-flop and explain its operation with the help of
        waveform.**
Answer:
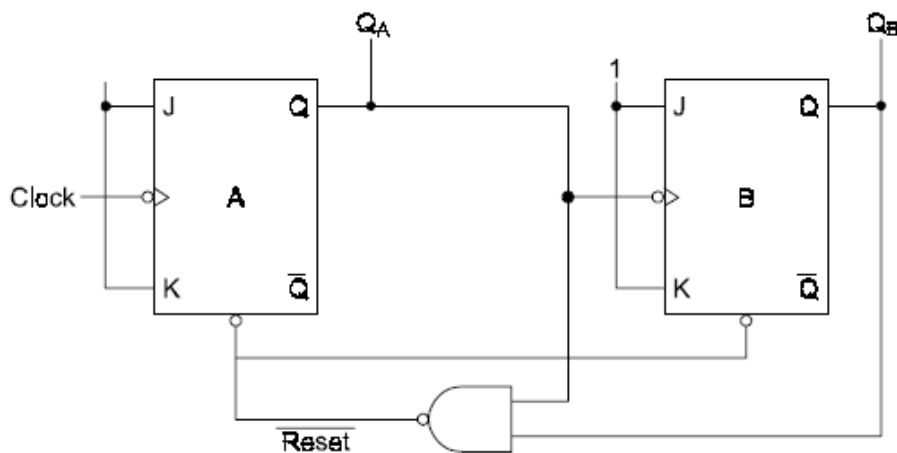
Fig. 7.29 Modulo-3 counter
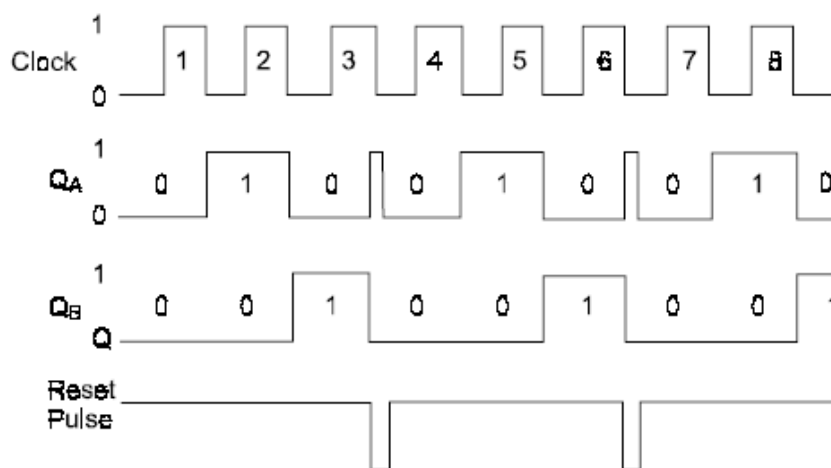
Q.5 a.   Design a 4 bit serial adder with the help of neat diagram.

Answer:

The two bits at the same positions in augend and addend word are applied serialy to A and B inputs of the full adder respectively. The single full adder is used to add one pair of bits at a time along with the carry C_{in}. The memory element is used to store the carry output of the full adder circuit so that it can be added to the next significant position of the nembers in the augend and addend word. This produces a string of output bits for sum as S_0, S_1, S_2 and S_3 respectively.

b.Determine the number of half and full adder circuit blocks required to   construct a 64-bit binary parallel adder. Also, determine the number and type of additional logic gates needed to transform this 64-bit adder into a 64-bit adder–subtractor.

Answer: *For a 64-bit adder: HA=1, FA=63*

For a 64-bit adder–subtractor: HA=1, FA=63, EX-OR gates=64

Q.6   a.   Distinguish between asynchronous and synchronous flip-flops.   Design a 4 bit universal synchronous counter using JK flip-flops.

Answer:

b. **Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010, _ _ _ Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops. What will the counter hardware look like if the unused states are to be considered as 'don't care's.**

Answer:
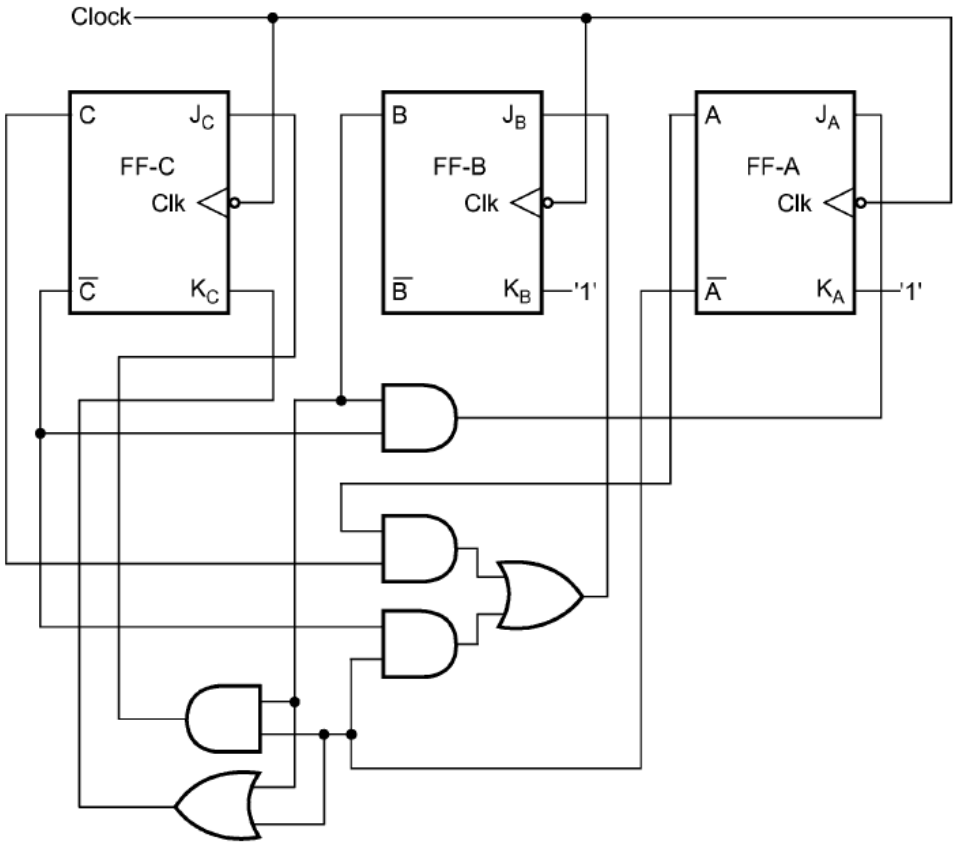
Present state			Next state			Inputs					
C	B	A	C	B	A	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X	X	X	X
1	0	1	1	1	0	X	1	1	X	X	0
1	1	0	0	0	0	0	X	X	1	X	1
1	1	1	X	X	X	X	X	X	X	X	X

c. **Determine the modulus of the presettable counter shown in Fig. 2. If the counter were initially in the 0110 state, what would be the state of the counter immediately after the eighth clock pulse be?**
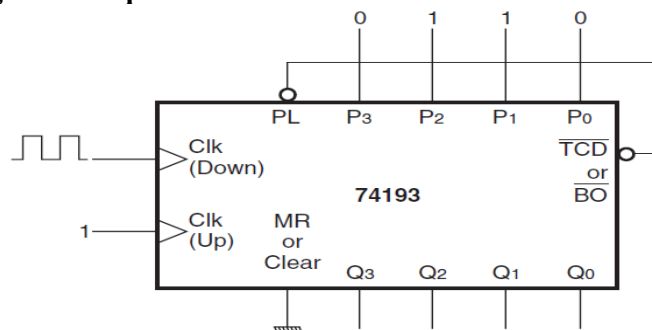

Fig.2

Answer:
This presettable counter has been wired as a DOWN counter.

• The preset data input is 0110.

• Therefore, the modulus of the counter is 6 (the decimal equivalent of 0110).

• Now, the counter is initially in the 0110 state.

• Therefore, at the end of the sixth clock pulse, immediately after the leading edge of the sixth clock pulse, the counter will be in the 0000 state.

• A HIGH-to-LOW transition at the TCD output, coinciding with the trailing edge of the sixth clock pulse, loads 0110 to the counter output.

• Therefore, immediately after the leading edge of the eighth clock pulse, the counter will be in the 0100 state.

Q.7   a.   Use an 8 input MUX to implement the following equation:
$$Y = A'.B'.C'.D' + A'.B'.C.D + A'.B.C'.D + A'.B.C'.D' + A.B'.C'.D +$$
$$A.B'.C.D' + A.B.C'.D' + A.B.C'.D.$$

Answer:

Input	"Address"	Residues
I_0	$\overline{A}.\overline{B}.\overline{C}$	$\overline{D}$
I_1	$\overline{A}.\overline{B}.C$	D
I_2	$\overline{A}.B.\overline{C}$	$D + \overline{D} = 1$
I_3	$\overline{A}.B.C$	
I_4	$A.\overline{B}.\overline{C}$	D
I_5	$A.\overline{B}.C$	$\overline{D}$
I_6	$A.B.\overline{C}$	$\overline{D} + D = 1$
I_7	$A.B.C$	

b.   Implement the functions defined by the following truth table in Fig.3 using a decoder and NAND gates.

A	B	C	Y_1	Y_2
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Fig.3

Answer:

| A	B	C	Y₁	Y₂
0	0	0	0	1
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0
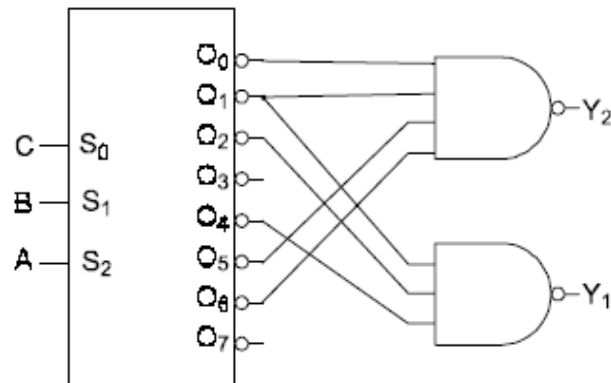
c.   **What is priority encoder? Design a 4x2 priority encoder.**

Answer:

A priority encoder is an encoder that includes priority function. If two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence. To understand priority encoder, consider a 4 to 2 line encoder which gives priority to higher subscript number input than lower subscript number. The truth table is given below.

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_1	Y_2	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1
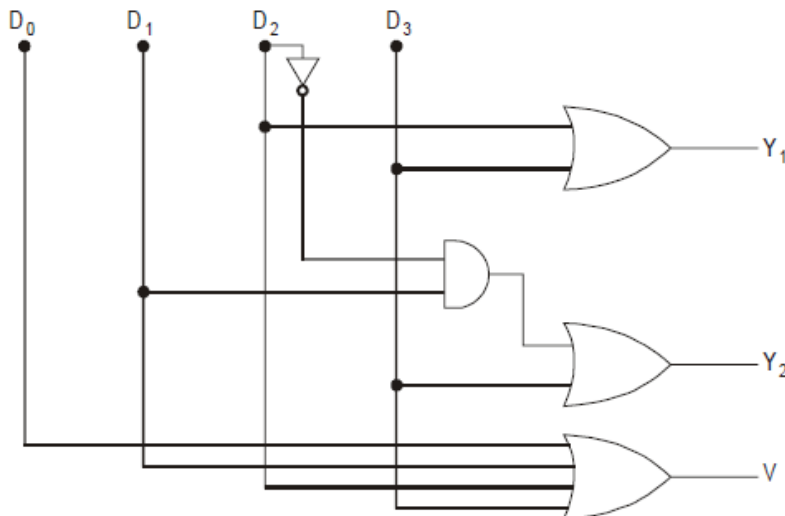
The Xs are don't care conditions. Input D_3 has the highest priority, so regardless of values of other inputs, when this input is 1, the output $Y_1 Y_2 = 11$. D_2 has next priority level. The o/p is 10 if D_2 is 1, provided $D_3 = 0$, irrespective of the values of the other two lower-priority inputs. The o/p is 01 if D_1 is 1, provided both D_2 and D_3 are O, irrespective of the value of lower-priority input D_0. The o/p is D_0 if 00 = 1, provided all other inputs are 0.

A valid output indicator, V is set to 1, only when one or more of the inputs are equal to 1. If all the inputs are O, V is equal to O. and the other two outputs if the circuit are not used.

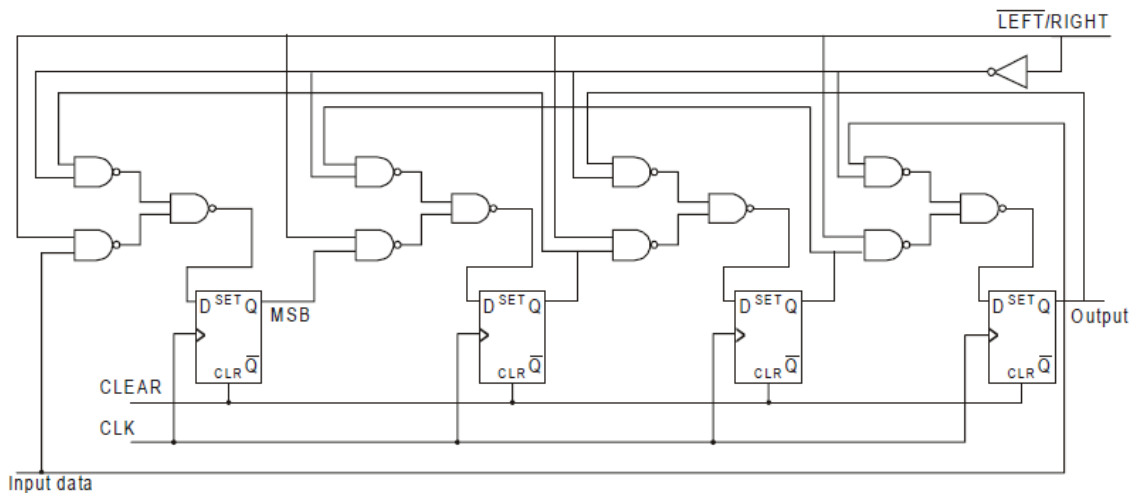Now, simplifying using k-map the outputs can be written as :

$$Y_1 = D_2 + D_3$$
$$Y_2 = D_3 + D_1 D_2{}'$$
$$V = D_0 + D_1 + D_2 + D_3.$$

Q.8   a.   Draw the diagram of four bit universal shift register and explain its operation.

Answer:

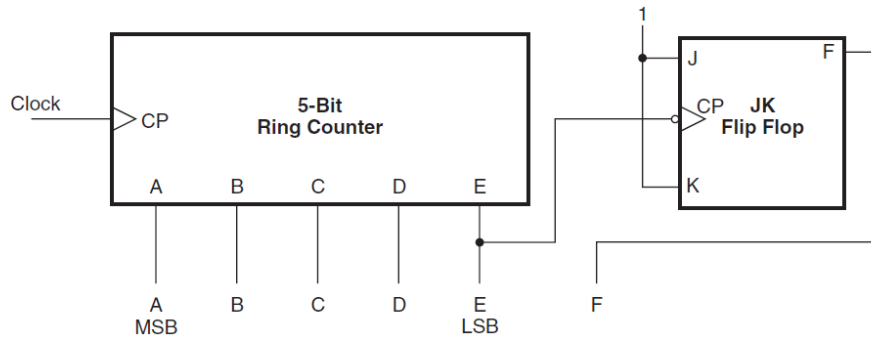b.   Refer to the logic circuit of Fig.3. Determine the modulus of this counter and write its counting sequence.


Fig.4

Answer:

Clock pulse	Outputs					
	A	*B*	*C*	*D*	*E*	*F*
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	1	0	0	0	0	1
7	0	1	0	0	0	1
8	0	0	1	0	0	1
9	0	0	0	1	0	1
10	0	0	0	0	1	1
11	1	0	0	0	0	0

Q.9 a.   It is required to obtain an 8K × 8 memory system for 8085 microprocessor system that has an addressing capability of 64K locations. Given memories are 2K × 8 ROM ICs and 2K × 8 RAM ICs. Obtain the exhaustive decoded system, which maps the 8K-memory system to begin from 8000H.

Answer:

	A₁₅	A₁₄	A₁₃	A₁₂	A₁₁	A₁₀	A₉	A₈	A₇	A₆	A₅	A₄	A₃	A₂	A₁	A₀	HEX Addr	IC
Start Addr	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000ₕ	ROM
End Addr	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	87FFₕ	1
Start Addr	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	8800ₕ	RAM
End Addr	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	8FFFₕ	1
Start Addr	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	9000ₕ	ROM
End Addr	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	97FFₕ	2
Start Addr	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	9800ₕ	RAM
End Addr	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	9FFFₕ	2
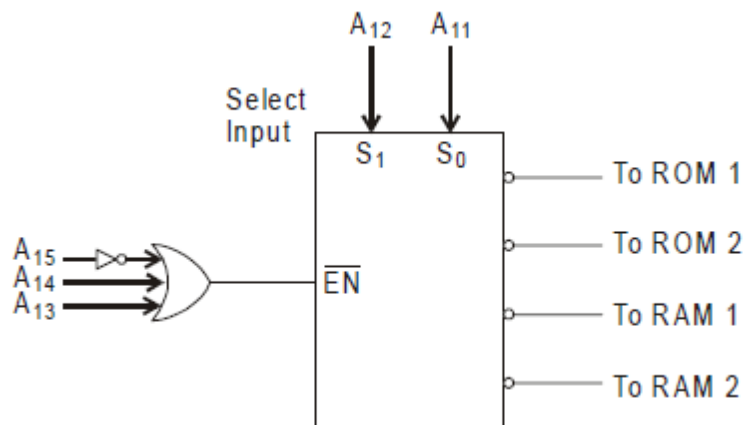
   b.   Draw the general structure of DRAM and explain it. Also compare it with SRAM.

Answer:

General Block Diagram of a $2^n \times 1$ DRAM

Fig. *(b)* General structure of A $2^n \times 1$ DRAM
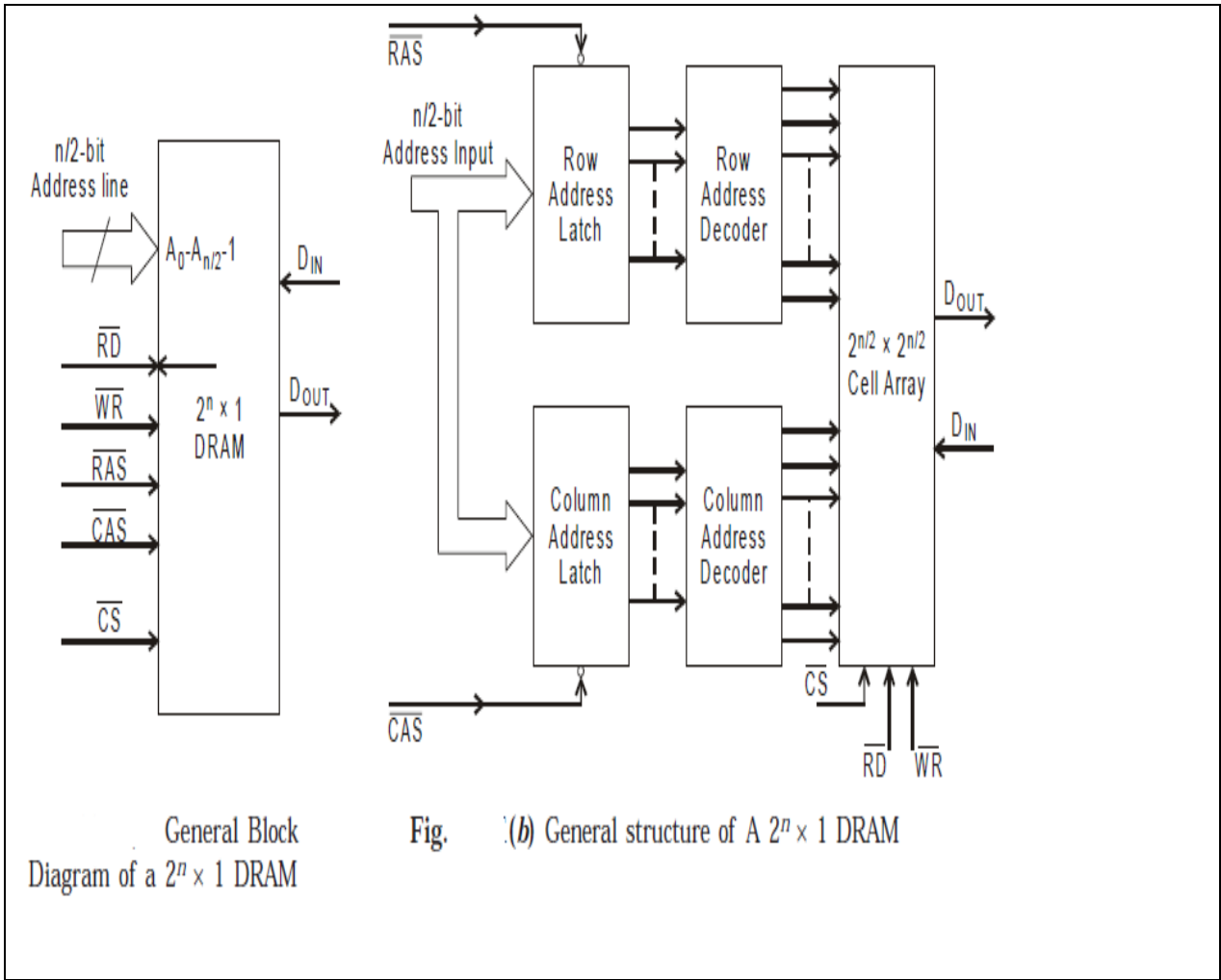
SRAMs and DRAMs

Having been studied the SRAMs & DRAMs it is worth to devote some time in comparative study of the two memories. Here are the few, which must be appreciated for the two types.

- The SRAMs cells can either be Bi-polar or MOS but DRAM cells can only be MOS.

- The DRAM cells are much simpler than the SRAM cells.

- SRAMs can retain information as long as power is ON where as DRAMs loose the retained information after a small time and thus requires refreshing.

- Data storage in DRAMs involves charge storage where as in SRAMs it involves ON/OFF the transistors.

- DRAM cells can be constructed around a single transistor where SRAMs may require 11 transistors per cell. Thus DRAMs offer higher storage density. Infact the DRAMs are among the densest VLSI circuits in terms of transistor per chip. Due to this almost all the RAMs greater than 16KB are DRAMs.

- DRAMs are cost effective memory solution than the SRAMs.

- The actual read/write mechanism of DRAMs are much more tedious than that of SRAMs.

- DRAMs are always organized with the word length of 1-bit so that they are used with SIMM module where as SRAMs are organized for many different word lengths.

- DRAMs require many hardware pins so that address lines have be multiplexed where as it is seldom the case with SRAMs.

- Timing requirements of DRAMs are very complex as compared to the timing requirements of SRAMs.

- The DRAMs suffer from destructive read out so that each read must be followed by a write whereas there is no such problem with SRAMs.

- The DRAM requires extra hardware circuitry, called DRAM Controllers, for its proper operation where as SRAM does not need such supports.

- DRAMs are slower than the SRAMs due to destructive read out, address multiplexing and mainly due to refresh requirements.

- Future expansion of DRAM is easier as they are used with SIMM module in which case expansion involves replacement of board on the slot of main board. Needless to mention that using SIMM further increases the storage capacity than achieved by using a single DRAM chip.

- The DRAM cells offer lesser power consumption compared to either BJT or MOS SRAM cell.

Text Book

1.   **Digital Systems – Principles and Applications, Ronald J Tocci, Neal S. Wildmer, Gregory L. Moss, Ninth Edition, Pearson Education, 2008**