Q.2a. Compare the available technologies in IC's Design.

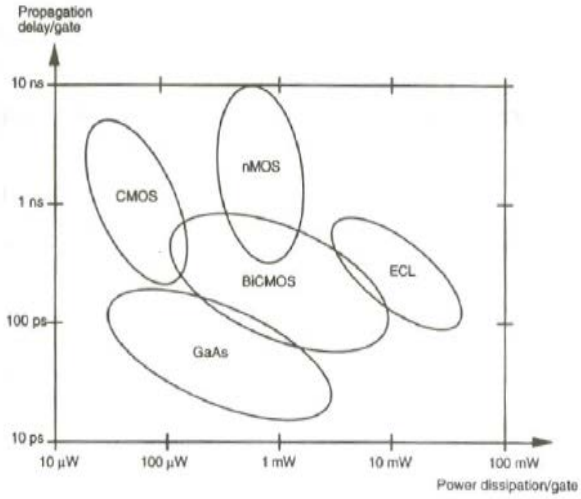
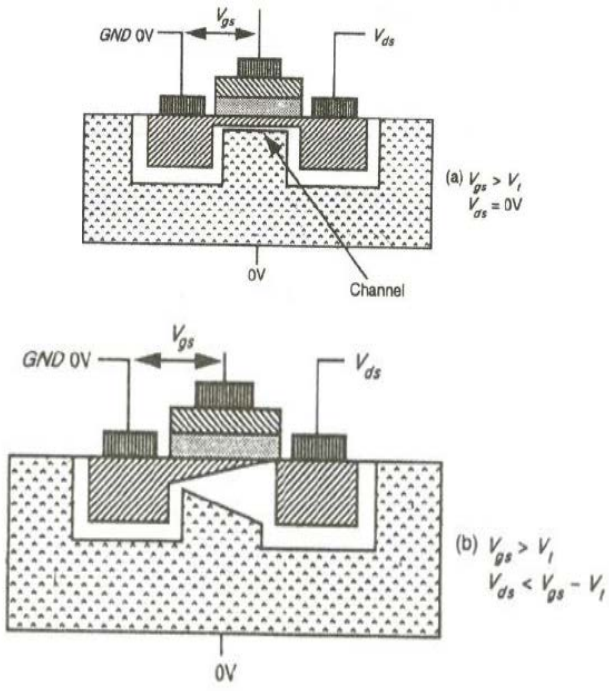


Figure 2.Comparison of available technologies.

b. With neat sketch explain the enhancement mode transistor action.



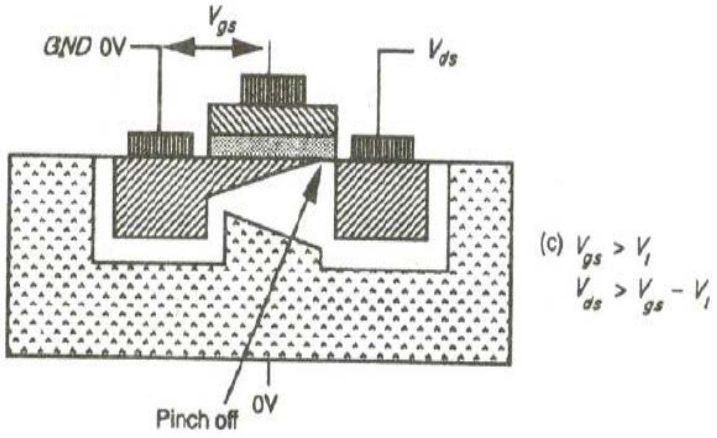
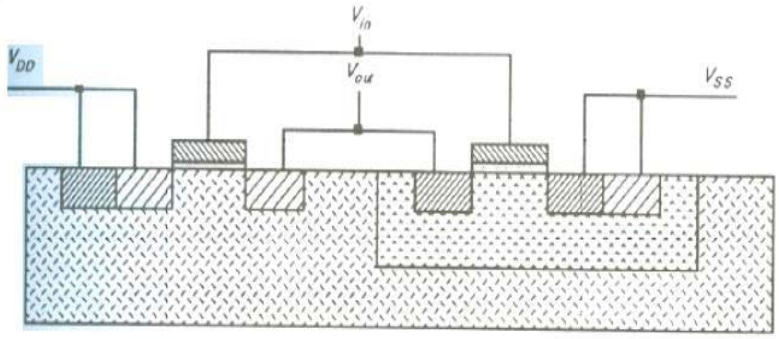


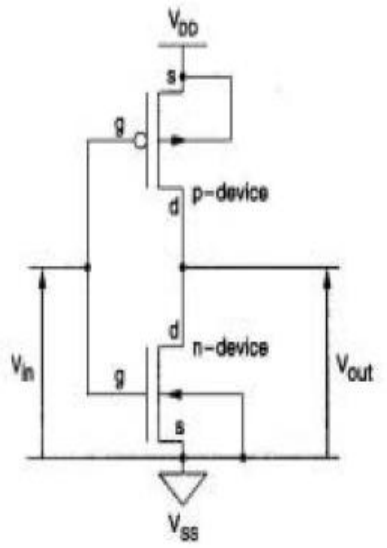
Figure7. (a)(b)(c) Enhancement mode transistor with different Vds values

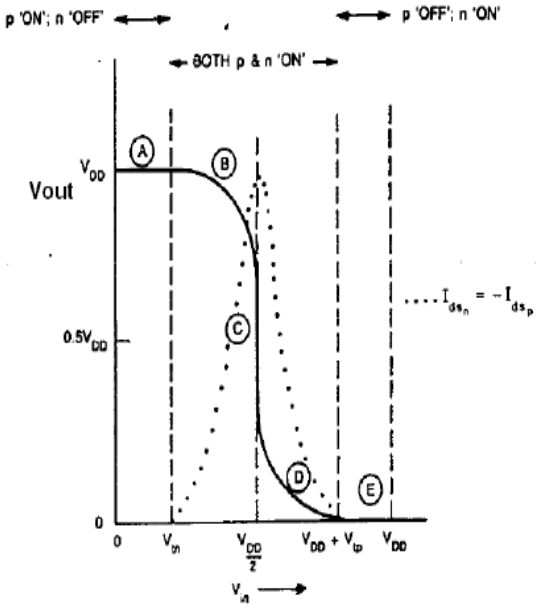
c. Draw the cross sectional view of CMOS –inverter (P-WELL).



CMOS p-well inverter showing V_{DD} and V_{SS} substrate connections.

Q.3a. Explain CMOS inverter with all the region of operations.

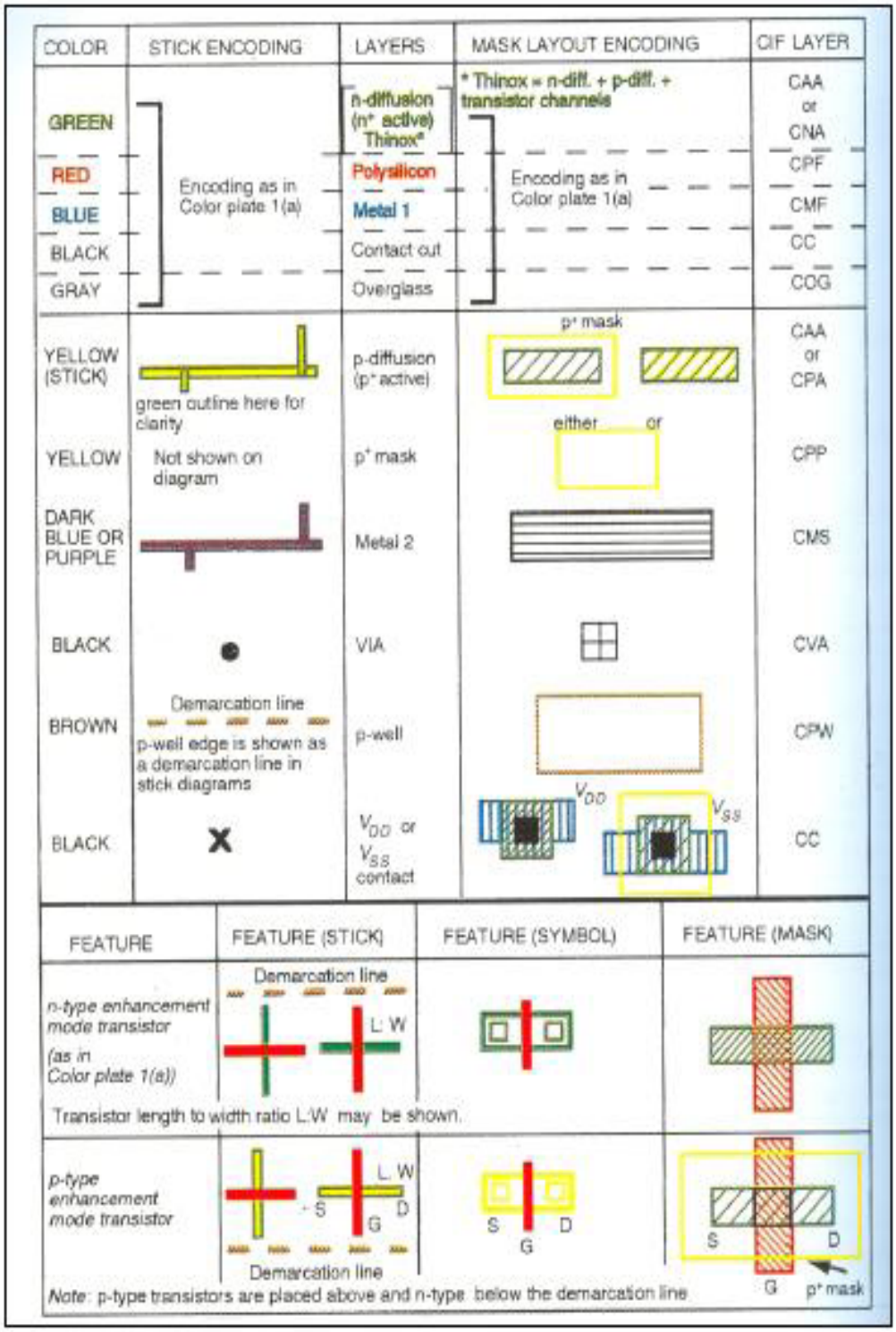




b.Define Stick Diagram. Explain the CMOS encodings in it.

Stick diagrams may be used to convey layer information through the use of a color code. For example: n-diffusion--green poly--red blue-- metal yellow--implant black--contact areas.

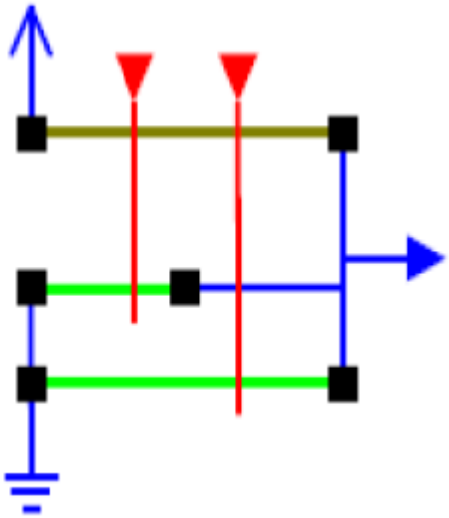
Encodings for CMOS process:


COLOR
STICK ENCODING
LAYERS
MASK LAYOUT ENCODING
CIF LAYER
GREEN
RED
BLUE
BLACK
GRAY
Encoding as in Color plate 1(a)
n-diffusion (n+ active) Thinox*
Polysilicon
Metal 1
Contact cut
Overglass
* Thinox = n-diff. + p-diff. + transistor channels
Encoding as in Color plate 1(a)
CAA or CNA
CPF
CMF
CC
COG
YELLOW (STICK)
green outline here for clarity
p-diffusion (p+ active)
p+ mask
CAA or CPA
YELLOW
Not shown on diagram
p+ mask
either or
CPP
DARK BLUE OR PURPLE
Metal 2
CMS
BLACK
VIA
CVA
BROWN
Demarcation line
p-well edge is shown as a demarcation line in stick diagrams
p-well
CPW
BLACK
VDD or VSS contact
VDD
VSS
CC
FEATURE
FEATURE (STICK)
FEATURE (SYMBOL)
FEATURE (MASK)
n-type enhancement mode transistor (as in Color plate 1(a))
Demarcation line
L
W
Transistor length to width ratio L:W may be shown.
p-type enhancement mode transistor
L
W
S
G
D
Demarcation line
S
G
D
S
D
G
p+ mask
Note: p-type transistors are placed above and n-type below the demarcation line

Q.4a. Write the circuit and stick diagram for:

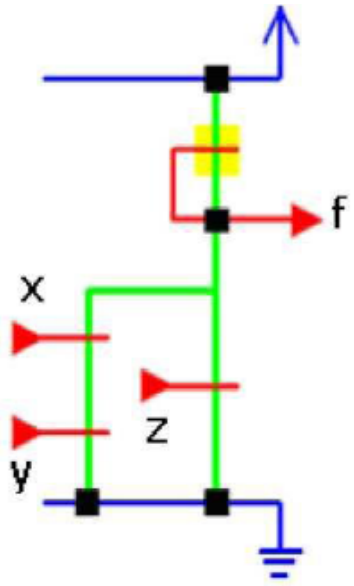
(i) two input CMOS NOR gate

(ii) f = [(xy) + z]'



CMOS NOR Gate.

Ii



stick diagram of a given function f.

b.Draw and explain nMOS enhancement mode pull-up and transfer characteristic.

Ans . Text book I 2.9-3 Fig 2.13

Q.5 a. Write short notes on – (i) Contact and Via Resistance (ii) Silicides

CONTACT AND VIA RESISTANCE

The contacts and the vias also have resistances that depend on the contacted materials and the area of contact. As the contact sizes are reduced for scaling ,the associated resistance increases. The resistances are reduced by making ohmic contacts which are also called loss less contacts. Currently the values of resistances vary from .25ohms to a few tens of ohms.

SILICIDES

The connecting lines that run from one circuit to the other have to be optimized. For this reason the width is reduced considerably. With the reduction is width the sheet resistance increases, increasing the RC delay component. With poly silicon the sheet resistance values vary from 15 to 100 ohm. This actually affects the extent of scaling down process. Polysilicon is being replaced with silicide. Silicide is obtained by depositing metal on polysilicon and then sintering it. Silicides give a sheet resistance of 2 to 4 ohm. The reduced sheet resistance makes silicides a very attractive replacement for poly silicon. But the extra processing steps are an offset to the advantage.

b.Draw the schematic of Inverting Type nMOS Super Buffer and explain its functionality briefly.

Text1 – 4.8.2 Super Buffers. Figure – 4.12

Q.6a. Discuss the Limitations of Scaling in VLSI Designs.

Effects, as a result of scaling down- which eventually become severe enough to prevent further miniaturization.

- Substrate doping
- Depletion width
- Limits of miniaturization
    - Limits of interconnect and contact resistance
    - Limits due to sub threshold currents
    - Limits on logic levels and supply voltage due to noise
    - Limits due to current density

b.Explain Structured Design Approach – Regularity with example.

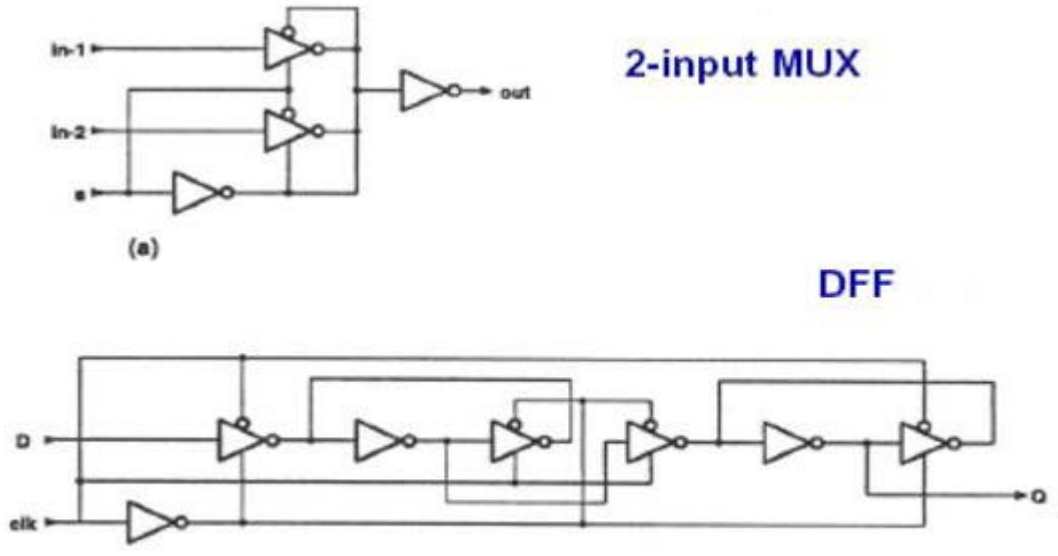
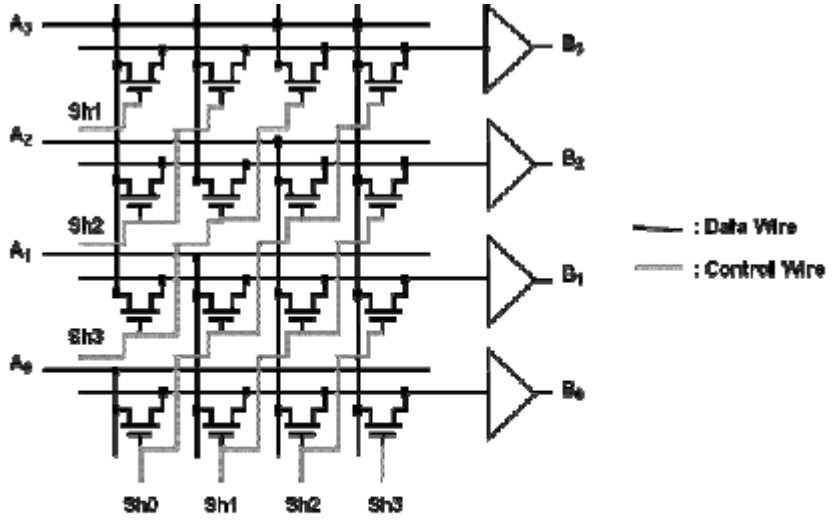


Figure5-.Structured Design Approach –Regularity

- Design of array structures consisting of identical cells.-such as parallel multiplication array.
- Exist at all levels of abstraction:
  transistor level-uniformly sized.
  logic level- identical gate structures
- 2:1 MUX, D-F/F- inverters and tri state buffers
- Library-well defined and well-characterized basic building block.
- Modularity: enables parallelization and allows plug-and-play
- Locality: Internals of each module unimportant to exterior modules and internal details remain at local level.

Q.7a. Design and explain 4 X 4 barrel shifter.



4 X 4 barrel shifter

b.Explain how to implement ALU functions with an adder?

$S_k = H_k'$ – An Ex-Nor operation

Next, consider the carry output of each element, first C_{k-1} is held at logical 0, then

$C_k = A_kB_k + H_k . 0$

$C_k = A_kB_k$ - An And operation

Now if C_{k-1} is at logical 1, then

$C_k = A_kB_k + H_k . 1$

On solving $C_k = A_k + B_k$ - An Or operation

The adder element implementing both the arithmetic and logical functions can be implemented as shown in the figure 6.12.

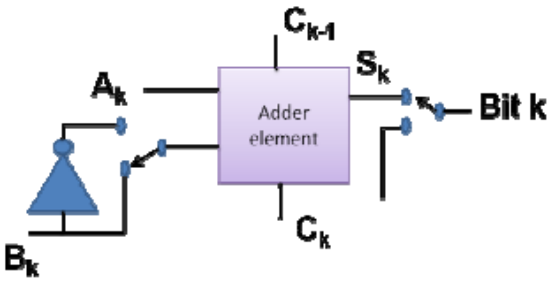


Figure 6.12: 1-bit adder element

The above can be cascaded to form 4-bit ALU.

Implementing ALU functions with an adder:

An ALU must be able to add and subtract two binary numbers, perform logical operations such as And, Or and Equality (Ex-or) functions. Subtraction can be performed by taking 2's complement of the negative number and perform the further addition. It is desirable to keep the architecture as simple as possible, and also see that the adder performs the logical operations also. Hence let us examine the possibility.

The adder equations are:

Sum $S_k = H_kC_{k-1}' + H_k'C_{k-1}$

New carry $C_k = A_kB_k + H_k C_{k-1}$

Where

Half sum $H_k = A_k'B_k + A_k B_k'$

Let us consider the sum output, if the previous carry is at logical 0, then

$S_k = H_k . 1 + H_k' . 0$

$S_k = H_k = A_k'B_k + A_k B_k'$ – An Ex-or operation

Now, if C_{k-1} is logically 1, then

$S_k = H_k . 0 + H_k' . 1$

Q.8 a. Write the circuit of one transistor dynamic RAM cell and explain briefly read and write functions.

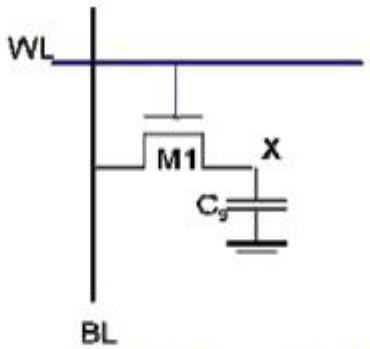
Working

- Row select (RS) = high, during write from R/W line Cm is charged
- data is read from Cm by detecting the charge on Cm with RS = high
- cell arrangement is bit complex.
- solution: extend the diffusion area comprising source of pass transistor, but Cd<<< Cgchannel
- another solution : create significant capacitor using poly plate over diffusion area.
- Cm is formed as a 3-plate structure
- with all this careful design is necessary to achieve consistent readability

Dissipation

- no static power, but there must be an allowance for switching energy during read/write

Circuit diagram



1T Dynamic RAM Cell

b. Explain the optimization of CMOS Inverters.

Text 1 – 10.1.1.1 THE CMOS Inverter, Figure 10.2.

Q.9 a. Explain the different requirements of large system designs in silicon.

Text1 – 10.8.

b. Explain how the interface with the fabrication house designer must establish.
Text1 – 10.10.

Text Book

1. Basic VLSI Design, Douglas A. Pucknell and Kamran Eshraghian, PHI, 3rd Edition, 2007