Q.2a. Give the classification of different IC technologies.

Integrated circuits offer a wide range of applications and could be broadly classified as:

Digital ICs

Linear ICs

Based upon the above requirements, two distinctly different IC technology namely, Monolithic technology and Hybrid technology have been developed.

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is more adaptable to small quantity custom circuits. Based upon the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (using FET). Bipolar and unipolar ICs may further be classified depending upon the isolation technique or type of FET used as in Fig. 1.1.

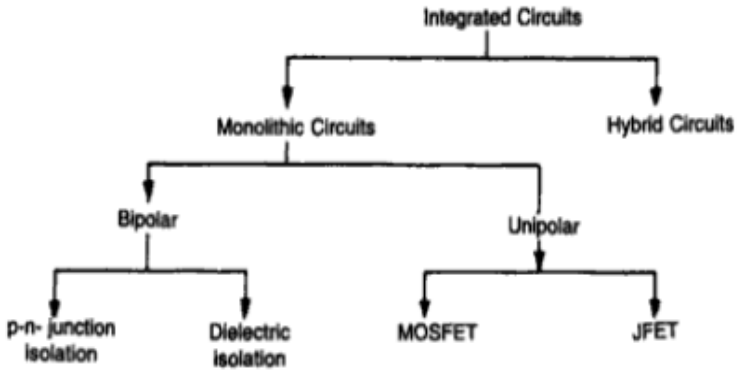


Fig. 1.1 Classification of ICs

b.For a differential amplifier using ideal op-amp(Shown in Fig. 2)

(i) Find the output voltage v_o

(ii) Show that the output corresponding to common-mode voltage $v_{CM} = \frac{(v_1 - v_2)}{2}$ **is zero if** $\frac{R'}{R} = \frac{R_2}{R_1}$

(iii) Find CMRR of the amplifier if $\frac{R'}{R} \neq \frac{R_2}{R_1}$ **(12)**

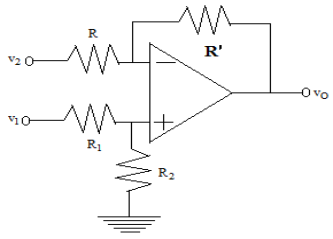


Fig.2

Solution

The voltage at the non-inverting input terminal is $\frac{R_2}{R_1 + R_2} v_1$. Using principle of superposition and Eqs. (2.4) and (2.20), we have

(a) $v_o = -\frac{R'}{R} v_2 + \left(\frac{R + R'}{R}\right)\left(\frac{R_2}{R_1 + R_2} v_1\right)$ (2.38)

(b) $v_{CM} = \frac{1}{2}(v_1 + v_2)$ and $v_d = (v_1 - v_2)$

So, $v_1 = v_{CM} + \frac{v_d}{2}$ and $v_2 = v_{CM} - \frac{v_d}{2}$

v_o from Eq. (2.38) is,

$$v_o = -\frac{R'}{R}\left(v_{CM} - \frac{v_d}{2}\right) + \frac{R_2}{R}\,\frac{R+R'}{R_1+R_2}\left(v_{CM} + \frac{v_d}{2}\right)$$

$$= \left(\frac{R_2}{R}\,\frac{R+R'}{R_1+R_2} - \frac{R'}{R}\right)v_{CM} + \left(\frac{R'}{R} + \frac{R_2}{R}\,\frac{R+R'}{R_1+R_2}\right)\frac{v_d}{2} \qquad (2.39)$$

Now, if $\frac{R'}{R} = \frac{R_2}{R_1}$, we get,

$$\frac{R'}{R} + 1 = \frac{R_2}{R_1} + 1$$

or, $$\frac{R'+R}{R} = \frac{R_1+R_2}{R_1}$$

So, from Eq. (2.39) the term corresponding to v_{CM} is zero, and

$$v_o = \left(\frac{R'}{R} + \frac{R_2}{R_1}\right)\frac{v_d}{2} = \left(\frac{R_2}{R_1}\right)v_d \qquad (2.40)$$

(c) CMRR $= \frac{A_{DM}}{A_{CM}}$

From Eq. (2.39), find (i) $A_{DM} = v_o/v_d$ by putting $v_{CM} = 0$
and (ii) $A_{CM} = v_o/v_{CM}$ by putting $v_d = 0$
then we get

$$\text{CMRR} = \frac{R'(R_1+R_2) + R_2(R+R')}{R'(R_1+R_2) - R_1(R+R')} \qquad (2.41)$$

Q.3 a. Draw and explain the circuit diagram of the voltage to current converter (Transconductance Amplifier). (8)

Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible.

V-I Converter with floating load
V-I Converter with grounded load

Figure 4.8 (a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \qquad (\text{as } I_B^- = 0)$$

or, $$i_L = \frac{v_i}{R_1} \quad (4.27)$$

That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in Fig. 4.8 (b). Let v_1 be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L \quad (4.28)$$

or, $$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or, $$v_i + v_o - 2v_1 = i_L R$$

Therefore, $$v_1 = \frac{v_i + v_o - i_L R}{2} \quad (4.29)$$

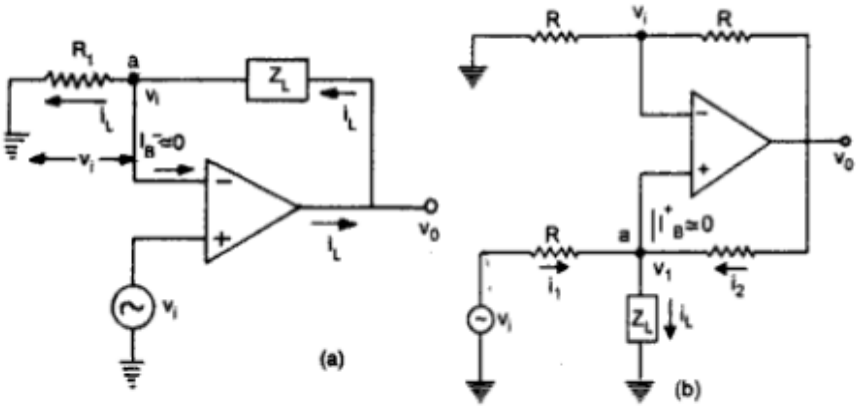


Fig. 4.8 Voltage to current converter with (a) floating load (b) grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

$$v_o = 2v_1 = v_i + v_o - i_L R$$

that is, $$v_i = i_L R$$

or, $$i_L = \frac{v_i}{R} \quad (4.30)$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

b.Explain the following non-ideal dc characteristics of real op-amp:

(i) Input bias current
(ii) Input offset current
(iii) Input offset voltage
(iv) Thermal drift

Q.3 b. Refer Section 3.2 of textbook Linear Integrated Circuits, Revised Second Edition, D Roy Choudhury, Shail B. Jain, New Age International Publishers.

Q.4 a. Design a circuit diagram of non-inverting integrator, also derive it's input output relation.

The voltage at the (+) input terminal of the op-amp due to the potential divider is,

$$V(+) = \frac{1/sC}{R + 1/sC} V_i(s) \qquad (4.95)$$

The output voltage $V_o(s)$ for the non-inverting amplifier is

$$V_o(s) = \left(1 + \frac{1/sC}{R}\right) V(+)$$

$$= \frac{1}{sRC} V_i(s) \qquad (4.96)$$

Hence in time-domain, we get,

$$v_o = \frac{1}{RC} \int v_i \, dt$$

Note that there is no phase inversion in a non-inverting integrator.

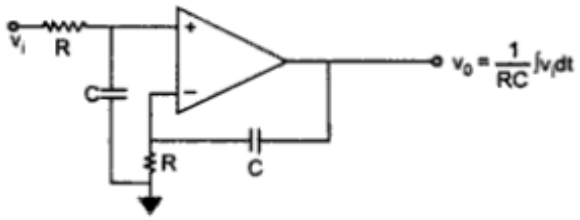


Fig. 4.28 Noninverting integrator circuit

b.Design a circuit diagram of zero crossing detector using op-amp as comparator.

Zero Crossing Detector

The basic comparators of Fig. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that V_{ref} is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.

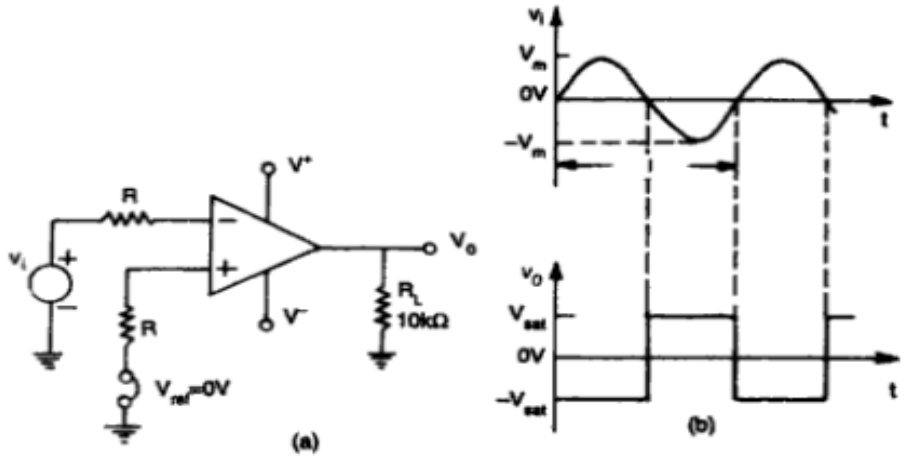


Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

Q.5 a. Describe the pin diagram of 555 timer IC and give examples of its application.

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8–pin circular style, TO–99 can or 8–pin mini DIP or as 14–pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

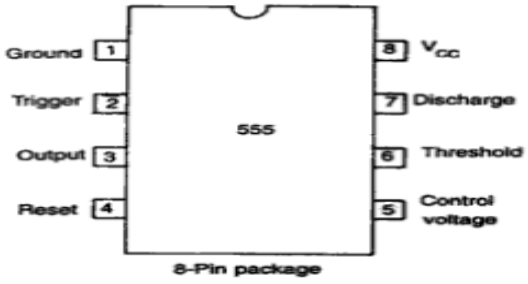


Fig. 8.1 Pin diagram

The 555 timer can be used with supply voltage in the range of + 5 V to + 18 V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply

voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

b.Design a circuit diagram of 3 bit R-2R Ladder DAC and also derive it's input output relation.

10.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 10.5 (a), where the switch position $d_1\ d_2\ d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 10.5 (b) and finally to Fig. 10.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

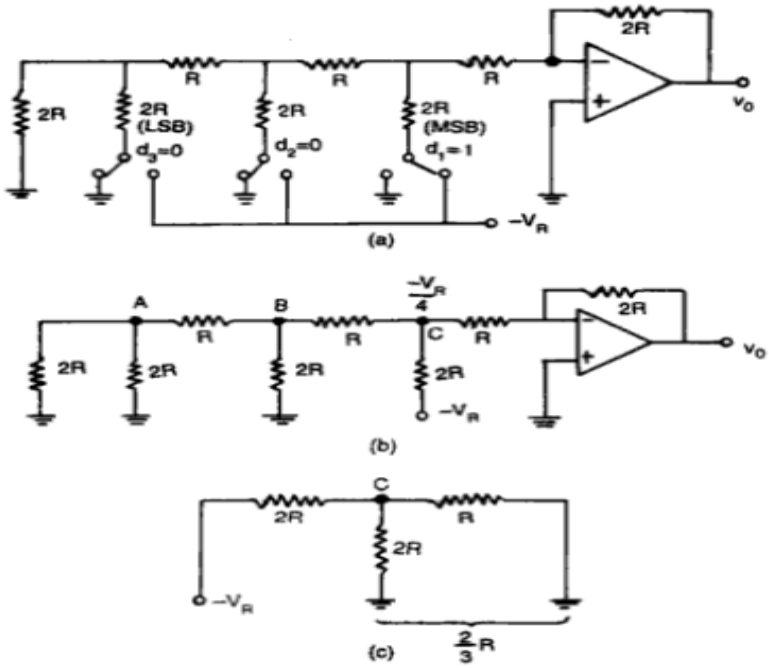


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

c.Explain the working of Series Op-Amp voltage regulator with its circuit diagram.

Ans: Refer Section 3.2 of textbook Linear Integrated Circuits, Revised Second Edition, D Roy Choudhury, Shail B. Jain, New Age International Publishers.

Q.6a. What are alphanumeric codes? Give suitable example and numbers of bits in the code?

Ans a. Codes that represent letters of the alphabet, punctuation marks and other special characters as well as numbers are called as alphanumeric codes.
Most widely used alphanumeric code is the American Standard Code for information Interchange(ASCII) and it is of 7 bits. $2^7 = 128$ possible code groups.

b.What is the advantage and disadvantage of encoding a decimal number in BCD as compared with straight binary?

Ans The main advantage of the BCD code is the relative ease of converting to and from a decimal compared to straight binary conversion to and from decimal.
Disadvantage is that we require a large number of bits for BCD representation
$137_{10} = 10001001_2$ (binary, 7 bits)
$137_{10} = 0001\ 0011\ 0111$ (BCD, 12 bits)

c. Perform the following conversions:

(i) $(1011.0011)_2 = (\quad)_{10}$ **(ii) $(204.125)_{10} = (\quad)_{16}$**
(iii) $(25.25)_{10} = (\quad)_2$ **(iv) $(B4.C9)_{16} = (\quad)_{10}$**
(v) $(5431.4)_8 = (\quad)_{16}$

Ans **(i)** $(1011.0011)_2 = (28.1875)_{10}$ (ii) $(204.125)_{10} = (CC.2)_{16}$
(iii) $(25.25)_{10} = (11001.01)_2$ (iv) $(B4.C9)_{16} = (180.78515)_{10}$
(v) $(5431.4)_8 = (B19.8)_{16}$

Q.7 a. What are the advantages of digital systems over analog systems?

Ans Advantages of digital systems:
(i) Digital systems are easier to design
(ii) Information storage is easy
(iii) Accuracy and precision are greater
(iv) operation can be programmed
(v) Less affected by noise
(vi) More digital circuits can be fabricated on IC Chips.

b.Minimize the given expression by using Boolean algebra, $Y = B(1+C)(B+\overline{B}C)(B+D)$

Ans. B(1+C)(B+B'C)(B+D)
= B(B+C)(B+D)

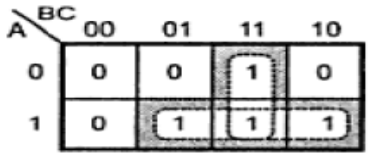
=(BB+BC)(B+D)
=(B+BC)(B+D)
=B(1+C)(B+D)
=B(B+D)
=BB+BD=B(1+D)
=B

c.Design a combinational logic circuit with three input variables(say A, B, C) that produce a logic 1 output (say Y)when more than one input variables are logic 1.Draw the truth table and minimize expression using k-map.

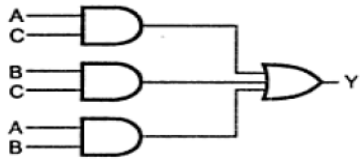
Ans.

c. The truth table for given problem is shown below, A, B and C as input and Y output

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



Logic diagram

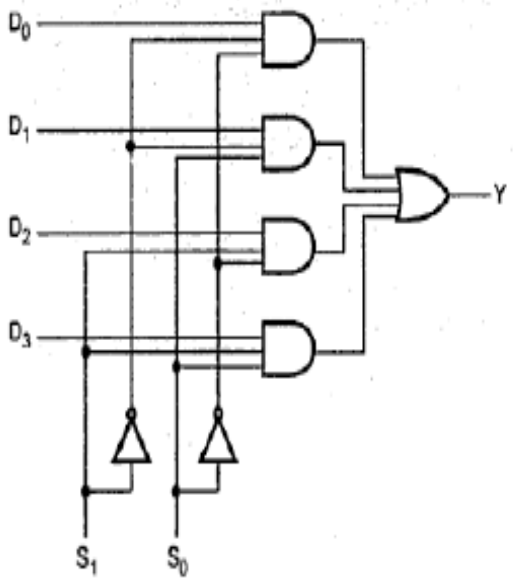


From truth table solving k-map we get, Y= AC + BC + AB and logic diagram as shown above

Q.8 a. What is Multiplexer? Draw the logic diagram and functional table for the 4×1 MUX.

Ans. Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a

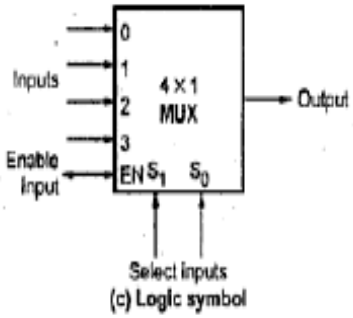
single output line. The basic multiplexer has several data-input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.. Therefore, multiplexer is 'many into one' and it provide the digital equivalent of anlog selection switch.4 to one line MUX is shown below :



(a) Logic diagram

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

(b) Function table



(c) Logic symbol

b. Design a Full Adder Circuit using two Half adder circuits and other basic gate?

Ans.

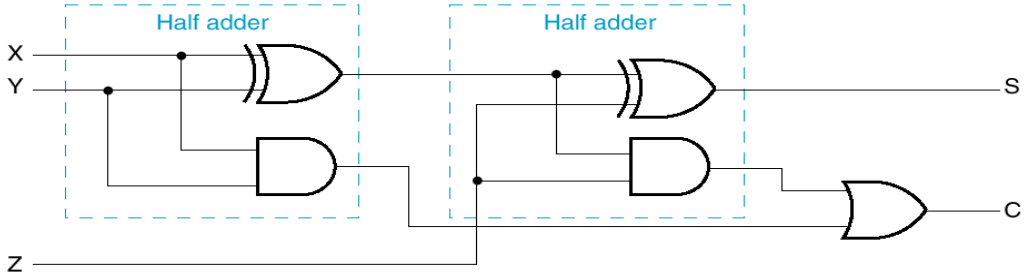


Fig. 3-27 Logic Diagram of Full Adder

Truth Table of Full Adder

Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$
$$= X \oplus Y \oplus Z$$

$$C = XY + XZ + YZ$$
$$= XY + Z(X\bar{Y} + \bar{X}Y)$$
$$= XY + Z(X \oplus Y)$$

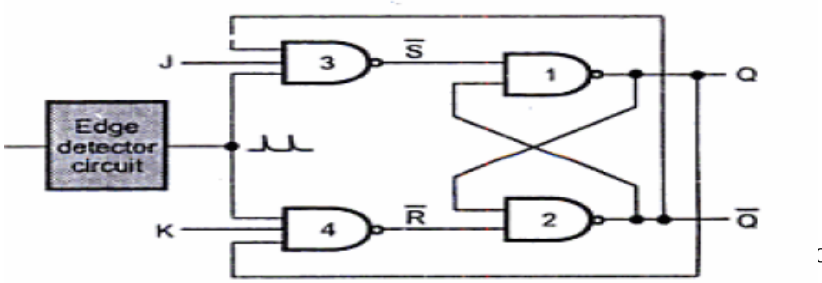
Q.9 a. Compare between Synchronous sequential circuits and asynchronous sequential circuits?

Ans

Synchronous sequential circuits	Asynchronous sequential circuits
In synchronous circuits, memory elements are clocked flip-flops.	In asynchronous circuits, memory elements are either unclocked flip-flops or time delay elements.
In synchronous circuits, the change in input signals can affect memory element upon activation of clock signal.	In asynchronous circuits change in input signals can affect memory element at any instant of time.
The maximum operating speed of clock depends on time delays involved	Because of absence of clock, asynchronous circuits can operate faster than synchronous circuits.
Easier to design.	More difficult to design.

b.Draw the circuit diagram of J-K flip-flop using NAND gate and draw the truth table and excitation table of J-K flip-flop.

J-K flip-flop using nand gate and draw the truth table and exitaion table of J-K flip-flop.



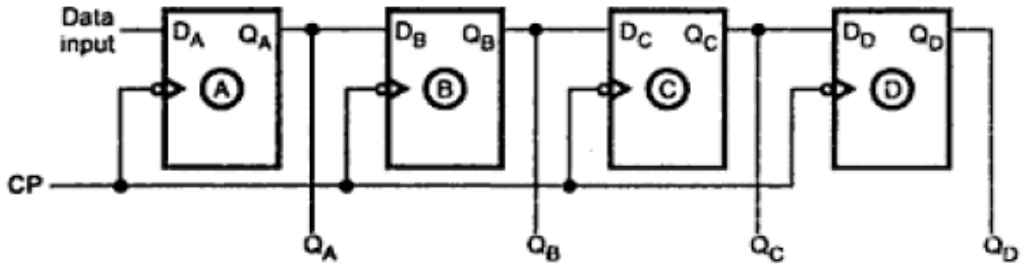
ɔn Table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

c. Explain and draw 4 bit Serial In / Parallel Out Shift Register, show the status of register at various clock pulses if data 10111 is fed into it.

Ans. 4 bit Serial In / Parallel Out Shift Register



Textbook

1. **Linear Integrated Circuits, Revised Second Edition, D Roy Choudhury, Shail B. Jain, New Age International Publishers.**

2. **Digital Systems – Principles and Applications, Ninth Edition, Ronald J Tocci, Neal S Widmer and Gregory L. Moss, Pearson Education, 2008**