Q.2 a. State and explain the Reciprocity Theorem and Thevenins Theorem.

Answer:

a. Reciprocity Theorem:

If we consider two loops A and B of network N and if an ideal voltage source E in loop A produces current I in loop B, then interchanging positions, if an identical source in loop B produces the same current I in loop A, the network is said to be reciprocal. A linear n/w is said to be reciprocal or bilateral if it remains invariant due to the interchange of position of cause and effect in the network.

Thevenins Theorem states that "Any linear circuit containing several voltages and resistances can be replaced by just a Single Voltage in series with a Single Resistor". In other words, it is possible to simplify any "Linear" circuit, no matter how complex, to an equivalent circuit with just a single voltage source in series with a resistance connected to a load as shown below. Thevenins Theorem is especially useful in the Circuit Analysis.

b. In the circuit shown below, determine the value of V_X.

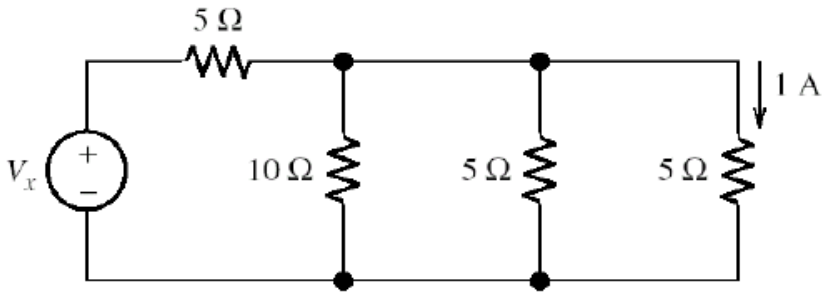
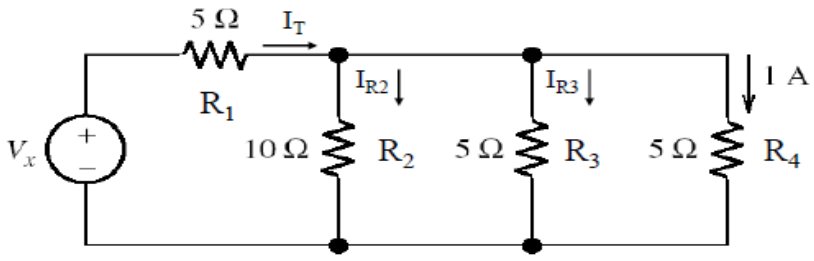


Fig.3

Answer:



Ohm's Law:

$V_{R4} = (1A)(5\Omega) = 5V = V_{R2} = V_{R3}$

$I_{R2} = 5V/10\Omega = 0.5A$

$I_{R3} = 5V/5\Omega = 1A$

KCL: $I_T = I_{R2} + I_{R3} + I_{R4} = 0.5A + 1A + 1A = 2.5A$

Ohm's Law: $V_{R1} = I_T R_1 = (2.5A)(5\Omega) = 12.5V$

KVL: $V_x = V_{R1} + V_{R4} = 12.5V + 5V = 17.5V$

c. Define the term: electrical current, direct current and alternating current.

Answer:

ELECTRICAL CURRENT: Electrical current is the time rate of flow of electrical charge through a conductor or circuit element. The units are amperes (A), which are equivalent to coulombs per second (C/s).

DIRECT CURRENT: When a current is constant with time, we say that we have direct current, abbreviated as dc.

ALTERNATING CURRENT: current that varies with time, reversing direction periodically, is called alternating current, abbreviated as ac.

Q.3 a. Explain the different biasing of P-N junction diode. Also draw VI characteristics. (10)

Answer:

Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities:

1. The Unbiased diode condition or no bias ($V_D = 0$)
2. Forward bias diode condition ($V_D > 0$)
3. Reverse bias diode condition ($V_D < 0$)

<u>The Unbiased Diode (V = 0V):</u>

The term "bias" refers to the application of an external voltage across the two terminals of the device to extract a response. Bias is a potential used to control the width of a depletion layer, and thus its resistance. As the width of a depletion layer increases, its resistance increases. As the width of a depletion layer decreases, its resistance decreases.

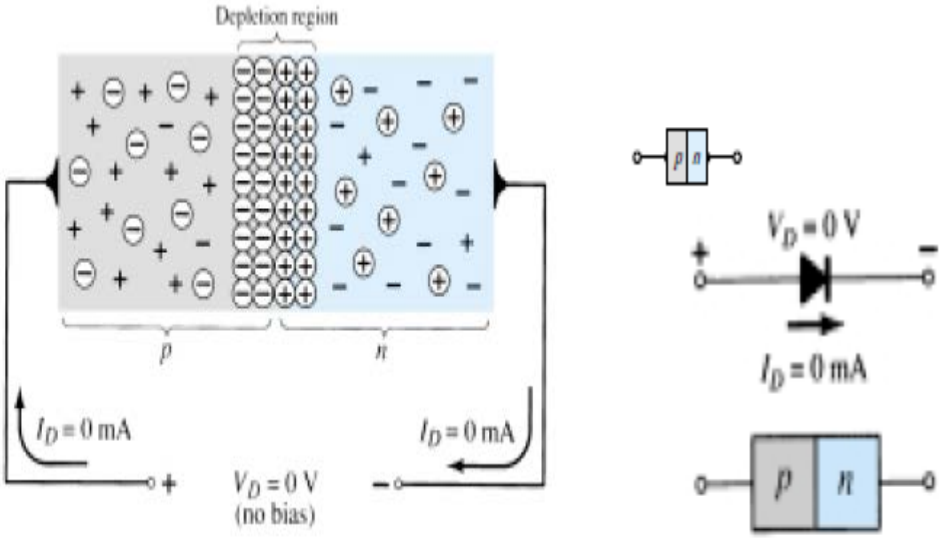


Fig 15: Unbiased pn junction diode.

Fig 15 is an unbiased pn junction diode. The circled plus sign represents donor atom and circled minus sign are acceptor atom. Plus sign represent the hole and free electros are represented by minus sign.

In unbiased condition no external voltage applied to the pn junction diode. At the instant the two materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction, as shown in Fig: 15.

This region of uncovered positive and negative ions is called the depletion region or potential barrier due to the "depletion" of free carriers in the region.

The potential barrier that now exists discourages the diffusion of any more majority carriers across the junction. However, the potential barrier helps minority carriers (few free electrons in the P-region and few holes in the N-region) to drift across the junction. Then an "Equilibrium" or balance will be established when the majority carriers are equal and both moving in opposite directions, so that the net result is zero current flowing in the circuit. When this occurs the junction is said to be in a state of "**Dynamic Equilibrium**".

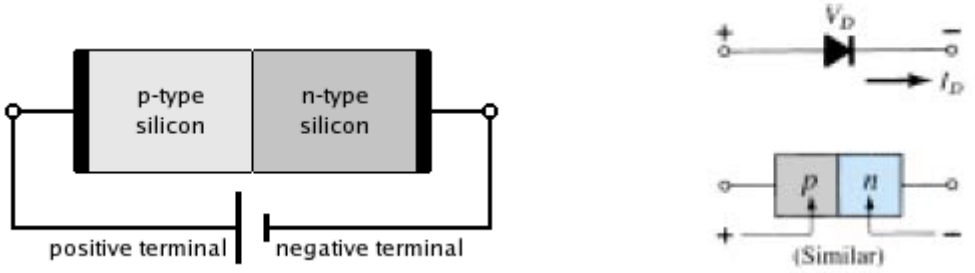
- In unbiased condition current across the diode is Zero.

Forward bias condition ($V_D > 0$):

A forward bias or "on" condition is established by applying the positive potential to the p-type material and the negative potential to the n-type material as shown in Fig: 16. Forward bias is a potential that reduces the size (and resistance) of a depletion layer The application of forward bias potential V_D will force electron in the n-type material and holes in the p-

type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig: 18.

The resulting minority carrier flow of electrons from the p-type material to the n-type material has not changed in magnitude but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. As the applied bias increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, resulting an exponential rise in current as shown in fig: 19.



(a) (b)

Fig 16: (a) Symbol of p-n junction in forward bias (b) direction of resulting current

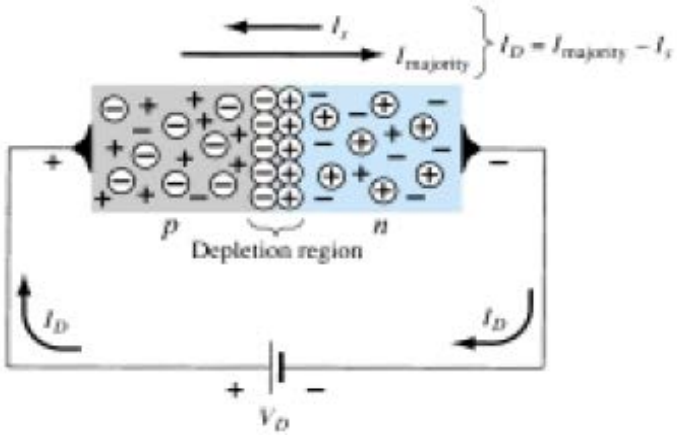


Fig 17: Internal distribution of charge under forward bias

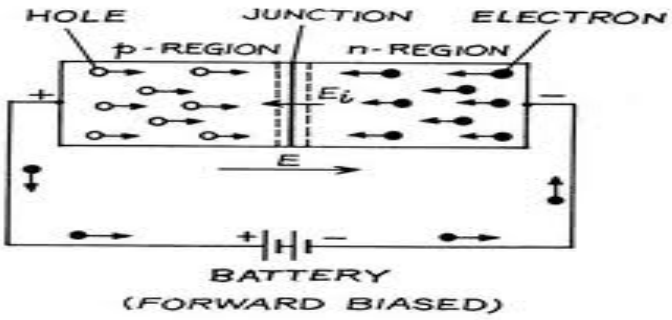


Fig 18: free electrons and holes movement in forward bias pn junction diode.

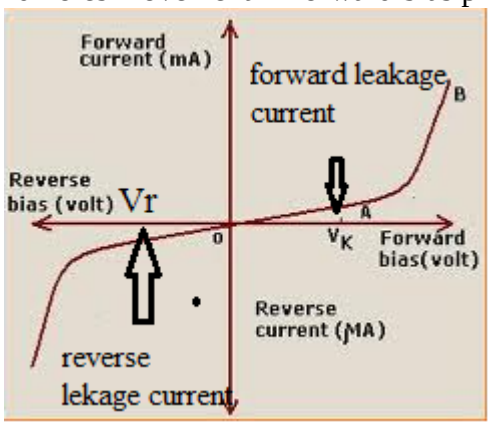


Fig 19: V-I characteristics of pn junction diode.

Where **V_K** is threshold or cut in voltage. For silicon it is 0.7 V and for germanium it is 0.3V

Vr is reverse break down voltage

Reverse bias condition ($V_D < 0$):

If an external potential of *V* volts is applied across the *p*-*n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material as shown in Fig 20, the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of "free" electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. **The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero** as shown in Fig. 21.

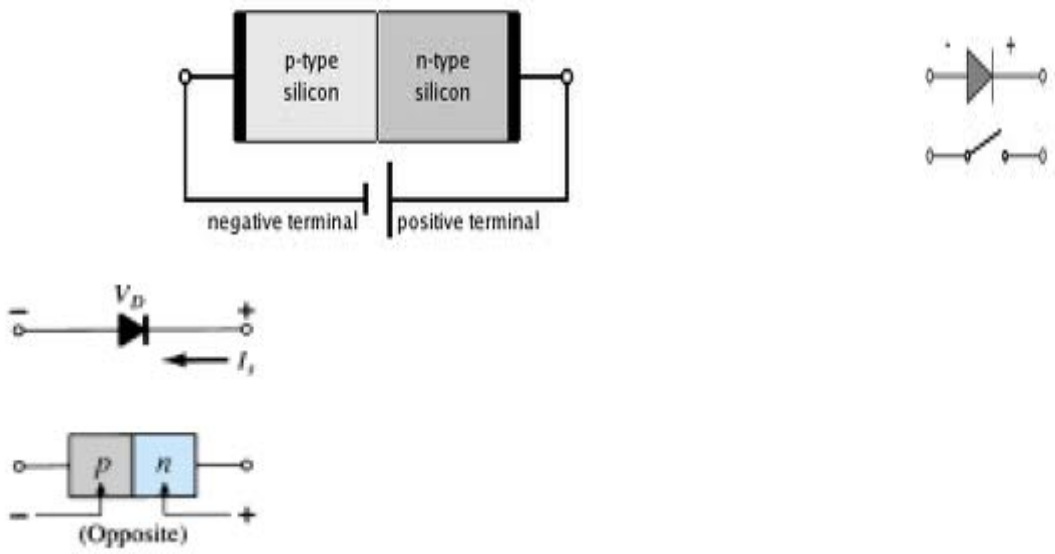


Fig 20: Reverse bias condition for pn junction diode

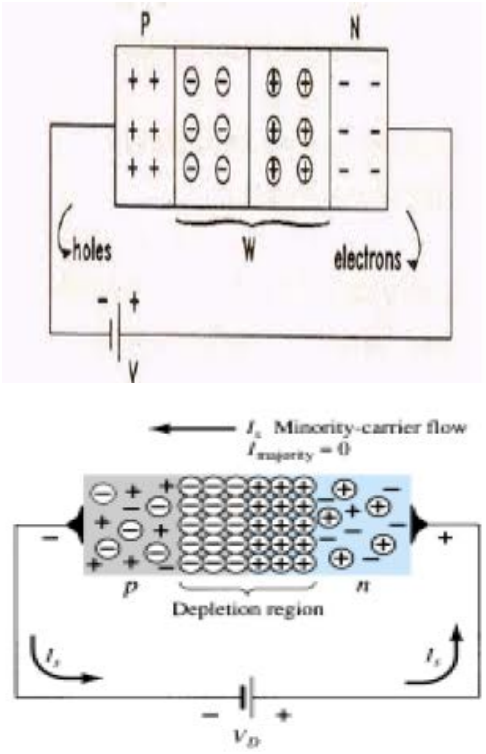


Fig. 21: Reverse biased pn junction diode.

The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude indicated in Fig. 17 with no applied voltage.

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by Is. I_s is caused by the thermally produced minority carriers.

The reverse saturation current is seldom more than a few microamperes except for high-power devices. The term *saturation* comes from the fact that it reaches its maximum level quickly and does not change significantly with increase in the reverse-bias potential, as shown on the diode characteristics of Fig. 19 for *VD* < 0 V. The reverse-biased conditions are depicted in Fig. 20 for the diode symbol and *p-n* junction. Note, in particular, that the direction of *Is* is against the arrow of the symbol.

b. For the zener diode network shown in figure below determine V_L, V_R, I_Z, and I. **(6)**

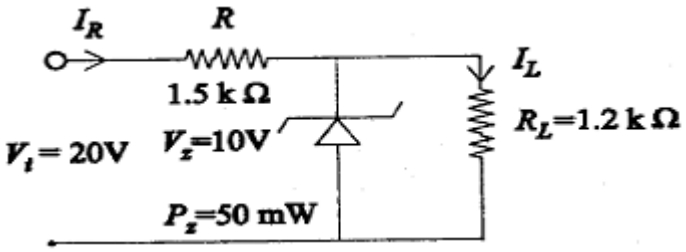


Fig.4

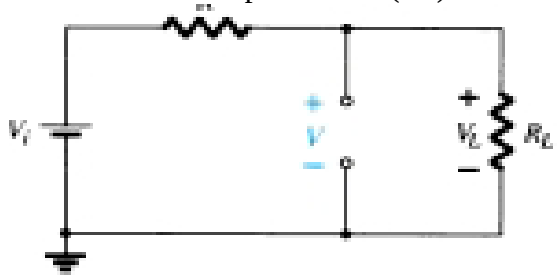
Answer:

Solution: $V = R_L V_i / R + R_L$

$= (1.2K\Omega \times 20) / (1.5\ K\Omega + 1.2\ K\Omega)$

$= 8.8$ V

As we get $V < V_Z$; zener diode works as open circuit (off) as shown in figure;



$V_L = V = 8.8$v

$V_R = Vi – VL = 11.2$ V

Iz = 0

$I_R = V_R / R = 11.2/1.5$ 7.4 mA

Q.4 a. A transistor used in CE arrangement has the following set of h parameters when the d.c. operating point is V_{CE} = 10 volts and I_C = 1 mA :

h_{ie} = 2000 Ω; h_{oe} =10^{-4} mho; h_{re} = 10^{-3}; h_{fe} = 50
Considering the a.c. load seen by the transistor is r_L = 600 Ω. Determine approximate values of the following using reasonable approximations:
(i) input impedance (ii) current gain and (iii) voltage gain (8)

Answer:

Solution. (*i*) Input impedance is given by :

$$Z_{in} = h_{ie} - \frac{h_{re}\,h_{fe}}{h_{oe} + \frac{1}{r_L}} = 2000 - \frac{10^{-3} \times 50}{10^{-4} + \frac{1}{600}} \quad \ldots (i)$$

$$= 2000 - 28 = 1972\ \Omega$$

The second term in eq. (*i*) is quite small as compared to the first.

$$\therefore \quad Z_{in} \simeq h_{ie} = 2000\ \Omega$$

(*ii*) Current gain, $A_i = \frac{h_{fe}}{1 + h_{oe} \times r_L} = \frac{50}{1 + (600 \times 10^{-4})} = 47$

If $h_{oe}\, r_L << 1$, then $A_i \simeq h_{fe} = 50$

(*iii*) Voltage gain, $A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \frac{-50}{1972\left(10^{-4} + \frac{1}{600}\right)} = -14.4$

The negative sign indicates that there is 180° phase shift between input and output. The magnitude of gain is 14.4. In other words, the output signal is 14.4 times greater than the input and it is 180° out of phase with the input.

b. Explain the working of BJT as a switch.

Answer:

Consider the circuit shown on Figure 8. If the voltage v_i is less than the voltage required to forward bias the base-emitter junction then the current $I_B = 0$ and thus the transistor is in the cutoff region and $I_C = 0$. Since $I_C = 0$ the voltage drop across *Rc* is zero and so *Vo=Vcc.*

If the voltage v_i increases so that V_{BE} forward biases the base-emitter junction the transistor will turn on and

$$I_B = \frac{v_i - V_{BE}}{R_B} \tag{1.6}$$

Once the transistor is on we still do not know if it is operating in the active region or in the saturation region. However, KVL around the C-E loop gives

$$V_{CC} = I_C R_C + V_{CE} \tag{1.7}$$

And so

$$V_{CE} = V_{CC} - I_C R_C \tag{1.8}$$

Note that $V_{CE} = V_0$ as shown on Figure 8.

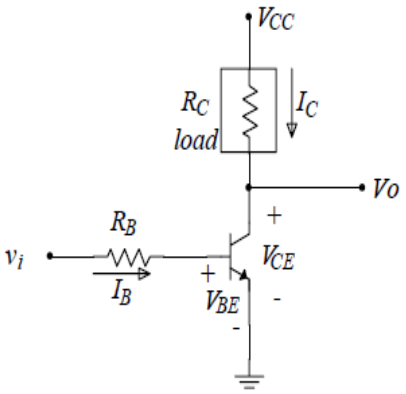


Figure 8. npn BJT switch circuit

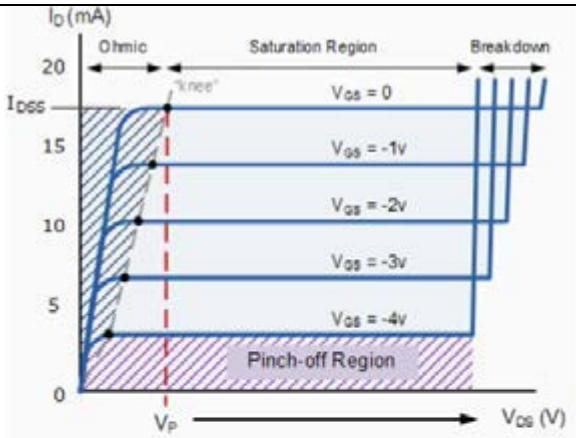
Q.5 a. Draw and explain in brief the output characteristics (V_{DS} Vs I_D) and transfer characteristics of n-channel JFET. Also show that μ = rd x gm.

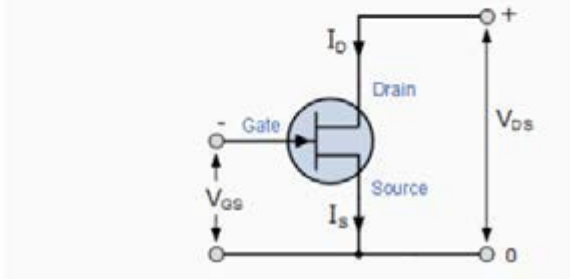
Answer:

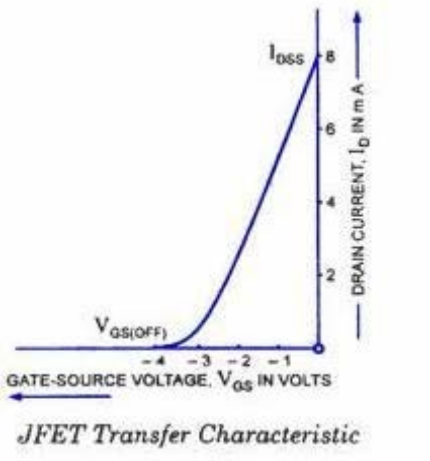
Drain resistance rd = $\Delta V_{DS} / \Delta I_D$

Tran conductance gm= $\Delta I_D / \Delta V_{GS}$

Amplification factor $\mu = \Delta V_{DS} / \Delta V_{GS} = (\Delta V_{DS} / \Delta I_D) \text{ X } (\Delta I_D / \Delta V_{GS}) = \text{rd X gm}$







JFET Transfer Characteristic

b. Assuming Si transistor with β= 100 Calculate V_{CE}, I_C for the following circuit

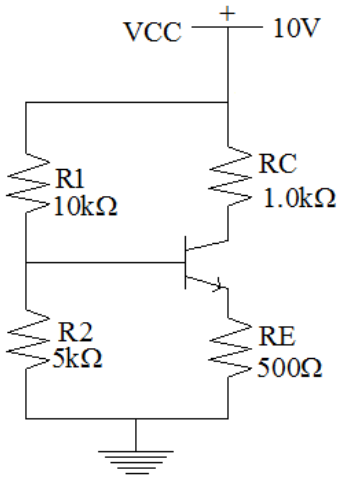


Fig.5

Answer:

VB = [R2 / R1 + R2] x Vcc=3.33V

VE= VB – VBE= 3.3 - 0.7 = 2.63 V

IE= VE / RE = 2.63/ 500 = 5.26 mA IB= IE / (1+ β) = 5.26 mA /

101 =52.08 μA

IC= β. IB = 100 X 52.08 μA **= 5.208 mA**

KVL to collector: VCC – IC.RC – VCE – IE.RE =0

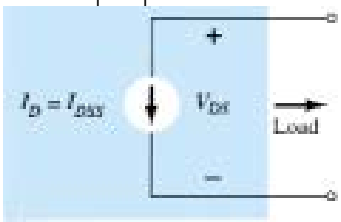
VCE = VCC – IC.RC — IE.RE

VCE = 2.162 V

c. Define the following: Darin to source saturation current of JFET, Pinch off voltage of JFET, Voltage controlled resistance of JFET.

Answer:

I_{DSS} : IDSS is the maximum drain current for a JFET and is defined by the conditions VGS = 0 V and VDS =|VP|.



Pinch off Voltage: If VDS is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P.

Voltage Controlled Resistance of JFET: The region to the left of the pinch-off

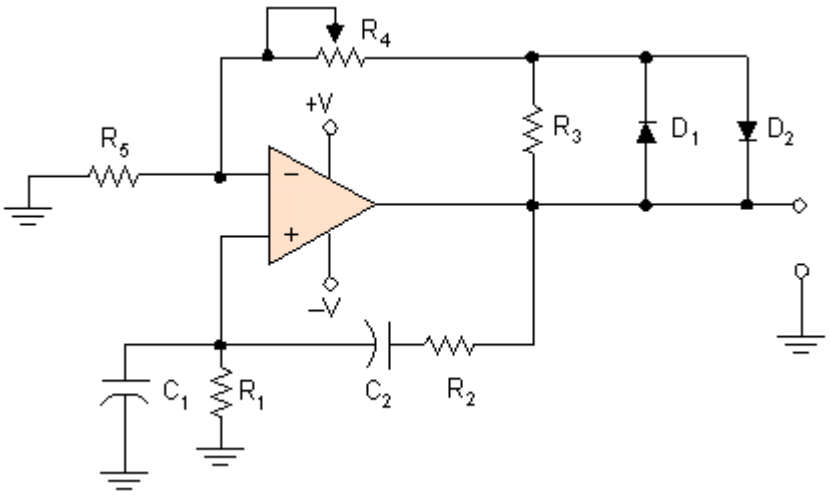
locus is referred to as the ohmic or voltage-controlled resistance region.

$$r_d = \frac{r_o}{(1 - V_{GS}/V_p)^2}$$

Q.6 a. Explain the working of Wein Bridge Oscillator.

Answer:

a. The Wien-bridge oscillator is a commonly used low-frequency oscillator. This circuit achieves regenerative feedback by introducing no phase shift (0°) in the positive feedback path. As shown in Figure 4, there are two RC circuits in the positive feedback path (output to noninverting input).



b. FIGURE -4 Wien-bridge oscillator.

The R_1C_1 circuit forms a low-pass filter, and the R_2C_2 circuit forms a high-pass filter. Both RC filters have the same cutoff frequency ($R_1C_1 = R_2C_2$). Combined, they create a band-pass filter. As you know, a band-pass filter has no phase shift in its pass-band. The circuit oscillates at the intersection of the high-pass and low-pass response curves. It is common to see trimmer potentiometers added in series with R_1 and R_2. They are used to fine-tune the circuit's operating frequency.

The negative feedback path is from the output to the inverting input of the op-amp. Note the differences from a normal negative feedback circuit. Two diodes have been added in parallel with R_3, as well as the potentiometer labeled R_4. The potentiometer is used to control the A_{CL} of the circuit. The diodes also limit the closed-loop voltage gain of the circuit. If the output signal tries to exceed a predetermined value $(V_{R4} + V_{R5})$ by more than 0.7 V, then the diodes conduct and limit signal amplitude. The diodes are essentially used as clippers.

Earlier we said that the Wien-bridge oscillator is a common low-frequency oscillator. As frequency increases, the propagation delay of the op-amp can begin to introduce a phase shift, which causes the circuit to stop oscillating. Propagation delay is the time required for the signal to pass through a component (in this case the op-amp). Most Wien-bridge oscillators are limited to frequencies below 1 MHz.

b. What are the advantages and disadvantages of negative feedback in amplifier?

Answer: **Advantages:**

1. Increased stability
2. Increased bandwidth
3. Less amplitude and harmonic distortion
4. Decreased noise
5. Less frequency distortion
6. Less phase distortion.
7. Input and output resistance can be modified as per requirement.

Disadvantage: Reduction in gain of amplifier

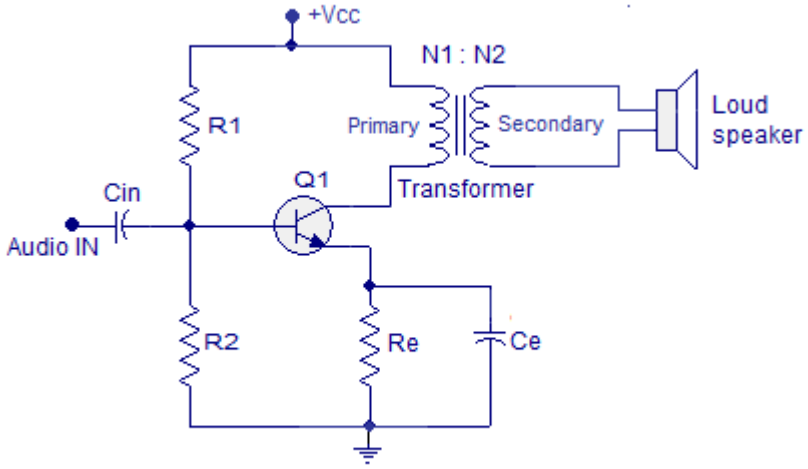
Q.7 a. Draw and explain the Transformer coupled Class A power amplifier. List the advantages and disadvantages also.

Answer:

Transformer coupled Class A power amplifier.

An amplifier where the load is coupled to the output using a transformer is called a transformer coupled amplifier. Using transformer coupling the efficiency of the amplifier can be improved to a great extend. The coupling transformer provides good impedance

matching between the output and load and it is the main reason behind the improved efficiency. Impedance matching means making the output impedance of the amplifier equal to the input impedance of the load and this is an important criterion for the transfer of maximum power. Circuit diagram of typical single stage Class A amplifier is shown in the circuit diagram below.



Tranformer coupled Class A amplifier www.circuitstoday.com

Impedance matching can be attained by selecting the number of turns of the primary so that its net impedance is equal to the transistors output impedance and selecting the number of turns of the secondary so that its net impedance is equal to the loudspeakers input impedance.

Advantages of transformer coupled amplifier.

- Main advantage is the improvement of efficiency.
- Provides good DC isolation as there is no physical connection between amplifier output and load. Audio signals pass from one side to other by virtue of induction.

Disadvantages of transformer coupled amplifier.

- It is a bit hard to make/find an exactly matching transformer.
- Transformers are bulky and so it increases the cost and size of the amplifier.
- Transformer winding does not provide any resistance to DC current. If any DC components if present in the amplifier output, it will flow through the primary winding and saturate the core. This will result in reduced transformer action.
- Transformer coupling reduces the low frequency response of the amplifier.
- Transformer coupling induces hum in the output.
- Transformer coupling can be employed only for small loads.

b. With the help of a neat diagram explain the functioning of Class-C power amplifier.

Answer: Refer Pages 306-307 from Text Book-I

Q.8 a. A certain BJT transistor has r_π = 2 kΩ and β = 50 at 1 MHz and β = 2.5 at 20MHz. Determine the values of f_T, f_B and c_π.

Answer: Refer Example 4.1, Page No. 249 from Text Book-I

b. With neat circuit diagram and frequency response, explain two stage RC coupled amplifier. What are its advantages and applications?

Answer:

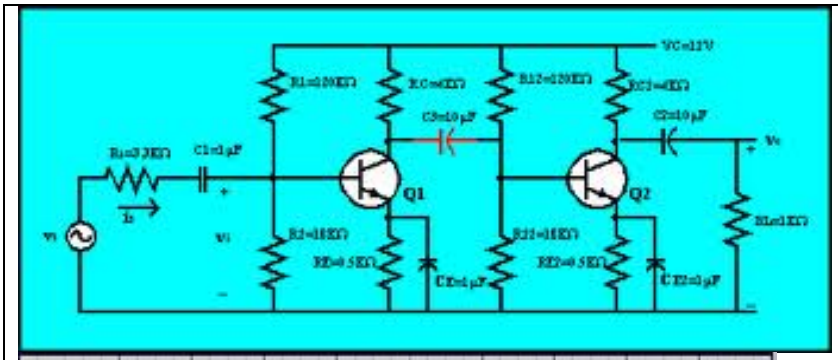
a. **Working Principle:** When a.c. signal is applied to the base of the first transistor, it is amplified and developed across the out of the 1st stage. This amplified voltage is applied to the base of next stage through the coupling capacitor Cc where it is further amplified and reappears across the out put of the second stage. Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gains can be obtained by connecting a number of amplifier stages in succession (one after the other). Resistance-Capacitance (RC) coupling is most widely used to connect the output of first stage to the input (base) of the second stage and so on. It is the most popular type of coupling because it is cheap and provides a constant amplification over a wide range of frequencies. Fig. shows the circuit arrangement of a two stage RC coupled CE mode transistor amplifier where resistor R is used as a load and the capacitor C is used as a coupling element between the two stages of the amplifier.

Frequency response curve

The curve representing the variation of gain of an amplifier with frequency is known as frequency response curve. It is shown in figure. The voltage gain of the amplifier increases with the frequency, f and attains a maximum value. The maximum value of the gain remains constant over a certain frequency range and afterwards the gain starts decreasing with the increase of the frequency. It may be seen to be divided into three regions. 1) Low frequency range (<50 Hz) 2) Mid frequency range (50 Hz to 20 KHz) and 3) High frequency range (> 20 kHz).

Advantages-

1. Requires no bulky or expensive components and no adjustment.
2. Small, light and inexpensive.
3. Overall amplification is higher than other couplings.
4. Wide frequency response.
5. Less frequency distortion.



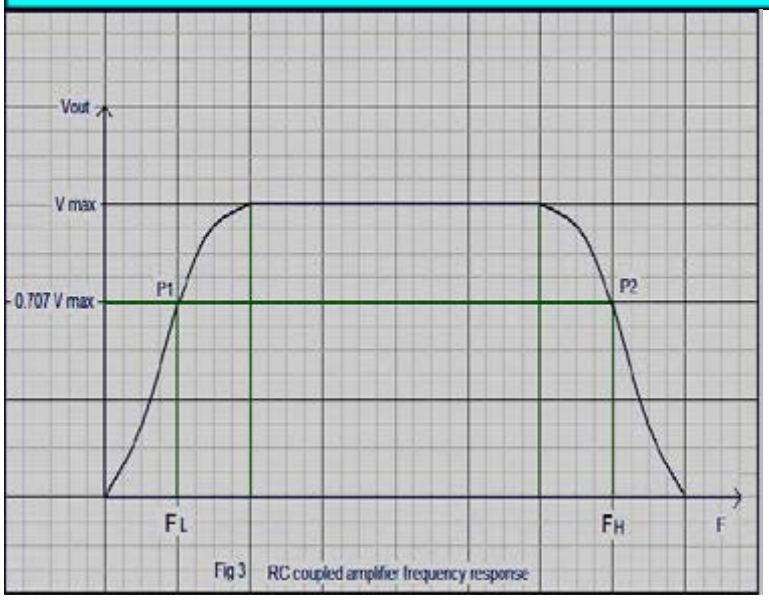


Fig 3 RC coupled amplifier frequency response

Q.9 a. What do you mean by Integrated Circuits? What are the advantages of ICs as compared to standard printed circuits?

Answer: Integrated Circuit is just a packaged electronic circuit.

ADVANTAGES:

1. Extremely small physical size.
2. Very less weight.
3. Reduced cost.
4. Extremely high reliability.
5. Increased speed.
6. Low power consumption.
7. Easy replacement.
8. Higher scale of production.

b. Explain in brief, the various steps involved in fabrication of ICs.

Answer:

The various steps involved in fabrication of ICs are- Explanation in brief about: Silicon wafer preparation, epitaxial growth, Oxidation, photolithography, etching, diffusion, ion implantation, metallization, interconnection, circuit probing, scribing and separating into chips, mounting and packaging and encapsulation.

TEXT BOOK

I. Electronic Devices and Circuits, 2009, I. J. Nagrath, PHI.