ROLL NO. _____

Code: AE05 **Subject: BASIC ELECTRONICS**

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **OCTOBER 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. In semiconductor the current is because of flow of _____

(A) only electrons **(B)** only holes
(C) both electrons and holes **(D)** photons

b. Cascode amplifier using BJT is composed of _____

(A) CE followed by CB **(B)** CB followed by CC
(C) CC followed by CE **(D)** CE followed by CC

c. Input impedance of FET is higher because of _____

(A) small gate current **(B)** large gate current
(C) drain current **(D)** drain to source voltage

d. Efficiency of Transformer Coupled Class A amplifier is _____

(A) 25 % **(B)** 78.5 %
(C) 50% **(D)** 90%

e. Ripple Factor for full wave rectifier without filter is _____

(A) 1.21 **(B)** 0.48
(C) 1.00 **(D)** 0.75

f. The oscillator which gives most stable frequency is _____

(A) Crystal oscillator **(B)** Wien Bridge oscillator
(C) RC phase shift oscillator **(D)** Hartley oscillator

g. Which statement is true for Bistable circuit _____

(A) has one stable state and one quasi stable state
(B) has two stable states
(C) has two quasi stable states
(D) does not need any external trigger for change of state.

h. Fermi level in intrinsic semiconductor at 0°K is _____

(A) near to valence band.
(B) near to conduction band.
(C) in the middle of energy gap between conduction band and valence band.
(D) inside the conduction band.

i. In a Master Slave flip flop circuit, master is enabled _____

(A) at positive trigger edge.
(B) at negative trigger edge.
(C) both positive and negative trigger edge.
(D) without any trigger.

j. Voltage Gain of the OP-AMP shown in Fig.1 with R_f=47 K and R_{in}=10 K is
(A) +4.7 **(B)** +5.7
(C) – 4.7 **(D)** +47

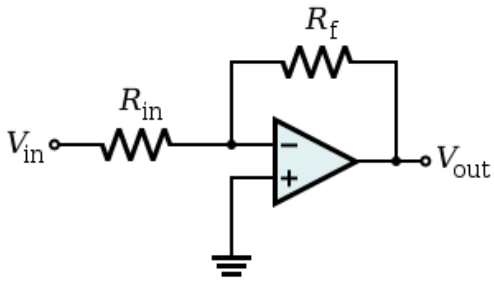

Fig.1

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Differentiate between Avalanche and Zener breakdown mechanisms. **(6)**

b. What is meant by stability factor S? Draw and explain the biasing circuit which gives the best stability. **(10)**

Q.3 a. Draw the h-Parameter equivalent circuit of a CE transistor amplifier and derive an expression of
(i) Its Voltage Gain and
(ii) Current Gain. **(8)**

b. Explain the circuit of Darlington Amplifier. Also obtain an expression for its overall current gain. **(8)**

Q.4 a. Describe the structure of JFET and also explain its working along with its characteristics. **(8)**

b. Draw the circuit of a class-B push-pull power amplifier and explain its operation. **(8)**

Q.5 a. For the circuit shown in Fig.2, identify the type of feedback and find out its effect upon Input Impedance, Output Impedance and Voltage Gain. **(8)**

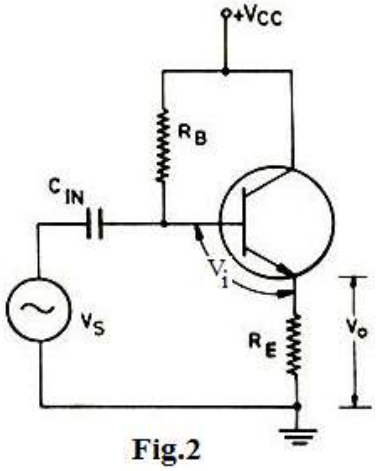

Fig.2

b. An amplifier with a 2.2KΩ input resistance and 40KΩ output resistance has a voltage gain of 80. The amplifier is now modified to provide 10% negative voltage feedback in series with the input. Calculate the following:
(i) the voltage gain with feedback.
(ii) the input resistance.
(iii) the output resistance.
If the feedback were effected using current series feedback which of the above (if any) would change? **(8)**

Q.6 a. Explain the distinguishing features of
(i) the Colpitts and
(ii) the Hertley oscillators. **(8)**

b. Explain how the IC 555 can be used as Astable multivibrator with the help of circuit diagram and waveforms. **(8)**

Q.7 a. With a neat diagram explain OP-AMP as
(i) Comparator
(ii) Sample and Hold circuit. **(12)**

b. Define
(i) Slew rate and
(ii) CMRR referred to OP-AMP. **(4)**

Q.8 a. What are the ideal characteristics of regulated power supply? Also draw the circuit of a series voltage regulator and describe its working. **(8)**

b. Draw the circuit of Sawtooth generator and explain its operation in detail. **(8)**

Q.9 a. State and Prove De-Morgan's Theorems. **(4)**

b. Simplify the following Boolean Function
$F(w,x,y,z) = \sum (0,1,2,4,5,6,8,9,12,13,14)$ **(4)**

c. Draw the truth table of a Full Adder circuit. Obtain the simplified expressions for the 'sum' and 'carry' outputs of the adder and draw its logic diagram. **(8)**