ROLL NO. _____

Code: AC07/AT07 Subject: COMPUTER ARCHITECTURE

AMIETE – CS/IT (OLD SCHEME)

Time: 3 Hours **OCTOBER 2012** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2 × 10)**

a. What is the equivalent of $(1010.011)_2$ in decimal?

(A) 10.375 **(B)** 10.03
(C) -2.03 **(D)** -2.375

b. How many possible outputs would a decoder have with a 6-bit binary input?

(A) 16 **(B)** 32
(C) 64 **(D)** 128

c. What is the control unit's function in the CPU?

(A) To transfer data to primary storage
(B) To store program instruction
(C) To perform logic operations
(D) To decode program instruction

d. How many address lines are needed to address each memory locations in a 2048 × 4 memory chip?

(A) 10 **(B)** 11
(C) 8 **(D)** 12

e. Which type of addressing is used in Stack-organized Computer?

(A) Indirect addressing **(B)** Two-addressing
(C) Zero addressing **(D)** Index addressing

f. In which addressing mode is the register transfer instruction AC ← M[ADR + XR]?

(A) Index addressing **(B)** Relative addressing
(C) Register indirect **(D)** Indirect address

g. What is the complement of $F = AB + C'D' + B'D$?

(A) $F' = (A' + B')(C + D)(B + D')$ **(B)** $F' = (A + B)(C' + D')(B' + D)$
(C) $F' = (AB)(C'D')(B'D)$ **(D)** $F' = A'B' + CD' + BD'$

h. Which of the following instruction is described by PC ← AR

(A) Load **(B)** Store
(C) Branch unconditional **(D)** Branch and save return address

i. Which of the following is faster than the remaining storage devices?

(A) Main memory **(B)** Cache Memory
(C) Disk Storage **(D)** Local Disks

j. Which type of the RAM is driven with rising clock edge?

(A) Synchronous DRAM
(B) Double data-rate synchronous DRAM
(C) Video RAM
(D) None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Given two binary numbers X = 1010100 and Y = 1000011, perform the subtraction
(i) X – Y (ii) Y – X using 2's complement. **(4)**

b. Design a 3-to-8-line decoder using NAND gates. **(6)**

c. What is a full adder? Draw and explain block diagram and logic diagram of full-adder circuit. **(6)**

Q.3 a. What is the difference between RAM and ROM? **(4)**

b. Draw a block diagram to illustrate the basic organisation system and explain function of various units. **(6)**

c. Show the block diagram of the hardware that implements the following register transfer statement:
yT : R2 ← R1, R1 ← R2 **(6)**

Q.4 a. What is a subroutine? Write a program to demonstrate the use of subroutines. **(8)**

b. Explain using a flowchart the steps carried during an interrupt cycle. **(8)**

Q.5 a. Write a program to evaluate (A+B) *(C+D) using
(i) zero address (ii) one address
(iii) two address (iv) three address instructions **(8)**

b. Explain all addressing modes, with a description of how operands are located. **(8)**

Q.6 a. Explain the four segment instruction pipeline with a flow chart and timing sequence. What are the major difficulties that cause the instruction pipeline to deviate from normal operation? **(8)**

b. What are the capabilities of address sequencing? **(4)**

c. Explain the microprogrammed control unit organization with a block diagram. **(4)**

Q.7 a. Explain Booth's algorithm for multiplication. Show the step by step process of (+15) * (-13) **(10)**

b. What is the disadvantage of strobe based communication? How is it overcome by handshaking? Describe how handshaking based communication works. **(6)**

Q.8 What is virtual memory? Describe how virtual memory is implemented using paging. Illustrate how logical address gets converted to physical address. **(16)**

Q.9 a. A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128k * 32.
(i) Format all pertinent information required to construct the cache memory.
(ii) What is the size of the cache memory? **(6)**

b. Explain DMA based data transfer with suitable block diagrams. **(10)**