Code: AC03/AT03   Subject: BASIC ELECTRONICS & DIGITAL CIRCUITS

AMIETE – CS/IT (OLD SCHEME)

Time: 3 Hours | **OCTOBER 2012** | **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated**

**Q.1   Choose the correct or the best alternative in the following: (2×10)**

a. The measurement of which one of the following will reveal the sign of charge carriers?

   (A) Conductivity   **(B)** Mobility
   (C) Hall Coefficient   **(D)** Diffusion Constant

b. The cascade amplifier is a multistage configuration of

   (A) CC-CB   **(B)** CE-CB
   (C) CB-CC   **(D)** CE-CC

c. The ideal op-amp has the following characteristics

   (A) $R_i=\infty$, $A_i=\infty$, $R_o=0$ **(B)** $R_i=0$, $A=\infty$, $R_o=0$
   (C) $R_i=\infty$, $A=\infty$, $R_o=\infty$ **(D)** $R_i=0$, $A=\infty$, $R_o=\infty$

d. Ripple frequency of the output waveform of a bridge rectifier when fed with a 50Hz sine wave is

   (A) 100 Hz   **(B)** 25 Hz
   (C) 50 Hz   **(D)** None of these

e. The sum S of A and B in a half adder can be implemented by using K NAND gates. The value of K is

   (A) 3   **(B)** 4
   (C) 5   **(D)** None of these

f. The reason for using Gray Code in K-map is

(A) gray code is efficient than binary code
(B) gray code provides cell values that differ in only one bit in adjacent cell
(C) no other code is available
(D) Any other code can be used.

g. The effective channel length of a MOSFET in Saturation decreases with increase in

(A) Gate Voltage   **(B)** Drain Voltage
(C) Source Voltage   **(D)** Base Voltage

h. Extremely low power dissipation and low cost per gate can be achieved in the following IC

(A) ECL   **(B)** CMOS
(C) TTL   **(D)** MOS

i. In which flipflop the output is transparent to input?

(A) JK FF   **(B)** T FF
(C) SR FF   **(D)** D FF

j. Which one of the following statement about RAM is not correct?

(A) RAM Stands for random access memory
(B) It is also called read/write memory
(C) When power supply is switched off, the information in RAM is usually lost
(D) The binary contents are entered or stored in the RAM chip during the Manufacturing

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the input and output characteristics of C B configuration.   **(8)**

b. A JFET amplifier with stabilized biasing circuit shown in Fig.1 has following parameters: **(8)**
$V_P = -2V$, $I_{DSS} = 5mA$, $R_L = 910\Omega$,
$R_F = 2.29k\Omega$, $R_1 = 12M\Omega$, $R_2 = 8.75M\Omega$
and $V_{DD} = 24V$. Determine the value
of drain current I_D at the operating point.
Also verify that FET will operate in
pinch-off region.

Fig.1
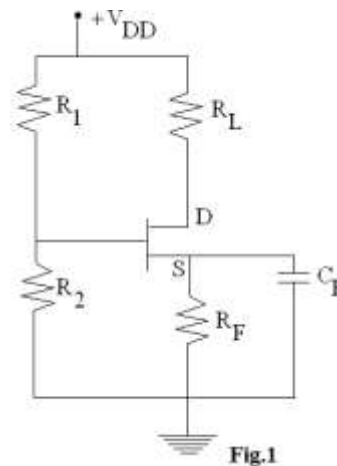
Q.3 a. Derive the general expression for Input impedance, Current gain, Voltage gain and output impedance in terms of h parameter and the load resistance. **(8)**

b. For a BJT $h_{ie} = 500\Omega$, $h_{fe} = 100$, $h_{re} = 10^{-4}$, $h_{oe} = 4 \times 10^{-5}$ A/V, $V_{CE} = 10V$, $I_C = 100mA$ and room temperature of 27°C. The BJT has $f_T = 50MHz$ and $C_{b'c} = 3pF$. Calculate all the parameters of the hybrid π model of the BJT. **(8)**

Q.4 a. Explain how LC tank circuit is used to generate AC oscillations in an electronic oscillator? **(8)**

b. Find an expression for the output V_0 of the amplifier shown in Fig 2. Assume op-amp is ideal. What mathematical operation does this circuit perform? **(8)**

Fig.2
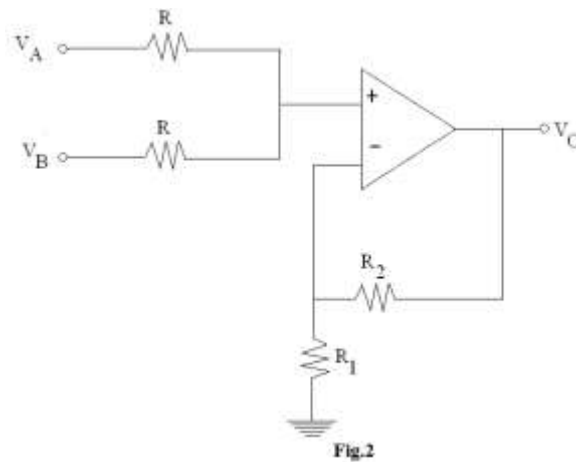
Q.5 a. Explain the working of a full wave bridge rectifier. Explain what is a ripple factor? **(8)**

b. Explain 'Junction diode switching time' to justify diode reverse recovery time. Storage time and transition time. **(8)**

Q.6 a. (i) Write minterms of $A + \overline{B}\,\overline{C}$
(ii) Write maxterms of (A+B) (B+C) **(4+4)**

b. Explain the operation of a decimal to BCD encoder. **(8)**

Q.7 a. Explain the operation of J-K flip-flop. **(8)**

b. Draw the circuit of a 3 bit synchronous counter and explain its working. **(8)**

Q.8 a. Explain the working of CMOS NAND gate and NOR gate **(8)**

b. Draw a TTL circuit with totem pole output and explain its working **(8)**

Q.9   Write short note on any **TWO** :-   **(8×2)**

  (i)   CCD
  (ii)   Seven segment Display
  (iii) Dynamic MOS
  (iv)   Bipolar memory cell.