ROLL NO. _____

Code: DE67/DC67/DE115/DC121 Subject: EMBEDDED SYSTEMS

DipIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **JUNE 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (10×2)

a. Clock of a processor is measured in
(A) Meter **(B)** Hz
(C) Kg. **(D)** Kelvin

b. Digit 10 ns is equal to
(A) 1×10^{-9} s **(B)** 10×10^{-10} s
(C) 1×10^{-8} s **(D)** 1×10^{-11} s

c. PWM stands for
(A) Power Width Modulation **(B)** Power Watch Meter
(C) Pulse Watch Modulation **(D)** Pulse Width Modulation

d. _____ is Volatile
(A) RAM **(B)** ROM
(C) REM **(D)** AND

e. SoC acronyms for
(A) State on Charge **(B)** System on Charge
(C) System of chip **(D)** System on Chip

f. Which architecture uses Parallel pipeline concept?
(A) RISC **(B)** CISC
(C) RAM **(D)** All of these

g. Term "Port" is used
(A) For I/O data fetching **(B)** As storing device
(C) As timer circuit **(D)** None of these

h. Convert Hexadecimal $(F9)_H$ to Decimal $(\quad)_D$
(A) 244 **(B)** 255
(C) 249 **(D)** 155

i. Term 'Semaphore' is related to
(A) RTOS **(B)** Microprocessor
(C) Communication protocol **(D)** Digital electronics

j. IDE platform for VxWorks is
(A) Tornado **(B)** PSOS
(C) VRTX **(D)** All of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What are the design challenges for an embedded system? **(8)**

b. Explain the main features/characteristics of embedded system in detail. **(8)**

Q.3 a. Design a 2 Input OR gate using a minimum number of CMOS transistors. **(8)**

b. Write short note on Sequential and Combinational circuits. **(8)**

Q.4 a. Define the types of architectures used for the processor. **(8)**

b. Illustrate how program and data memory fetches can be overlapped in Harvard architecture? **(8)**

Q.5 a. Draw a circuit and program to initialize the stepper motor controller for a microcontroller. **(8)**

b. What is the role of timer/counter and watch dog timer features in the embedded processor? **(8)**

Q.6 a. Write down a short note on types of memory used in the microcontroller. **(8)**

b. Explain the cache memory and memory hierarchy concept. **(8)**

Q.7 a. What do you mean by protocols? Describe the main transmission mediums. **(8)**

b. Draw a block diagram of a processor memory and peripherals connected with a system bus. Show all the relevant control and data lines of the bus. **(8)**

Q.8 a. What are the task states in RTOS? **(8)**

b. Explain the terms task, Semaphore, and process scheduler. **(8)**

Q.9 Discuss a case study for an automatic chocolate vending machine. **(16)**