ROLL NO. _____

Code: CT12 **Subject: COMPUTER ARCHITECTURE**

ALCCS

Time: 3 Hours **JUNE 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 a. State how different policies of writing into cache are implemented.

b. What do you understand by the term Computer organization, design and architecture?

c. What is the stack memory and what is the roll of stack in subroutine?

d. How do you explain the computer system from the following different views?
(i) Programmer's view
(ii) Computer architect's view

e. Apply arithmetic shift right and arithmetic shift left operation on the data $(10110011)_2$ and give your comment.

f. What is Burst mode DMA transfer?

g. Explain priority interrupt. Mention the role of polling in priority interrupt. **(4×7)**

Q.2 a. Explain the metrics used in the performance of a computer. **(9)**

b. What is the philosophy of RISC based machine? How is it diffeent from a CISC Based machine? Discuss briefly. **(9)**

Q.3 a. With neat flow chart explain the working of First Pass and Second Pass of assembler. **(9)**

b. How the performance of a system is measured? Discuss different techniques for improving system performance. **(9)**

Q.4 a. The page-address generated by a cache-main memory scheme uses demand paging and has a cache capacity of four pages. Initially the cache was having the pages 1, 2, 3, 4 in it. Which of the page-replacement policies FIFO / LRU is more suitable in this case? Justify by showing the process. **(9)**

b. Explain the IEEE-754 single precision floating point representation and its format. Represent -1.5_{10} in single precision IEEE-754 floating-point representation. **(9)**

Q.5 a. What is the difference between hardwired and micro-programmed control unit? Design a hardware control unit for a CPU capable of executing following instructions: **(2+7)**

Instruction	Instruction Code	Operation
ADD ADD	00 AAAAAA	AC ← AC + M[AAAAAA] + M[AAAAAA+1]
INC OR	01 AAAAAA	AC ← (AC+1)V M[AAAAAA]
EX-OR SKIP	1X AAAAAA	AC ← AC ⊕ M[AAAAAA], PC ← PC+1

b. Design an Associative Memory of m word, n cells per word. Derive the match logic for each word stored in the memory. Draw the internal organization of a typical cell of Associative Memory. **(9)**

Q.6 a. A digital computer has a memory unit of 64K x 16 and a cache memory of 1K word. The cache uses direct mapping with a block size of four words.
(i) How many bits are there in the tag, index, block and word field of the address format?
(ii) How many bits are there in each word of cache, and how are they divided in to functions?
(iii) How many blocks can the cache accommodate? **(9)**

b. Explain superscalar, super pipelined and VLIW architecture. **(9)**

Q.7 a. Design a look ahead carry adder and state its advantages. **(9)**

b. Explain the following: **(3×3)**
(i) Pipeline processing
(ii) Vector processing
(iii) Array processors