ROLL NO. _____

Code: AE74/AE122/AC122 **Subject: VLSI DESIGN**

AMIETE – ET/CS (Current & New Scheme)

Time: 3 Hours **JUNE 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. MOS devices are used for VLSI because of
(A) Their higher propagation delay
(B) Availability of p-channel and n-channel devices
(C) Lower silicon chip area required
(D) Availability of enhancement and depletion mode MOSFETs

b. An ideal voltage source can supply ..... current
(A) 0 A **(B)** 1 A
(C) Infinite **(D)** Depends upon the source specifications

c. A MOSFET has a drain current of 6 mA. If I_{DSS} = 12 mA, and V_p= -4V, find V_{GS}.
(A) - 3.64 V **(B)** -1.17 V
(C) - 8.84 V **(D)** - 4.10 V

d. An n- channel MOSFET has I_{DSS} = 2mA,and V_p = -4V.Its transconductance gm (in mA/V) for an applied gate to source voltage V_{GS} = -2V, is
(A) 0.25 **(B)** 0.5
(C) 0.75 **(D)** 1

e. The action of JFET in its equivalent circuit can best be represented as a
(A) Current controlled Current source
(B) Current controlled voltage source
(C) Voltage controlled voltage source
(D) Voltage controlled current source

f. The write cycle time of memory is 200ns. The maximum rate at which data can be stored is
(A) 200 words/s **(B)** 5 X 10^3 words/s
(C) 5 X 10^6 words/s **(D)** 5 X 10^9 words

g. In the semiconductor diode, V-I relationship is such that
(A) Current increase exponentially with voltage
(B) Current varies linearly with voltage
(C) Current varies inversely with voltage
(D) None on these

h. The capacitance appearing across a reverse biased semiconductor junction
(A) increases with increase in bias voltage
(B) decreases with increase in bias voltage
(C) is independent of bias voltage
(D) None of these

i. Which of the following is a layout layer in an n-well CMOS process?
(A) n-type substrate **(B)** contact
(C) p- type substrate **(D)** transistor gate

j. The density of the dynamic RAM is
(A) More than that of the static RAM
(B) less than that of the static RAM
(C) Equal to that of the static RAM
(D) equal to or more than that of the static RAM

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw VLSI design flow chart and explain its design steps in detail. **(8)**

b. Explain the main steps required in a typical n-MOS fabrication. **(8)**

Q.3 a. Find pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistors. **(8)**

b. Determine drain-to-source current I_{DS} vs voltage V_{DS} relationship in all three regions of operations of an n-MOS transistor. **(8)**

Q.4 a. What is stick diagram? Explain with suitable example of nMOS inverter and p-well CMOS inverter. **(8)**

b. Give significance of well rule and transistor rule for layout design. Take an example of CMOS n-well process transistor and well contact construction to explain it. **(8)**

Q.5 a. Derive mathematical expression for rise-time estimation and fall-time estimation of CMOS inverter. **(8)**

b. Sketch a 3-input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R). **(8)**

Q.6 a. Describe various scaling model & scaling factors. Discuss the impact of scaling on
(i) Gate Area, (ii) C_{ox},
(iii) C_g (iv) Gate delay **(8)**

b. Draw structured design of parity generator. **(8)**

Q.7 a. What are the problems associated with VLSI design? How these can be reduced? **(8)**

b. Design a 4-bit adder and draw its truth table. **(8)**

Q.8 a. Explain area, power dissipation and volatility for three-transistor dynamic RAM cell. Also draw its circuit and stick diagram. **(8)**

b. What is design for testability? Explain main approaches for DFT. **(8)**

Q.9 a. Why test programs are required? Give various attributes of a tester. **(8)**

b. Explain the role of CAD tools for design and simulation of a chip. **(8)**