ROLL NO.	

Code: AE68/AE117 Subject: EMBEDDED SYSTEMS DESIGN

AMIETE - ET (Current & New Scheme)

Time: 3 Hours JUNE 2017 Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following:

 (2×10)

- a. CAN (Controller Area network) bus is:
 - (A) Serial communication protocol
 - (B) Parallel communication protocol
 - (C) Wireless communication protocol for large distance
 - (**D**) Wireless communication for short distance
- b. In the DMA (Direct Memory Access) which operation is performed?
 - (A) The Microprocessor does not need to jump to an ISR
 - **(B)** Microprocessor execute its regular program
 - (C) Data transfer between memories and peripherals is without use of microprocessor
 - (**D**) All of these
- c. Among DRAM, EEPROM and NVRAM which is/are non-volatile memory.
 - (A) Both EEPROM and NVRAM
- (B) Only EEPROM
- (C) Both DRAM and EEPROM
- (D) Only DRAM
- d. The state where a process is incepted in to the memory and waiting the process time for execution, is known as
 - (A) Create state

(B) Blocked state

(C) Ready state

- (D) Running state
- e. Among the following statements which is/are correct:
 - (i) Queens, pipes, mailbox semaphores and event may be used for communication between two tasks or task and interrupt routine.
 - (ii) Event is simpler than semaphores.
 - (iii) Semaphores are usually the fastest and simplest method
 - (A) Only (i) is true

- (B) Both (i) and (ii) are true
- (C) Only (ii) is true
- (D) Both (i) and (iii) are true
- f. Interrupt routine in an RTOS must adhere following rules:
 - (i) They must not call RTOS functions that block.
 - (ii) They must not call any RTOS function unless the RTOS know that an interrupt routine is running.
 - (iii) They can call the RTOS functions that block
 - (A) Both (i) and (ii) are true
- (B) Only (i) is true
- (C) Only (ii) is true
- (**D**) All are true

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	g.	 (i) Generalised architecture (iii) Tightly constrained (A) Only (i), (ii) and (iii) are true (C) Only (iii) and (iv) are true 	(ii) Single functioned (iv) Relative and real time (B) Only (ii), (iii) and (iv) are true (D) All are true
	h.	Datapath unit of controller is used to (A) Perform only Arithmetic operat (B) Generate control signals for cor (C) Perform data routing and all type (D) Perform logical operations only	ions. atroller oes of arithmetic, logical and data routing.
	i.	Which type of addressing mode is u	sed in instruction $MOV @R_d$, R_s ?
		(A) Register indirect(C) Relative	(B) Indirect(D) Direct
	j.	Fallowing statements are given for (i) It helps programmers to correct (ii) Support stepwise program (iii) Allow the user specific breakpo (A) Only (i) is true (C) Only (ii) is true	the programs
		Answer any FIVE Questions Each question car	_
Q.2	a.	-	system design process. Clearly mention the (6)
	b.	Explain the given addressing mode Indirect, Immediate, Direct, Registe	<u> </u>
	c.	Explain the methods of IC technological method?	ogy. What are the application areas of each (4)
Q.3	a.	What are the major combination design? How are they used in design	al components required at the RT- level n? (6)
	b.	Draw the block diagram of general data path unit and control unit.	-purpose processor, explain the function of (6)
	c.	What is application specific inst methods to implement this?	ruction-set processor? What are different (4)
		methods to implement this:	· ·
Q.4	a.	-	with example and write the pseudo code for (6)
Q.4		What is watchdog timer? Explain what.	with example and write the pseudo code for

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Q.5	a.	Draw and explain the memory hierarchy. Explain the direct mapping procedure of cache mapping. (6)
	b.	Explain the architecture and operation of the basic DRAM with suitable block diagram. (6)
	c.	Write short technical note on: OTPROM and EPROM (4)
Q.6	a.	Discuss the Standard I/O (I/O mapped I/O) with example and compare it with memory mapped I/O. (6)
	b.	Discuss CAN bus and IEEE802.11 wireless LAN protocol. (6)
	c.	Explain daisy-chain arbitration method with necessary diagram. (4)
Q.7	a.	"Interrupt routine in most RTOS environment must follow two rules that do not apply to task code". What are these two rules? Explain rule 1 with suitable example. (6)
	b.	How does the RTOS know to setup the timer hardware on his particular hardware? How accurate are the delay produced by the <i>taskDelay</i> function? What you have to do if the system needs extremely accurate timing? (6)
	c.	Compare the operation performed for the communication between two tasks using semaphore, events and queues.
Q.8	a.	Define the function of scheduler in reference of RTOS. Draw the state diagram of task and clearly show the transition among the three tasks. (6)
	b.	Define the semaphore in reference of RTOS in detail. How will it solve the shared data problems? (6)
	c.	What are the different methods to protect the shared data? Explain each method in brief. (4)
Q.9	a.	An underground tank monitoring system monitors the multiple underground tanks. This complete work should be divided in to tasks. Give the name of tasks created, their priority and reason for creating that task. (6)
	b.	What are the semaphore problems? Explain with diagram. (6)
	c.	Write the different methods to achieve the power saving in embedded system design. (4)