ROLL NO. _____

**Code: AE66/AC66/AT66/ AE108/AC108/AT108**
**Subject: MICROPROCESSORS & MICROCONTROLLERS**

## AMIETE – ET/CS/IT (Current & New Scheme)

**Time: 3 Hours** **JUNE 2017** **Max. Marks: 100**

***PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.***

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or the best alternative in the following: (2×10)**

a. Which register pair is not accessible by user?
**(A)** AB **(B)** WZ
**(C)** DE **(D)** HL

b. What is SIM in 8085 Microprocessor?
**(A)** Select Interrupt Mask **(B)** Set Interrupt Mask
**(C)** Start Interrupt Mask **(D)** Sort Interrupt Mask

c. Which kind of stack memory is used in 8085 microprocessor?
**(A)** First In, First Out **(B)** First In, Last Out
**(C)** Last In, First Out **(D)** Last In, Last Out

d. A device employing INTR line for device interrupt puts the CALL instruction on the data bus while
**(A)** $\overline{INTA}$ is active **(B)** HOLD is active
**(C)** READY is active **(D)** None of these

e. To put the 8085 microprocessor in the wait state
**(A)** lower the HOLD input **(B)** lower the READY input
**(C)** raise the HOLD input **(D)** raise the READY input

f. Which flag is used to perform DAA instruction in 8085 microprocessor?
**(A)** S **(B)** Z
**(C)** AC **(D)** P

g. The advantage of memory mapped I/O over mapped I/O is,
**(A)** Faster
**(B)** Many instruction supporting memory mapped I/O
**(C)** Require a bigger address decoder
**(D)** All of these

h. 8279 is
**(A)** Programmable Timer/Counter **(B)** Interrupt Controller
**(C)** DMA Controller **(D)** Keyboard Controller

i. How is the status of the CY, AC and P flag affected, after the following program is executed?
MOV A,#9Ch
ADD A,#64H

**(A)** CY=0, AC=0, P=0 **(B)** CY=1, AC=1, P=0
**(C)** CY=0, AC=1, P=0 **(D)** CY=1, AC=1, P=1

j. In 8051 microcontroller, which of the following has the highest priority, with default values in IP register?
**(A)** INT0 **(B)** Timer 0 overflow
**(C)** INT1 **(D)** Serial port

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2** a. Describe about various control and status signals of 8085 microprocessor. Explain the sequence of events that occurs when 8085 MPU reads instruction code from memory, with neat diagram. **(8)**

b. Describe about de-multiplexing of the bus (AD7-AD0) for 8085 microprocessor. Explain how various read/write control signals are generated for memory and I/O operations. **(8)**

**Q.3** a. Differentiate between peripheral mapped I/O and memory mapped I/O. Design a seven-segment LED output port with the device address F5H, using a 3-to-8 decoder, 4-input NAND gate, 2-input NOR gate and a common-anode seven segment LED. **(8)**

b. Explain the operational difference between **any four** pairs of instructions: **(8)**
(i) SPHL and XTHL (ii) CALL and JMP addr
(iii) LHLD and SHLD addr (iv) XRA A and MVI A, 00h
(v) INR A and ADI 01h (vi) DAD $R_p$ and DAA

**Q.4** a. Write a program to sort given 10 numbers from memory location 2200H in the ascending order. **(8)**

b. Divide 16-bit number stored in memory locations 2200H and 2201H by the 8-bit number stored at memory location 2202H. Store the quotient in memory locations 2300H and 2301H and remainder in memory locations 2302H and 2303H. **(8)**

**Q.5** a. Explain how 8085 responds to INTR interrupt. Explain the software interrupts supported by 8085. **(8)**

b. Explain any two of the following modes for 8253/54 programmable interval timer. **(8)**
(i) Interrupt on terminal count
(ii) Rate generator
(iii) Square wave rate generator

**Q.6** a. A set of eight current readings is stored in memory locations starting at XX40h. Check data byte for D7 and D0 bits. If D7 or D0 is 1, reject the data byte, otherwise store the data bytes at the memory location starting at XX60h. **(8)**

b. Transfer ten bytes of data from one memory to another memory block. Source memory block starts from memory location 2200H, where as destination memory block starts from memory location 2300h. **(8)**

**Q.7** a Write a note on different registers used in 8259. **(8)**

b. Explain the function of $A_{3-0}$, MR*, MW*, IOR*, IOW* and $D_{7-0}/AE_{15-8}$ pins of 8257 when it is working as **(8)**
(i) Slave to the processor
(ii) Master controlling DMA data transfer

**Q.8** a. (i) Write a program to initialise 8255 in the configuration given below: **(3)**
- Port A: Simple input
- Port B: Simple output
- Port $C_L$: Output
- Port $C_U$: Input

Assume address of the control word register of 8255 as 83H.

(ii) Write a program to blink Port C bit 0 of the 8255. Assume address of control word register of 8255 as 83H. Use Bit Set/Reset mode. **(5)**

b. Differentiate between synchronous and asynchronous transmission in USART. **(8)**

**Q.9** a. Explain the various addressing modes of 8051. **(8)**

b. Write a program to perform 16-bit subtraction of Minuend and Subtrahend located at External memory location 76h, 77h and 78h, 79h respectively. Store result at External memory location 80h, 81h, 82h. **(8)**