ROLL NO. _____

Code: AC58/AT58/AC106/AT106 Subject: COMPUTER ORGANIZATION

AMIETE – CS/IT (Current & New Scheme)

Time: 3 Hours **JUNE 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. If a system is 64 bit machine, then the length of each word will be _____
(A) 4 bytes **(B)** 8 bytes
(C) 16 bytes **(D)** 12 bytes

b. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
(A) Relative **(B)** Indirect
(C) Index with Offset **(D)** Immediate

c. The alternate way of writing the instruction, ADD #5,R1 is _____
(A) ADD [5],[R1]; **(B)** ADDI 5,R1;
(C) ADDIME 5,[R1]; **(D)** There is no other way

d. When the process is returned after an interrupt service _____ should be loaded again

i. Register contents
ii. Condition codes
iii. Stack contents
iv. Return addresses

(A) i, iv **(B)** ii, iii and iv
(C) iii, iv **(D)** i, ii

e. IDE disk is connected to the PCI BUS using _____ interface.
(A) ISA **(B)** ISO
(C) ANSI **(D)** IEEE

f. A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM is
(A) 4 **(B)** 5
(C) 6 **(D)** 7

g. _____is used to implement virtual memory organisation.
(A) Page table **(B)** Frame table
(C) MMU **(D)** None of these

h. A 32-bit CLA is constructed using 4-bit CLAs with logic to generate c4 from c0, c8 from c4, c12 from c8 and so on and a 3-input XOR gate is used to generate Si from Ci, how many gate delays are required to generate S29?
(A) 16 **(B)** 20
(C) 18 **(D)** 19

i. What will be the Single Precision floating point format of the decimal value -1.75
(A) 1 1000 0000 111000 000000 000000 00000
(B) 1 0111 1111 111000 000000 000000 00000
(C) 1 1000 0000 110000 000000 000000 00000
(D) 1 0111 1111 110000 000000 000000 00000

j. In _____ technology, the implementation of the register file is by using an array of memory locations.
(A) VLSI **(B)** ANSI
(C) ISA **(D)** ASCI

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw the diagram to show how the memory and the processor can be connected. Discuss the various components in it.
List the steps needed to execute the machine instruction
Load R2, LOC
in terms of transfers between the components and some simple control commands. Assume that the address of the memory location containing this instruction is initially in register PC. **(8)**

b. Represent both positive and negative numbers using following number systems. Prepare a table to show all three representations using 3-bit numbers.
1. Sign-and-magnitude
2. 1's-complement
3. 2's-complement
Also prepare a table to represent the decimal values 5, -2, 26, -10, -19 and 51 as signed, 7-bit numbers in the signed and magnitude, 1's complement and 2's complement form. **(8)**

Q.3 a. Register R1 and R2 contain the decimal values 1400 and 5000. What is the effective address in each instruction if each of them is executed independently? Assume word size of 32 bits and it is byte addressable.
(i) Load R5, X(R1) (X is equal to -20 represented using 16 bits)
(ii) Move R5, #3000
(iii) Store 30(R1,R2),R5
(iv) Add R5, (R2)+
(v) Subtract R5, –(R1) **(1x5)**

b. Explain with syntax and examples, any two addressing modes supported by CISC but not supported by RISC. **(4)**

c. Explain the following logical and arithmetic shift instructions with example:
(i) Logical shift left
(ii) Logical shift right
(iii) Arithmetic shift right **(2+2+3)**

Q.4 a. With neat diagram, explain the use of DMA controllers in a computer system.**(5)**

b. Explain the following:
(i) Handshaking scheme for controlling data transfers on the bus between the master and the slave.
(ii)Timing of an input transfer on a synchronous bus
(iii) Handshake control of data transfer during an output operation **(3+4+4)**

Q.5 a. With neat block diagram explain serial port. **(6)**

b. Explain how PCI bus operates. **(10)**

Q.6 a. Draw static RAM cell and explain how read and write operations are performed. **(8)**

b. A 2-way set associative cache consists of a total of 64 blocks. The main memory contains 4096 blocks, each block consisting of 128 words.
(i) How many bits will be there in a main memory address?
(ii) How many bits will be there in each of the tag, set, word fields?
(iii) How many bits will be there in each of the tag, set, word fields, if the cache is 4-way set associative? **(1x3)**

c. What is memory interleaving? Explain it with neat diagram. **(5)**

Q.7 a. With a neat sketch, explain the process of address translation in virtual memory **(8)**

b. In a disk system there are 29 recording surfaces. The diameter of each recording surface is 30 cm and the inter track distance is 0.05 cm. All the disks are 2 sided

disks except for one disk. There is an average of 360 sectors per track and each sector contains 512 bytes of data.
(i) How many tracks will be there in total in a two sided disk?
(ii) How many disks will be there in the entire system?
(iii) What is the total capacity of the disk system? **(1x3)**

c. Convert the following pairs of decimal numbers to 5-bit 2's-complement numbers, then perform addition and subtraction on each pair. Indicate whether or not overflow occurs for each case.
(i) 7 and 13
(ii) −12 and 9 **(2.5+2.5)**

Q.8 a. Explain Booth's algorithm for 2's complement multiplication and multiply (+8) x (-5) using this algorithm. **(8)**

b. Consider the following 12-bit floating-point number representation format. The first bit is the sign of the number. The next five bits represent an excess 15 exponent for the scale factor, which has an implied base of 2. The last six bits represent the fractional part of the mantissa, which has an implied 1 to the left of the binary point. Represent the number in binary and perform Subtract and Multiply operations on the operands. **(8)**

A =	0	10001	011011
B =	1	01111	101010

Q.9 a. With the neat block diagram explain a complete processor. **(5)**

b. Consider the instruction ADD (R3),R1
(i) Write the steps required for execution of above instruction
(ii) Control sequence for execution of the above instruction. **(5)**

c. With neat block diagram, explain control unit organization. **(6)**