ROLL NO. _____

Code: AC103/AT103 Subject: ANALOG AND DIGITAL ELECTRONICS

AMIETE – CS/IT (New Scheme)

Time: 3 Hours **JUNE 2017** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The temperature coefficient of an intrinsic semiconductor is
(A) zero. **(B)** positive.
(C) negative. **(D)** None of these.

b. The width of depletion layer of a P-N junction
(A) decreases with light doping. **(B)** increases with heavy doping.
(C) is independent of applied voltage. **(D)** is increased under reverse bias.

c. Bridge rectifiers are preferred because
(A) they require small transformer.
(B) they have less peak inverse voltage.
(C) they need small transformer and also have less peak inverse voltage.
(D) they have low ripple factor.

d. An emitter in a bipolar junction transistor is doped much more heavily than the base as it increases the
(A) emitter efficiency. **(B)** base transport factor.
(C) forward current gain. **(D)** All of these.

e. In an R-C phase shift oscillator, the minimum number of R-C networks to be connected in cascade will be
(A) one. **(B)** two.
(C) three. **(D)** four.

f. The decimal equivalent of hexadecimal number **03E3** is
(A) 3416 **(B)** 2989
(C) 205 **(D)** 1000

g. According to De-Morgan's second theorem
(A) A NAND gate is always complementary to an AND gate.
(B) An AND gate is equivalent to a bubbled NAND gate.
(C) A NAND gate is equivalent to a bubbled AND gate.
(D) A NAND gate is equivalent to a bubbled OR gate.

h. In a sequential circuit, the output state depends upon
(A) past output states and present input states.
(B) input states only.
(C) input and output states.
(D) None of these.

i. D flip-flop can be configured from
(A) J-K flip-flop and an inverter. **(B)** R-S flip-flop.
(C) R-S flip-flop and an inverter. **(D)** Both **(A)** and **(B)**

j. The number of flip-flops required in a decade counter is
(A) 2 **(B)** 3
(C) 4 **(D)** 10

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is forbidden energy gap? Differentiate among insulators, semiconductors and conductors on the basis of band gap. **(4)**

b. A copper wire of 2 mm diameter with conductivity of 5.8×10^7 s/m and electron mobility of 0.0032 m^2 / V-s is subjected to an electric field of 20 mv/m. Find **(6)**
(i) charge density of free electrons (ii) current density
(iii) drift velocity of the electron

c. What are the two basic types of capacitances associated with P-N junction? How will you represent the capacitive effect of a practical diode on an ideal diode? **(6)**

Q.3 a. What is the necessity of having filter in the power supply? Explain the following characteristics of a power supply **(8)**
(i) peak Inverse voltage (ii) ripple factor
(iii) rectification efficiency (iv) regulation
(v) TUF (transformer utilization factor)

b. What is the difference between clipping and clamping? Explain the operation of a positive Clamper circuit with its output waveform for an ideal diode. **(8)**

Q.4 a. What do you understand by transistor biasing? Why is it necessary to bias a transistor? Explain the operation of a potential -divider bias circuit. **(8)**

b. Derive the relationship between α and β of a transistor. In a transistor I_C =0.95 mA, I_E = 1 mA. Determine I_B, α and β in CB Configuration. **(8)**

Q.5 a. A single stage amplifier has a gain of 60. The collector load R_C = 500 Ω, hfe =50 and the input impedance is 1KΩ. Calculate the load when two stages are cascaded through capacitor coupling. **(6)**

b. Draw the circuit of R-C phase shift oscillator and derive an expression for its frequency of oscillation. **(10)**

Q.6 a. What is the trade-off between parallel and serial transmission of binary data? **(3)**

b. Differentiate between Static and Dynamic RAM. **(4)**

c. Find out the following **(9)**
(i) Octal equivalent of $(2F.C4)_{16}$.
(ii) Decimal equivalent of $(1A2B)_{16}$
(iii) Gray code equivalent of $(15)_D$

Q.7 a. How will you use an Ex-OR gate as an inverter? **(4)**

b. Implement $Y = \overline{AB} + A + \overline{(B + C)}$ using NAND gate only. **(4)**

c. Simplify the following three-variable expression using Boolean algebra **(4)**
Y (A, B, C) = Σm (0, 1, 3, 4, 7)

d. Simplify the following Boolean expression using Karnaugh map **(4)**
Y = Σm(1,3,7,11,15) + d(0, 2, 5)

Q.8 a. Write down the following decimal numbers in 2's complement representation using 8 bits **(4)**
(i) -44 (ii) 64

b. Explain the operation of a 4-bit parallel binary adder using cascaded full-adders. **(4)**

c. Design a two-bit comparator circuit. **(8)**

Q.9 a. Briefly explain why a ripple counter's maximum usable clock frequency decreases as more flip-flops are added to the counter to increase its mod number. **(4)**

b. What is meant by the race around condition in J-K flip-flop? How can it be overcome? **(4)**

c. With the help of schematic arrangement, explain, how a J-K flip-flop can be used as a D flip-flop? **(4)**

d. Draw a synchronous MOD-16 down counter. **(4)**