ROLL NO. _____

Code: DE67 / DC67 **Subject: EMBEDDED SYSTEMS**

DipIETE – ET/CS

Time: 3 Hours **JUNE 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. The number of tasks that can be processed per unit time is called

(A) Latency **(B)** Response Time
(C) Bit rate **(D)** None of these

b. The performance could be measured as

(A) Latency **(B)** Throughput
(C) Both **(A)** and **(B)** **(D)** None of these

c. A register-transfer (RT) synthesis tool converts FSM and RT into

(A) Data path **(B)** Control path
(C) Both **(A)** and **(B)** **(D)** None of these

d. ASIP's are designed to perform

(A) Embedded applications **(B)** All processing
(C) Domain-specific processing **(D)** Only network routing

e. The ISA bus protocol is common in

(A) 8085 processors **(B)** 8086 processors
(C) Both **(A)** and **(B)** **(D)** None of these

f. Which of the following is incorrect common design metrics?

(A) Size, Performance, flexibility
(B) Maintainability, correctness, safety
(C) NRE cost, unit cost, power
(D) Rigid, linearity, sturdy

g. A sequential circuit is a digital circuit whose outputs are a function of

(A) Present as well as previous input values
(B) Present values
(C) Previous values
(D) None of these

h. Emulator supports

(A) Debugging the program while it executes on development processor
(B) Debugging the program while it executes on target processor
(C) Programmers to evaluate and correct their programs
(D) Programmers to convert HLL to MLL

i. Baud rate is defined as

(A) Number of signals changes per second
(B) Number of bits per second
(C) Number of signals changes per minute
(D) Number of bits per minute

j. Storage permanence is defined as

(A) Storage capacity
(B) Ability of memory to hold its stored data
(C) Size of the memory
(D) None of these

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain design metrics used for embedded systems. **(10)**

b. Compute the annual growth rate of IC capacity and designer productivity. **(6)**

Q.3 a. Design a single purpose processor that outputs Fibonacci number upto n places. Start with a function computing the desired result, translate it into a state diagram and sketch a probable datapath. **(12)**

b. Briefly explain the following:
(i) Combinational & Sequential circuit
(ii) Single purpose processor and general purpose processor **(4)**

Q.4 a. With example explain how program & data memory can be overlapped in Harvard architecture. **(6)**

b. Explain the following:
(i) Device programmers (ii) Linker
(iii) Cross compiler (iv) System call
(v) Pipelining **(10)**

Q.5 a. Given a timer with a terminal count and a clock frequency of 10 MHz calculate the following:
(i) Range & Resolution
(ii) Terminal count values needed to measure 3ms interval
(iii) If the prescaler is added, what is the minimum division needed to measure an interval of 100 ms
(iv) Instead of a prescalar assume 16-bit up counter is cascaded, what is the range and resolution of this design? **(8)**

b. With example, explain watch dog timer and reaction timer. **(8)**

Q.6 a. Explain direct and fully associative cache mapping technique. **(8)**

b. Given the following three cache designs, find the one with the best performance by calculating the average cost of access. Show all calculations.
(i) 4 Kbytes, 8-way set associative cache with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycle
(ii) 8 Kbyte, 4-way set associative cache with a 4% miss rate; cache hit costs two cycle, cache miss costs 12 cycle
(iii) 16 Kbyte, 2-way set associative cache with a 2% miss rate; cache hit costs three cycle, cache miss costs 12 cycle. **(8)**

Q.7 a. Compare the serial protocols, parallel protocols and wireless protocols interms of formats, speed, performance and security issues. **(8)**

b. Briefly explain two popular parallel protocol used in embedded system. **(8)**

Q.8 a. List the detailed functions inside the digital camera. **(10)**

b. List the requirements of a sub-system for application, which is transmitting a TCP/IP stack. **(6)**

Q.9 a. Describe Task, Task states and RTOS. **(10)**

b. Explain the following terms in brief:

(i) Scheduler
(ii) Semaphore
(iii) Re-entrant function **(6)**