ROLL NO.	

Code: DE58 / DC58 Subject: LOGIC DESIGN

## **Diplete - ET/CS**

Time: 3 Hours

**JUNE 2013** 

Max. Marks: 100

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1	Choose the correct or the best alternative in the following:
V.1	choose the correct of the best afternative in the following.

 $(2\times10)$ 

- a. In Boolean algebra a + ab = a is \_\_\_\_\_
  - (A) Involution Law
- (B) De Morgan Law
- (C) Absorption Law
- (D) Idempotent Law
- b. One of the following is equivalent to AND-OR realization is \_\_\_\_\_
  - (A) NAND-NOR realization
- **(B)** NOR-NOR realization
- (C) NOR-NAND realization
- (D) NAND-NAND realization
- c. The number of cells in a 4-variable K-map is \_\_\_\_\_
  - **(A)** 4

**(B)** 16

**(C)** 8

- **(D)** 64
- d. J-K flip-flop is made to toggle in one of the following condition
  - **(A)** J = 0, K = 0

**(B)** J = 1, K = 0

**(C)** J = 0, K = 1

- **(D)** J = 1, K = 1
- e. A shift register which can enter the data into it only one bit at a time, but has all data bits available as outputs is \_\_\_\_\_
  - (A) Serial In / Serial Out
- (B) Serial In / Parallel Out
- (C) Parallel In / Serial Out
- (**D**) Parallel In / Parallel Out

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- f. The switching function  $f = \sum m(1,2,4,8,10,14)$  is implemented by using decoder
  - **(A)** 4 x 16

**(B)** 3 x 8

(C) 2 x 4

- **(D)** 5 x 32
- g. A Flip-Flop has two outputs which are \_\_\_\_\_
  - (A) always zero

- (B) always one
- (C) always complementary
- (**D**) in one of the above status

- h. Gray Code is:
  - (A) non-weighted code
- (B) adjacent code differ by one bit

(C) reflected code

- (D) all of these
- i. An example of canonical SOP is \_\_\_\_\_
  - (A) ABC+BC+AB
- **(B)** AB

(C) ABC + AB

- **(D)**  $A\overline{B}C + AB\overline{C}$
- j. The memory which can be programmed by the user and then cannot be erased and reprogrammed is \_\_\_\_\_
  - (A) ROM

(B) PROM

(C) EPROM

(D) EEPROM

## Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

- **Q.2** a. Perform the following conversions
  - (i)  $(7825.6875)_{10} = (?)_8$
  - (ii)  $(A4F)_{16} = (?)_8$
  - (iii)  $(3F2A)_{16} = (?)_2$

(iv) 
$$(546)_8 = (?)_{16}$$

(8)

- b. Compare Analog and Digital systems. Explain the advantages and disadvantages of digital systems over analog systems. (8)
- Q.3 a. Implement two input EX-OR gate using minimum number of two input NOR gates only. (4)
  - b. Simplify the Boolean function  $f(w, x, y, z) = \sum (0,1,6,7,14,15) + \sum d(3,4,11,12)$  by using the don't care conditions "d" in
    - (i) SOP Form
    - (ii) POS Form

**(8)** 

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- c. Find the simplified complemented expression for the function  $f(A, B, C) = ABC + \overline{ABC} + \overline{ABC} + \overline{ABC}$  (4)
- Q.4 a. Explain the working of JK Flip Flop with the help of its logic diagram, characteristic equation, state table and excitation table. (8)
  - b. Describe the working of 4 bit Serial In Serial Out Shift Register using logic diagram and waveforms. (8)
  - Q.5 a. Represent (275)<sub>10</sub> and (641)<sub>10</sub> in BCD and then perform BCD addition. Verify the answer by converting back to decimal.
    - b. Describe the working of a five bit parallel Binary adder circuit using full adders. (8)
    - c. Compute the following using 2's complement arithmetic (i) 9 4 (ii) 4 + 9 (4)
  - Q.6 a. Explain the operation of a 4 bit Asynchronous Up Counter using JKFF, with the help of logic diagram and waveforms.(8)
    - b. Design a MOD 5 Synchronous Counter using D Flip Flops. (8)
  - Q.7 a. Draw and explain the logic circuit and truth table for an Octal to Binary Encoder. (8)
    - b. Design a 1 line to 8 line demultiplexer. (8)
- Q.8 a. Distinguish between Serial in /Parallel out and Parallel in/Serial out shift registers. (8)
  - b. Design a three bit serial in serial out shift register using JKFF. (8)
- Q.9 a. Describe the timing diagrams for read cycle and write cycle for static RAM. (8)
  - b. Write a short note on the following:
    - (i) Static memory device
- (ii) Dynamic memory device

(iii) Access time

(iv) External memory