ROLL NO. _____

Code: DC57 **Subject: COMPUTER ORGANIZATION**

DipIETE – CS

Time: 3 Hours **JUNE 2013** **Max. Marks: 100**

PLEASE WRITE YOUR ROLL NO. AT THE SPACE PROVIDED ON EACH PAGE IMMEDIATELY AFTER RECEIVING THE QUESTION PAPER.

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Which of the following logical operations produce a '0' if the three inputs 0, 1, 1 are given?

(A) OR **(B)** NAND
(C) Exclusive-OR **(D)** None of these

b. Which of the following is true about program counter?

(A) It is a cell in ROM
(B) It is a register
(C) During the execution of the current instruction content remain unaffected.
(D) None of these

c. The idea of cache memory is based

(A) on the property of locality of reference
(B) on the heuristic 90-10 rule
(C) on the fact that references generally tend to cluster
(D) All of the above

d. X + Y can be implemented by

(A) NAND gate alone **(B)** AND alone
(C) XOR gate alone **(D)** None of these

e. On receiving an interrupt from an input/output device, the CPU

(A) Halts for a pre determined time
(B) Transfer the control of addressing and data bus to the interrupting device
(C) Branches off to the interrupt service routine immediately
(D) Branches off to the interrupt service routine after completion of the current instruction.

f. Which of the following is not a weighted code?

(A) Decimal Number system **(B)** Excess 3-code
(C) Binary number System **(D)** None of these

g. If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10 ns memory) is

(A) 93 % **(B)** 90 %
(C) 88 % **(D)** 87 %

h. Part of the operating system is usually stored in ROM so that it can be used to boot up the computer. ROM is used rather than RAM because

(A) ROM chips are faster than RAM **(B)** ROM chips are not volatile
(C) ROM chips are cheaper than RAM chips **(D)** none of these

i. In a vectored interrupt

(A) the branch address is obtained from a register in the processor
(B) the interrupting source supplies the branch information to the processor through an interrupt vector
(C) the branch address is assigned to a fixed location in memory
(D) none of the above

j. Von Neumann computers execute

(A) Java programs **(B)** Assembly language programs
(C) C programs **(D)** Machine language programs

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. How do various factors like Hardware design, Instruction set, Compiler related to the performance of a computer? **(10)**

b. What are the various Instruction categories? **(6)**

Q.3 a. Consider the symbolic instruction ADD 3000, 5000. Memory locations 3000 and 5000 contain the operands. Suppose the program is stored from the locations 2000. Explain the fetch-decode-execute cycle of this instruction, showing clearly the roles of special purpose registers, Control Unit and ALU. Data is stored in memory locations 3000 and 5000 show how this is fetched and decoded **(10)**

b. A program begins from memory location 4000H. An instruction MOV 600AH, R1 is stored in the memory starting from location 4020H. Assume that the whole program is shifted to a locations starting from 6000H. The memory location 600AH, which contained the data to be moved to register R1 is over written by the content of the program. Suggest solutions to overcome this situation. **(6)**

Q.4 a. What do you mean by bus arbitration? Differentiate between centralized and distributed arbitration. **(8)**

b. How the interrupt-service routine is different from that of a subroutine? Summarize the sequence of events involved in handling an interrupt request from a single device. **(8)**

Q.5 a. What are the various functions of Input/output interface? **(6)**

b. With the help of a block diagram show a typical arrangement in which different interfaces are used to connect various peripheral devices. **(10)**

Q.6 a. Explain with a neat sketch the internal organization of a memory chip consisting of 16 words of 8 bits each (16 × 8 organisation). **(8)**

b. Outline the three cache mapping policies: direct mapping, associative mapping and set associative mapping. Briefly discuss the advantages and disadvantages of each. **(8)**

Q.7 a. What is full adder and n-bit ripple-carry adder? Explain logic specification for a stage of binary addition. **(8)**

b. Explain virtual-memory address translation scheme with the help of a diagram. **(8)**

Q.8 a. Explain Booths algorithm for multiplying two signed binary numbers. **(8)**

b. Give algorithm for restoring division. Also draw a logic circuit that implements restoring division. **(8)**

Q.9 a. Using suitable example, explain how a word is fetched from memory and how it is stored in memory. **(8)**

b. Draw the block diagram of a basic hardwired control organisation with two decoders, a sequence counter and a number of control logic gates. Explain. **(8)**